

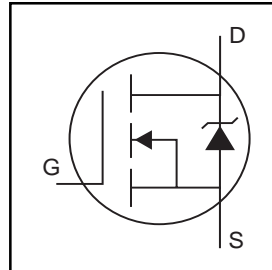
HEXFET® Power MOSFET

- Surface Mount
- Available in Tape & Reel
- Dynamic dv/dt Rating
- Logic-Level Gate Drive
- $R_{DS(on)}$ Specified at $V_{GS}=4V$ & $5V$
- Fast Switching
- Ease of Paralleling

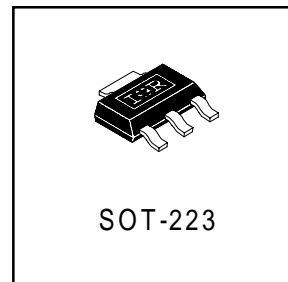
Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SOT-223 package is designed for surface-mount using vapor phase, infra red, or wave soldering techniques. Its unique package design allows for easy automatic pick-and-place as with other SOT or SOIC packages but has the added advantage of improved thermal performance due to an enlarged tab for heatsinking. Power dissipation of greater than 1.25W is possible in a typical surface mount application.



$V_{DSS} = 60V$
$R_{DS(on)} = 0.20\Omega$
$I_D = 2.7A$



Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ $T_c = 25^\circ C$	Continuous Drain Current, V_{GS} @ 10 V	2.7	A
I_D @ $T_c = 100^\circ C$	Continuous Drain Current, V_{GS} @ 10 V	1.7	
I_{DM}	Pulsed Drain Current ①	22	
P_D @ $T_c = 25^\circ C$	Power Dissipation	3.1	W
P_D @ $T_A = 25^\circ C$	Power Dissipation (PCB Mount)**	2.0	
	Linear Derating Factor	0.025	
	Linear Derating Factor (PCB Mount)**	0.017	$W/^\circ C$
V_{GS}	Gate-to-Source Voltage	-/+10	V
E_{AS}	Single Pulse Avalanche Energy②	100	mJ
I_{AR}	Avalanche Current①	2.7	A
E_{AR}	Repetitive Avalanche Energy①	0.31	mJ
dv/dt	Peak Diode Recovery dv/dt ③	4.5	V/ns
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to + 150	$^\circ C$
	Soldewring Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-PCB	—	40	$^\circ C/W$
$R_{\theta JA}$	Junction-to-Ambient. (PCB Mount)**	—	60	

** When mounted on 1" SQUARE pcb (FR-4 or G-10 Material).

For recommended footprint and soldering techniques refer to application note #AN-994.

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	60	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.073	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.20	Ω	$V_{GS} = 5.0V, I_D = 1.6A$ ④
		—	—	0.28		$V_{GS} = 4.0V, I_D = 1.4A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	2.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
g_{fs}	Forward Transconductance	3.2	—	—	S	$V_{DS} = 25V, I_D = 1.6A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS} = 60V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 48V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 10V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -10V$
Q_g	Total Gate Charge	—	—	8.4	nC	$I_D = 10A$
Q_{gs}	Gate-to-Source Charge	—	—	3.5		$V_{DS} = 48V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	6.0		$V_{GS} = 5.0V$, See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	9.3	—	ns	$V_{DD} = 30V$
t_r	Rise Time	—	110	—		$I_D = 10A$
$t_{d(off)}$	Turn-Off Delay Time	—	17	—		$R_G = 12\Omega$
t_f	Fall Time	—	26	—		$R_D = 2.8\Omega$, See Fig. 10 ④
L_D	Internal Drain Inductance	—	4.0	—	nH	Between lead, 6mm(0.25in) from package and center of die contact.
L_S	Internal Source Inductance	—	6.0	—		
C_{iss}	Input Capacitance	—	400	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	170	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	42	—		$f = 1.0\text{MHz}$, See Fig. 5



Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	2.7	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	22		
V_{SD}	Diode Forward Voltage	—	—	1.6	V	$T_J = 25^\circ\text{C}, I_S = 2.7A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	65	130	ns	$T_J = 25^\circ\text{C}, I_F = 10A$
Q_{rr}	Reverse Recovery Charge	—	0.33	0.65	μC	$di/dt = 100A/\mu\text{s}$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② $V_{DD}=25V$, starting $T_J = 25^\circ\text{C}$, $L = 16\text{mH}$
 $R_G = 25\Omega, I_{AS} = 2.7A$. (See Figure 12)

③ $I_{SD} \leq 10A, di/dt \leq 90A/\mu\text{s}, V_{DD} \leq V_{(BR)DSS}, T_J \leq 150^\circ\text{C}$

④ Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.

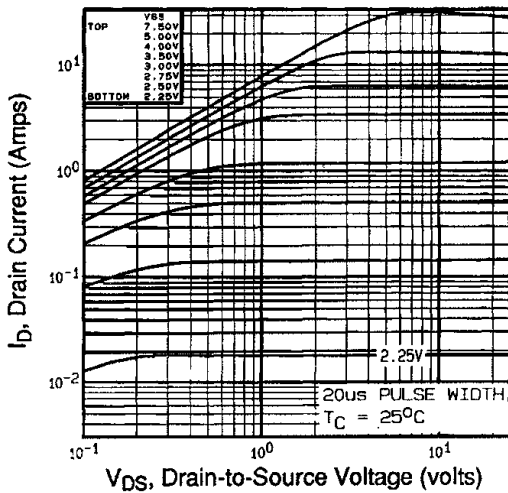


Fig 1. Typical Output Characteristics,
 $T_C=25^{\circ}\text{C}$

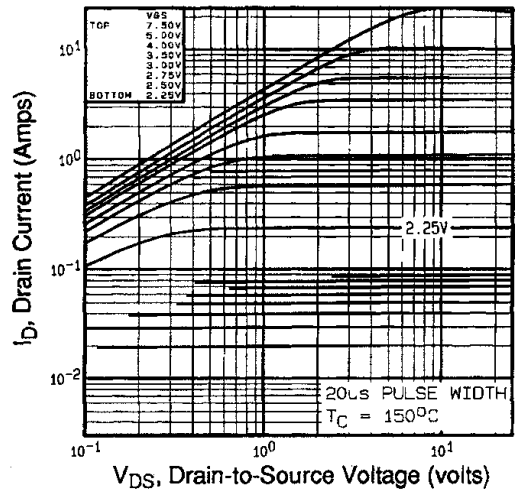


Fig 2. Typical Output Characteristics,
 $T_C=150^{\circ}\text{C}$

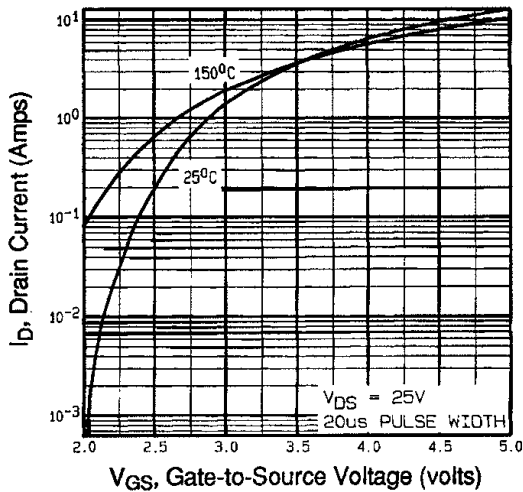


Fig 3. Typical Transfer Characteristics

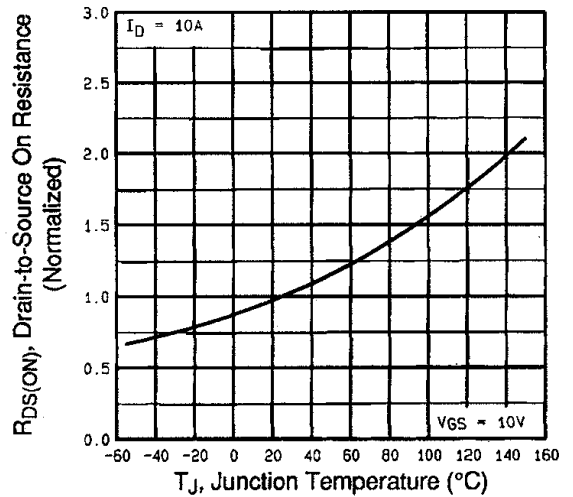


Fig 4. Normalized On-Resistance
Vs. Temperature

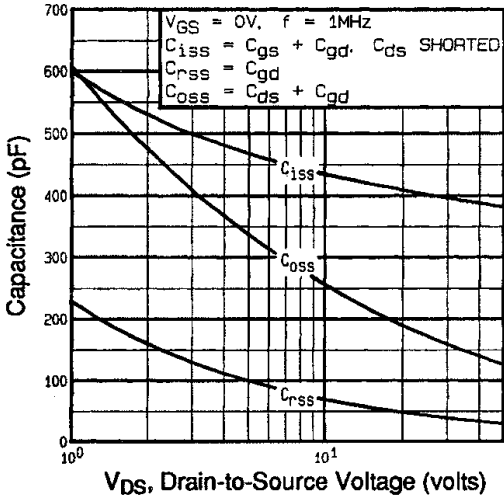


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

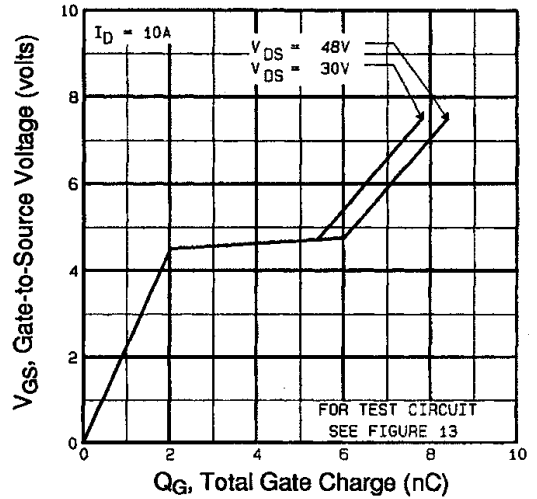


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

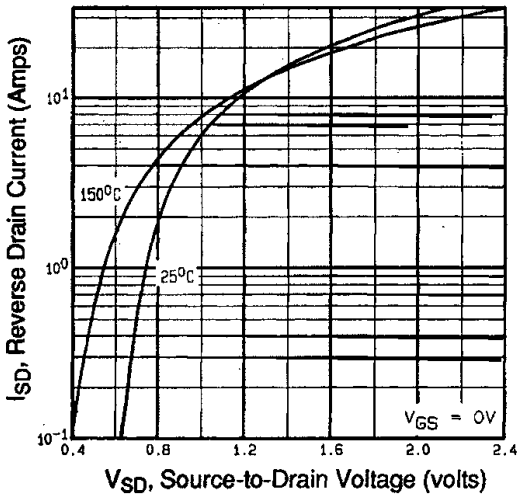


Fig 7. Typical Source-Drain Diode Forward Voltage

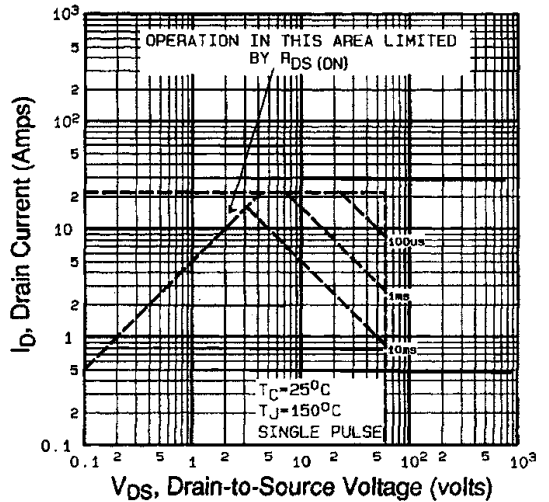


Fig 8. Maximum Safe Operating Area

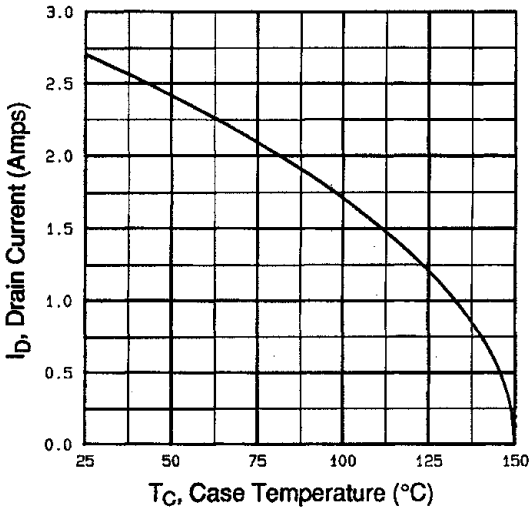


Fig 9. Maximum Drain Current Vs. Case Temperature

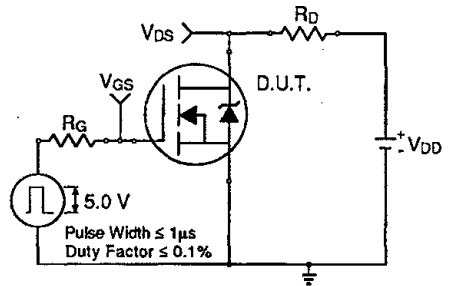


Fig 10a. Switching Time Test Circuit

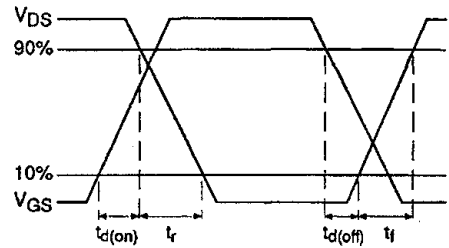


Fig 10b. Switching Time Waveforms

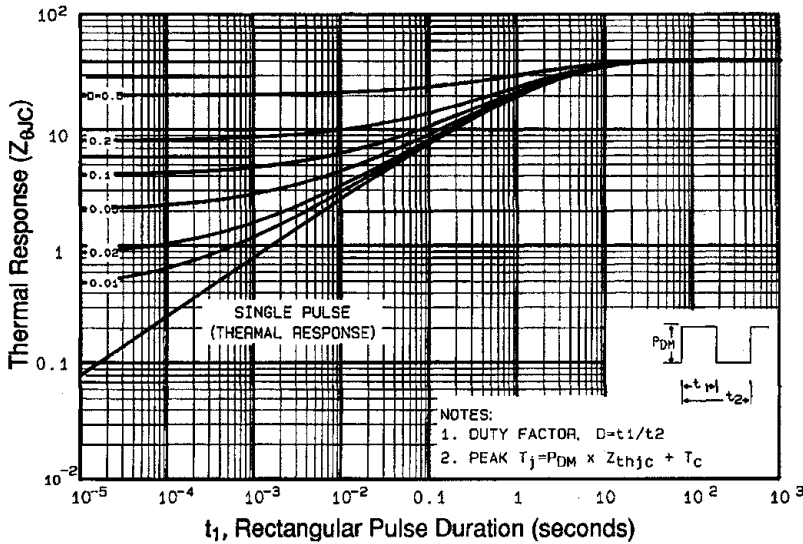


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

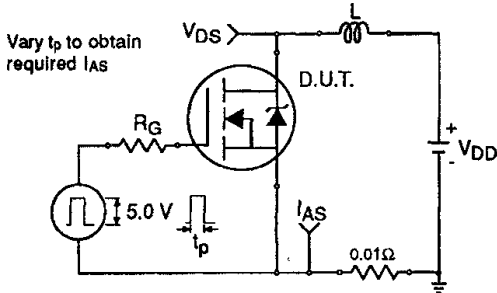


Fig 12a. Unclamped Inductive Test Circuit

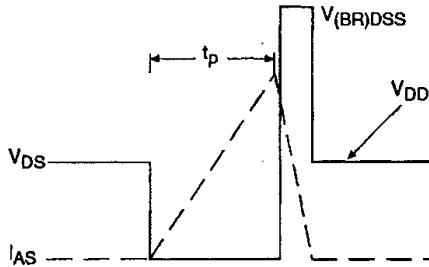


Fig 12b. Unclamped Inductive Waveforms

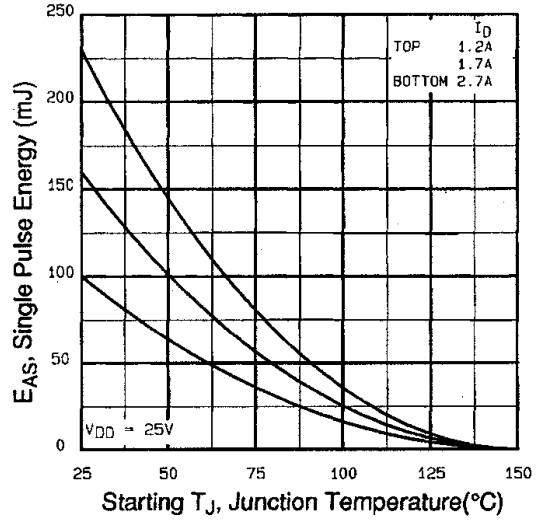


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

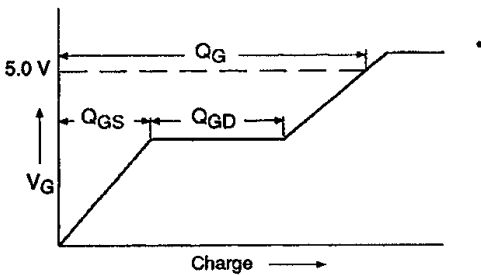


Fig 13a. Basic Gate Charge Waveform

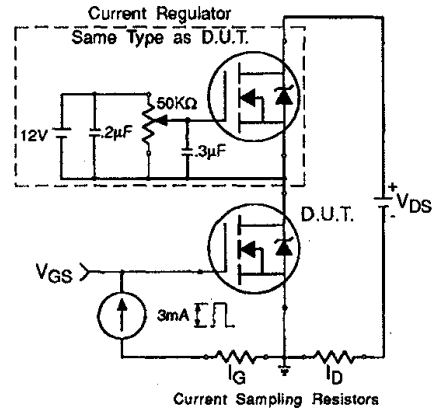
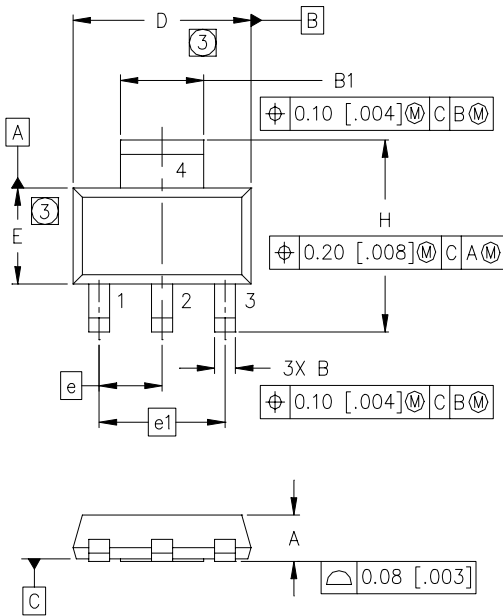
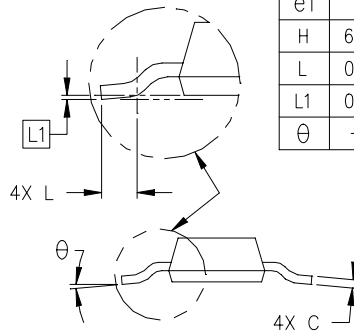


Fig 13b. Gate Charge Test Circuit

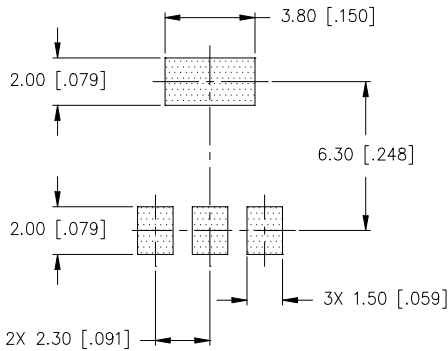
Package Outline SOT-223 (TO-261AA) Outline



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.55	1.80	.061	.071
B	0.65	0.85	.026	.033
B1	2.95	3.15	.116	.124
C	0.25	0.35	.010	.014
D	6.30	6.70	.248	.264
E	3.30	3.70	.130	.146
e	2.30	BSC	.0905	BSC
e1	4.60	BSC	.181	BSC
H	6.71	7.29	.264	.287
L	0.91	—	.036	—
L1	0.061	BSC	.0024	BSC
θ	—	10°	—	10°



MINIMUM RECOMMENDED FOOTPRINT



LEAD ASSIGNMENTS

- 1 = GATE
- 2 = DRAIN
- 3 = SOURCE
- 4 = DRAIN

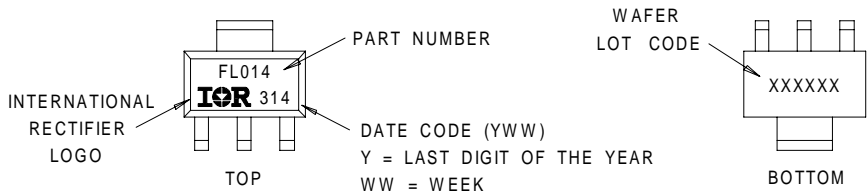
NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS DO NOT INCLUDE MOLD FLASH.
4. OUTLINE CONFORMS TO JEDEC OUTLINE TO-261AA.
5. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].

Part Marking Information

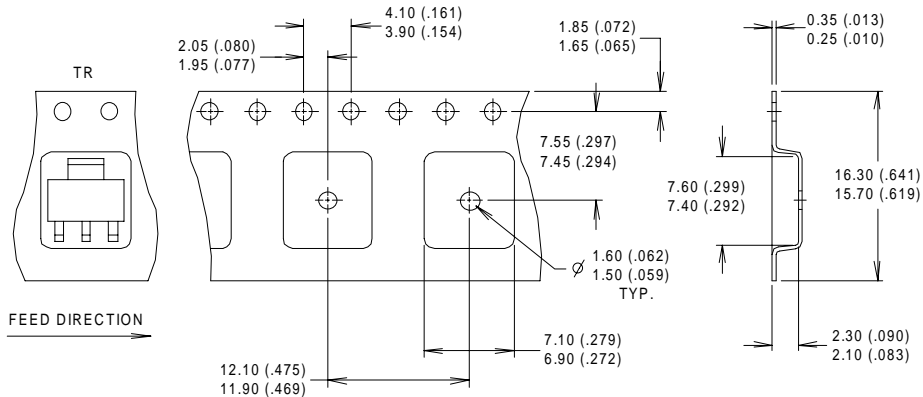
SOT-223

EXAMPLE : THIS IS AN IRFL014



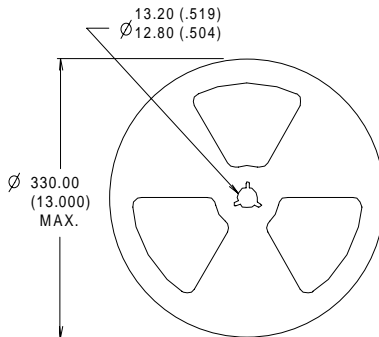
Tape & Reel Information

SOT-223 Outline



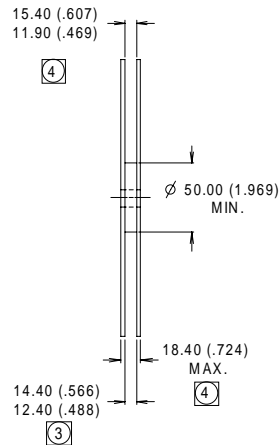
NOTES :

1. CONTROLLING DIMENSION: MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.
3. EACH Ø330.00 (13.00) REEL CONTAINS 2,500 DEVICES.



NOTES :

1. OUTLINE COMFORMS TO EIA-418-1.
2. CONTROLLING DIMENSION: MILLIMETER..
- ③ DIMENSION MEASURED @ HUB.
- ④ INCLUDES FLANGE DISTORTION @ OUTER EDGE.





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