IRU3038

SYNCHRONOUS PWM CONTROLLER FOR TERMINATION POWER SUPPLY APPLICATIONS

PRELIMINARY DATA SHEET

FEATURES

- Synchronous Controller in 14-Pin Package
- Operating with single 5V or 12V supply voltage
- 200KHz to 400KHz operation set by an external resistor
- Soft-Start Function
- Fixed Frequency Voltage Mode
- 500mA Peak Output Drive Capability
- Uncommitted Error Amplifier available for DDR voltage tracking application
- 1.25V Reference Voltage
- Protects the output when control FET is shorted

APPLICATIONS

- DDR memory source sink Vtt application
- Low cost on-board DC to DC such as 5V to 3.3V, 2.5V or 1.8V
- Graphic Card
- Hard Disk Drive

DESCRIPTION

The IRU3038 controller IC is designed to provide a low cost synchronous Buck regulator for voltage tracking applications such DDR memory and general purpose on-board DC to DC converter. Modern micro processors combined with DDR memory, need high-speed bandwidth data bus which requires a particular bus termination voltage. This voltage will be tightly regulated to track the half of chipset voltage for best performance. The IRU3038 together with dual N-channel MOSFETs such as IRF7313, provide a low cost solution for such applications. This device features a programmable frequency set from 200KHz to 400KHz, under-voltage lockout for both Vcc and Vc supplies, an external programmable soft-start function as well as output under-voltage detection that latches off the device when an output short is detected.

TYPICAL APPLICATION

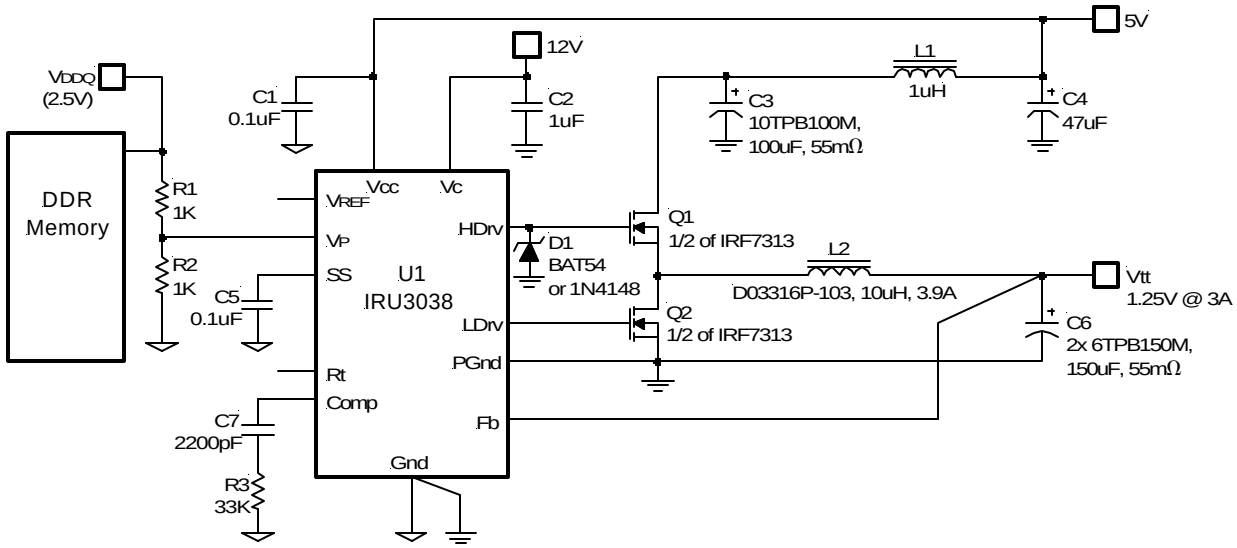


Figure 1 - Typical application of IRU3038 when Vtt tracks the V_{DDQ}.

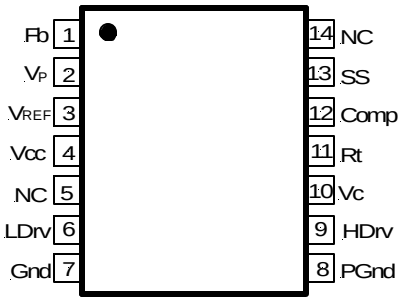
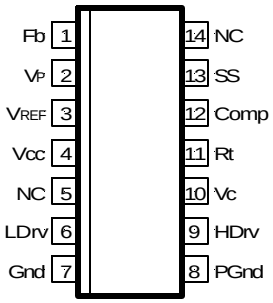
PACKAGE ORDER INFORMATION

T_A (°C)	DEVICE	PACKAGE
0 To 70	IRU3038CF	14-Pin Plastic TSSOP (F)
0 To 70	IRU3038CS	14-Pin Plastic SOIC NB (S)

ABSOLUTE MAXIMUM RATINGS

Vcc Supply Voltage 25V
Vc Supply Voltage ..... 30V (not rated for inductive load)
Storage Temperature Range ..... -65°C To 150°C
Operating Junction Temperature Range ..... 0°C To 125°C

PACKAGE INFORMATION

14-PIN PLASTIC TSSOP (F)	14-PIN PLASTIC SOIC (S)
	
θ_{JA}=100°C/W	θ_{JA}=88°C/W

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over Vcc=5V, Vc=12V and T_A=0 to 70°C. Typical values refer to T_A=25°C. Low duty cycle pulse testing is used which keeps junction and case temperatures equal to the ambient temperature.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Reference Voltage						
V_{REF} Voltage	V_{FB}		1.225	1.250	1.275	V
Fb Voltage Line Regulation	L_{REG}	5<Vcc<12		0.2	0.35	%
UVLO						
UVLO Threshold - Vcc	UVLO Vcc	Supply Ramping Up	4	4.2	4.4	V
UVLO Hysteresis - Vcc				0.25		V
UVLO Threshold - Vc	UVLO Vc	Supply Ramping Up	3.1	3.3	3.5	V
UVLO Hysteresis - Vc				0.2		V
UVLO Threshold - Fb	UVLO Fb	Fb Ramping Down	0.4	0.6	0.8	V
UVLO Hysteresis - Fb				0.1		V
Supply Current						
Vcc Dynamic Supply Current	Dyn Icc	Freq=200KHz, C_L=1500pF	2	5	8	mA
Vc Dynamic Supply Current	Dyn Ic	Freq=200KHz, C_L=1500pF	2	7	10	mA
Vcc Static Supply Current	I_{CCQ}	SS=0V	1	3.5	6	mA
Vc Static Supply Current	I_{CQ}	SS=0V	0.5	1	4.5	mA
Soft-Start Section						
Charge Current	SS_{IB}	SS=0V	-10	-20	-30	µA

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Error Amp						
Fb Voltage Input Bias Current	I_{FB1}	SS=3V, Fb=1V		-0.1		µA
Fb Voltage Input Bias Current	I_{FB2}	SS=0V, Fb=1V		-64		µA
V_P Voltage Range			0.8		1.5	V
Transconductance	gm		450	600	750	µmho
Oscillator						
Frequency	Freq	Rt=Open	180	200	220	KHz
		Rt=Gnd	360	400	440	
Ramp Amplitude	V_{RAMP}		1.225	1.25	1.275	V
Output Drivers						
Rise Time	T_r	C_{LOAD}=1500pF		50	100	ns
Fall Time	T_f	C_{LOAD}=1500pF		50	100	ns
Dead Band Time	T_{DB}		50	150	250	ns
Max Duty Cycle	T_{ON}	Fb=1V, Freq=200KHz	85	90	95	%
Min Duty Cycle	T_{OFF}	Fb=1.5V	0	0		%

PIN DESCRIPTIONS

PIN#	PIN SYMBOL	PIN DESCRIPTION
1	Fb	This pin is connected directly to the output of the switching regulator via resistor divider to provide feedback to the Error amplifier.
2	V_P	Non-inverting input of error amplifier.
3	V_{REF}	Reference Voltage.
4	Vcc	This pin provides biasing for the internal blocks of the IC as well as power for the low side driver. A minimum of 1µF, high frequency capacitor must be connected from this pin to ground to provide peak drive current capability.
5 14	NC	No Connection.
6	LDrv	Output driver for the synchronous power MOSFET.
7	Gnd	Analog ground for internal reference and control circuitry. Connect to PGnd with a short trace.
8	PGnd	This pin serves as the separate ground for MOSFET's drivers and should be connected to system's ground plane. A high frequency capacitor (0.1 to 1µF) must be connected from Vcc and Vc pins to this pin for noise free operation.
9	HDrv	Output driver for the high side power MOSFET. Connect a diode, such as BAT54 or 1N4148, from this pin to ground for the application when the inductor current goes negative (Source/ Sink), soft-start at no load and for the fast load transient from full load to no load.
10	Vc	This pin is connected to a voltage that must be at least 4V higher than the bus voltage of the switcher (assuming 5V threshold MOSFET) and powers the high side output driver. A minimum of 1µF, high frequency capacitor must be connected from this pin to ground to provide peak drive current capability.
11	Rt	The switching frequency can be Programmed between 200KHz and 400KHz by connecting a resistor between Rt and Gnd. Floating the pin set the switching frequency to 200KHz and grounding the pin set the switching frequency to 400KHz.
12	Comp	Compensation pin of the error amplifier. An external resistor and capacitor network is typically connected from this pin to ground to provide loop compensation.
13	SS	This pin provides soft-start for the switching regulator. An internal current source charges an external capacitor that is connected from this pin to ground which ramps up the output of the switching regulator, preventing it from overshooting as well as limiting the input current. The converter can be shutdown by pulling this pin below 0.5V.

BLOCK DIAGRAM

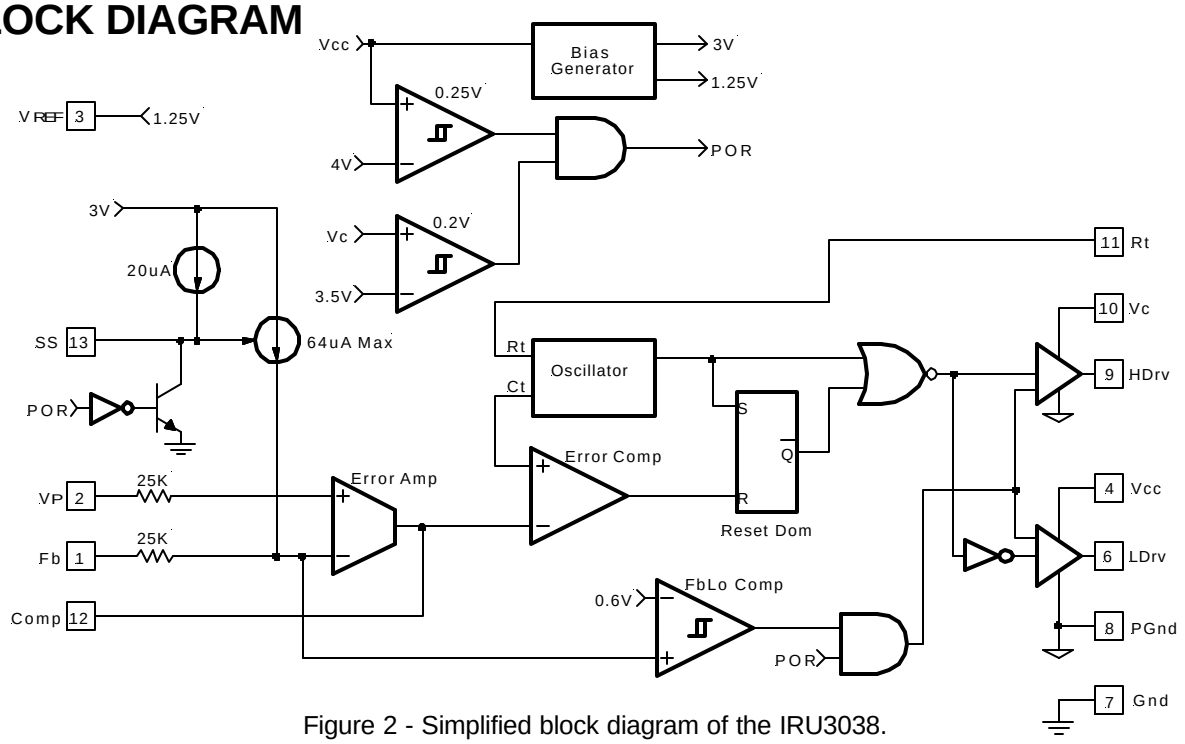


Figure 2 - Simplified block diagram of the IRU3038.

THEORY OF OPERATION

Introduction

The IRU3038 is a fixed frequency, voltage mode synchronous controller and consists of a precision reference voltage, an uncommitted error amplifier, an internal oscillator, a PWM comparator, 0.5A peak gate driver, soft-start and shutdown circuits (see Block Diagram).

The output voltage of the synchronous converter is set and controlled by the output of the error amplifier; this is the amplified error signal from the sensed output voltage and the voltage on non-inverting input of error amplifier(V_P). This voltage is compared to a fixed frequency linear sawtooth ramp and generates fixed frequency pulses of variable duty-cycle, which drives the two N-channel external MOSFETs.

The timing of the IC is provided through an internal oscillator circuit which uses on-chip capacitor. The oscillation frequency is programmable between 200 to 400KHz by using an external resistor. Figure 12 shows switching frequency vs. external resistor (Rt).

Soft-Start

The IRU3038 has a programmable soft-start to control the output voltage rise and limit the current surge at the start-up. To ensure correct start-up, the soft-start sequence initiates when the Vc and Vcc rise above their threshold (3.3V and 4.2V respectively) and generates the Power On Reset (POR) signal. Soft-start function operates by sourcing an internal current to charge an external capacitor to about 3V. Initially, the soft-start function clamps the E/A's output of the PWM converter. As the charging voltage of the external capacitor ramps up, the PWM signals increase from zero to the point the feedback loop takes control.

Short-Circuit Protection

The outputs are protected against the short-circuit. The IRU3038 protects the circuit for shorted output by sensing the output voltage (through the external resistor divider). The IRU3038 shuts down the PWM signals, when the output voltage drops below 0.6V.

The IRU3038 also protects the output from over-voltaging when the control FET is shorted. This is done by turning on the sync FET with the maximum duty cycle.

Under-Voltage Lockout

The under-voltage lockout circuit assures that the MOSFET driver outputs remain in the off state whenever the supply voltage drops below set parameters. Lockout occurs if Vc and Vcc fall below 3.3V and 4.2V respectively. Normal operation resumes once Vc and Vcc rise above the set values.

APPLICATION INFORMATION

Design Example:
The following example is a typical application for IRU3038, the schematic is Figure 11 on page 12.

V_{IN} = 5V
V_{OUT} = 2.5V
I_{OUT} = 8A
ΔV_{OUT} = 100mV
f_S = 200KHz

Output Voltage Programming
Output voltage is programmed by reference voltage and external voltage divider. The Fb pin is the inverting input of the error amplifier, which is referenced to the voltage on non-inverting pin of error amplifier. For this application, this pin (V_P) is connected to reference voltage (V_{REF}). The output voltage is defined by using the following equation:

$$V_{OUT} = V_P \times \left(1 + \frac{R_6}{R_5}\right) \qquad ---(1)$$

$V_P = V_{REF}$ = 1.25V

When an external resistor divider is connected to the output as shown in Figure 3.

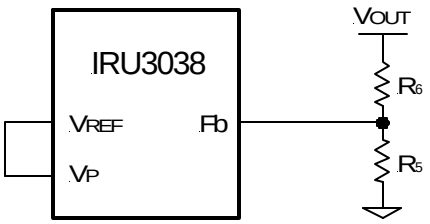


Figure 3 - Typical application of the IRU3038 for programming the output voltage.

Equation (1) can be rewritten as:

$$R_6 = R_5 \times \left(\frac{V_{OUT}}{V_P} - 1\right)$$

Choose R_5 = 1KΩ
This will result to R_6 = 1KΩ

If the high value feedback resistors are used, the input bias current of the Fb pin could cause a slight increase in output voltage. The output voltage set point can be more accurate by using precision resistor.

Soft-Start Programming
The soft-start timing can be programmed by selecting the soft-start capacitance value. The start-up time of the converter can be calculated by using:

$$t_{START} = 75 \times Css \quad (ms) \qquad ---(2)$$

Where C_{SS} is the soft-start capacitor (μF)

For a start-up time of 7.5ms, the soft-start capacitor will be 0.1μF. Choose a ceramic capacitor at 0.1μF.

Shutdown
The converter can be shutdown by pulling the soft-start pin below 0.5V. The control MOSFET turns off and the synchronous MOSFET turns on during shutdown.

Boost Supply Vc
To drive the high-side switch it is necessary to supply a gate voltage at least 4V greater than the bus voltage. This is achieved by using a charge pump configuration as shown in Figure 11. The capacitor is charged up to approximately twice the bus voltage. A capacitor in the range of 0.1μF to 1μF is generally adequate for most applications. In application, when a separate voltage source is available the boost circuit can be avoided as shown in Figure 1.

Input Capacitor Selection
The input filter capacitor should be based on how much ripple the supply can tolerate on the DC input line. The ripple current generated during the on time of control MOSFET should be provided by input capacitor. The RMS value of this ripple is expressed by:

$$I_{RMS} = I_{OUT}\sqrt{D \times (1\text{-}D)} \qquad ---(3)$$

Where:
D is the Duty Cycle, $D=V_{OUT}/V_{IN}$.
I_{RMS} is the RMS value of the input capacitor current.
I_{OUT} is the output current for each channel.

For V_{IN}=5V, I_{OUT}=8A and D=0.5, the I_{RMS}=4A

For higher efficiency, a low ESR capacitor is recommended. Choose two Poscap from Sanyo 10TPB100ML (10V, 100μF, 55mΩ) with a maximum allowable ripple current of 1.9A.

Output Capacitor Selection

The criteria to select the output capacitor is normally based on the value of the Effective Series Resistance (ESR). In general, the output capacitor must have low enough ESR to meet output ripple and load transient requirements, yet have high enough ESR to satisfy stability requirements. The ESR of the output capacitor is calculated by the following relationship:

$$ESR \leq \frac{\Delta V_O}{\Delta I_O} \qquad ---(4)$$

Where:
ΔV_O = Output Voltage Ripple
ΔI_O = Output Current
ΔV_O=100mV and ΔI_O=4A
This results to: ESR=25mΩ

The Sanyo TPC series, Poscap capacitor is a good choice. The 6TPC150M 150μF, 6.3V has an ESR 40mΩ. Selecting two of these capacitors in parallel, results to an ESR of $\cong$ 20mΩ which achieves our low ESR goal.

The capacitor value must be high enough to absorb the inductor's ripple current. The larger the value of capacitor, the lower will be the output ripple voltage.

Inductor Selection

The inductor is selected based on output power, operating frequency and efficiency requirements. Low inductor value causes large ripple current, resulting in the smaller size, but poor efficiency and high output noise. Generally, the selection of inductor value can be reduced to desired maximum ripple current in the inductor (Δi). The optimum point is usually found between 20% and 50% ripple of the output current.

For the buck converter, the inductor value for desired operating ripple current can be determined using the following relation:

$$V_{IN} - V_{OUT} = L \times \frac{\Delta i}{\Delta t} \; ; \; \Delta t = D \times \frac{1}{f_S} \; ; \; D = \frac{V_{OUT}}{V_{IN}}$$

$$L = (V_{IN} - V_{OUT}) \times \frac{V_{OUT}}{V_{IN} \times \Delta i \times f_S} \qquad ---(5)$$

Where:
V_{IN} = Maximum Input Voltage
V_{OUT} = Output Voltage
Δi = Inductor Ripple Current
f_S = Switching Frequency
Δt = Turn On Time
D = Duty Cycle

If $\Delta i = 30\%(I_O)$, then the output inductor will be:

$L = 2.6\mu H$

The Coilcraft DO5022HC series provides a range of inductors in different values, low profile suitable for large currents, 3.3μH, 10A is a good choice for this application. This will result to a ripple approximately 26.5% of output current.

Power MOSFET Selection

The IRU3038 uses two N-Channel MOSFETs. The selections criteria to meet power transfer requirements is based on maximum drain-source voltage (V_{DSS}), gate-source drive voltage (V_{GS}), maximum output current, On-resistance $R_{DS(ON)}$ and thermal management.

The MOSFET must have a maximum operating voltage (V_{DSS}) exceeding the maximum input voltage (V_{IN}).

The gate drive requirement is almost the same for both MOSFETs. Logic-level transistor can be used and caution should be taken with devices at very low V_{GS} to prevent undesired turn-on of the complementary MOSFET, which results a shoot-through current.

The total power dissipation for MOSFETs includes conduction and switching losses. For the Buck converter, the average inductor current is equal to the DC load current. The conduction loss is defined as:

$$P_{COND} \text{ (Upper Switch)} = I_{LOAD}^2 \times R_{DS(ON)} \times D \times \vartheta$$

$$P_{COND} \text{ (Lower Switch)} = I_{LOAD}^2 \times R_{DS(ON)} \times (1 - D) \times \vartheta$$

$\vartheta = R_{DS(ON)}$ Temperature Dependency

The $R_{DS(ON)}$ temperature dependency should be considered for the worst case operation. This is typically given in the MOSFET data sheet. Ensure that the conduction losses and switching losses do not exceed the package ratings or violate the overall thermal budget.

Choose IRF7460 for both control MOSFET and synchronous MOSFET. This device provides low on-resistance in a compact SOIC 8-Pin package.

The MOSFET has the following data:

IRF7460
V_{DSS} = 20V
I_D = 10A @ 75°C
$R_{DS(ON)}$ = 10mΩ @ V_{GS}=10V
ϑ = 1.8 for 150°C (Junction Temperature)

The total conduction losses will be:

$P_{CON(TOTAL)}$ = 1.152W

The switching loss is more difficult to calculate, even though the switching transition is well understood. The reason is the effect of the parasitic components and switching times during the switching procedures such as turn-on / turnoff delays and rise and fall times. With a linear approximation, the total switching loss can be expressed as:

$$P_{SW} = \frac{V_{DS(OFF)}}{2} \times \frac{t_r + t_f}{T} \times I_{LOAD} \qquad ---(6)$$

Where:
$V_{DS(OFF)}$ = Drain to Source Voltage at off time
t_r = Rise Time
t_f = Fall Time
T = Switching Period
I_{LOAD} = Load Current

The switching time waveform is shown in Figure 4.

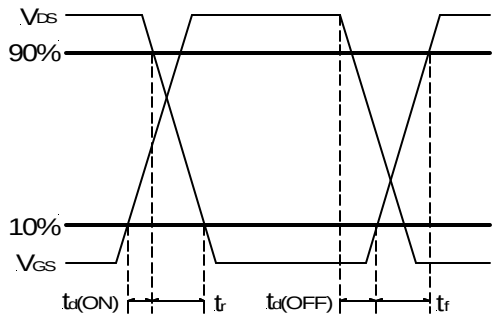


Figure 4 - Switching time waveforms.

From IRF7460 data sheet we obtain:

t_r = 6.9ns
t_f = 4.3ns

These values are taken under a certain condition test. For more detail please refer to the IRF7460 data sheet.

By using equation (6), we can calculate the total switching losses.

$P_{SW(TOTAL)}$ = 44.8mW

Feedback Compensation

The IRU3038 is a voltage mode controller; the control loop is a single voltage feedback path including error amplifier and error comparator. To achieve fast transient response and accurate output regulation, a compensation circuit is necessary. The goal of the compensation network is to provide a closed loop transfer function with the highest 0dB crossing frequency and adequate phase margin (greater than 45°).

The output LC filter introduces a double pole, –40dB/decade gain slope above its corner resonant frequency, and a total phase lag of 180° (see Figure 5). The Resonant frequency of the LC filter is expressed as follows:

$$F_{LC} = \frac{1}{2\pi \times \sqrt{L_O \times C_O}} \qquad ---(7)$$

Figure 5 shows gain and phase of the LC filter. Since we already have 180° phase shift just from the output filter, the system risks being unstable.

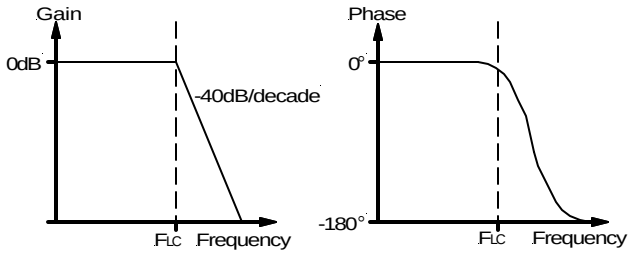


Figure 5 - Gain and phase of LC filter.

The IRU3038's error amplifier is a differential-input transconductance amplifier. The output is available for DC gain control or AC phase compensation.

The E/A can be compensated with or without the use of local feedback. When operated without local feedback, the transconductance properties of the E/A become evident and can be used to cancel one of the output filter poles. This will be accomplished with a series RC circuit from Comp pin to ground as shown in Figure 6.

Note that this method requires that the output capacitor should have enough ESR to satisfy stability requirements. In general, the output capacitor's ESR generates a zero typically at 5KHz to 50KHz which is essential for an acceptable phase margin.

The ESR zero of the output capacitor expressed as follows:

$$F_{ESR} = \frac{1}{2\pi \times ESR \times Co} \qquad ---(8)$$

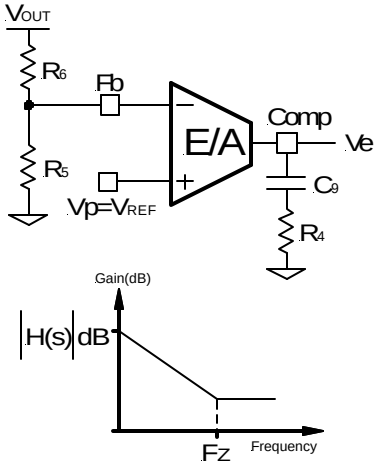


Figure 6 - Compensation network without local feedback and its asymptotic gain plot.

The transfer function (Ve / V_{OUT}) is given by:

$$H(s) = \left(g_m \times \frac{R_5}{R_6 + R_5}\right) \times \frac{1 + sR_4C_9}{sC_9} \qquad ---(9)$$

The (s) indicates that the transfer function varies as a function of frequency. This configuration introduces a gain and zero, expressed by:

$$|H(s)| = g_m \times \frac{R_5}{R_6 \times R_5} \times R_4 \qquad ---(10)$$

$$F_Z = \frac{1}{2\pi \times R_4 \times C_9} \qquad ---(11)$$

The gain is determined by the voltage divider and E/A's transconductance gain.

First select the desired zero-crossover frequency (Fo):

$Fo > F_{ESR}$ and $Fo \leq (1/5 \sim 1/10) \times f_S$

Use the following equation to calculate R_4:

$$R_4 = \frac{V_{OSC}}{V_{IN}} \times \frac{Fo \times F_{ESR}}{F_{LC}^2} \times \frac{R_5 + R_6}{R_5} \times \frac{1}{g_m} \qquad ---(12)$$

Where:
V_{IN} = Maximum Input Voltage
V_{OSC} = Oscillator Ramp Voltage
Fo = Crossover Frequency
F_{ESR} = Zero Frequency of the Output Capacitor
F_{LC} = Resonant Frequency of the Output Filter
R_5 and R_6 = Resistor Dividers for Output Voltage Programming
g_m = Error Amplifier Transconductance

For:
V_{IN} = 5V
V_{OSC} = 1.25V
Fo = 30KHz
F_{ESR} = 26.5KHz
F_{LC} = 5KHz
R_5 = 1K
R_6 = 1K
g_m = 600µmho

This results to R_4=26.52KΩ. Choose R_4=26.1KΩ

To cancel one of the LC filter poles, place the zero before the LC filter resonant frequency pole:

$F_Z \cong 75\% F_{LC}$

$$F_Z \cong 0.75 \times \frac{1}{2\pi\sqrt{L_O \times C_O}} \qquad ---(13)$$

For:
Lo = 10µH
Co = 300µF
F_Z = 3.8KHz
R_4 = 26.1KΩ

Using equations (11) and (13) to calculate C_9, we get:

$C_9 \cong$ 1800pF

One more capacitor is sometimes added in parallel with C_9 and R_4. This introduces one more pole which is mainly used to suppress the switching noise. The additional pole is given by:

$$F_P = \frac{1}{2\pi \times R_4 \times \frac{C_9 \times C_{POLE}}{C_9 + C_{POLE}}}$$

The pole sets to one half of switching frequency which results in the capacitor C_{POLE}:

$$C_{POLE} = \frac{1}{\pi \times R_4 \times f_S - \frac{1}{C_9}} \cong \frac{1}{\pi \times R_4 \times f_S}$$

for $F_P << \frac{f_S}{2}$

For a general solution for unconditionally stability for ceramic capacitor with very low ESR and any type of output capacitors, in a wide range of ESR values we should implement local feedback with a compensation network. The typically used compensation network for voltage-mode controller is shown in Figure 7.

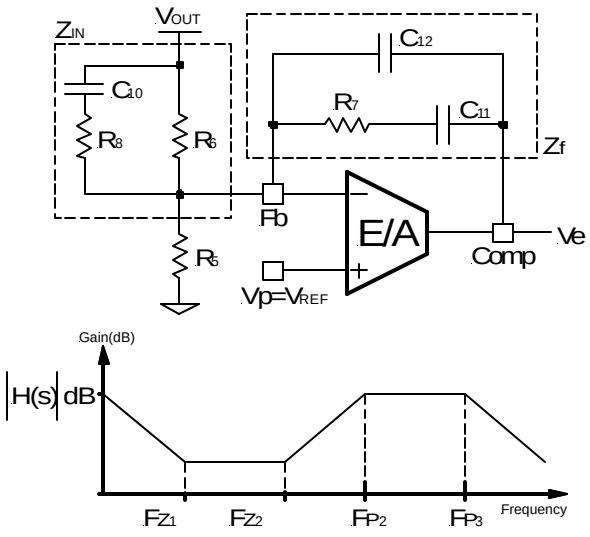


Figure 7 - Compensation network with local feedback and its asymptotic gain plot.

In such configuration, the transfer function is given by:

$$\frac{Ve}{V_{OUT}} = \frac{1 - g_m Z_f}{1 + g_m Z_{IN}}$$

The error amplifier gain is independent of the transconductance under the following condition:

$$g_m Z_f >> 1 \quad \text{and} \quad g_m Z_{IN} >> 1 \qquad \text{---(14)}$$

By replacing Z_{IN} and Z_f according to Figure 7, the transformer function can be expressed as:

$$H(s) = \frac{1}{sR_6(C_{12}+C_{11})} \times \frac{(1+sR_7C_{11}) \times [1+sC_{10}(R_6+R_8)]}{\left[1+sR_7\left(\frac{C_{12}C_{11}}{C_{12}+C_{11}}\right)\right] \times (1+sR_8C_{10})}$$

As known, transconductance amplifier has high impedance (current source) output, therefore, consider should be taken when loading the E/A output. It may exceed its source/sink output current capability, so that the amplifier will not be able to swing its output voltage over the necessary range.

The compensation network has three poles and two zeros and they are expressed as follows:

$$F_{P1} = 0$$

$$F_{P2} = \frac{1}{2\pi \times R_8 \times C_{10}}$$

$$F_{P3} = \frac{1}{2\pi \times R_7 \times \left(\frac{C_{12} \times C_{11}}{C_{12}+C_{11}}\right)} \cong \frac{1}{2\pi \times R_7 \times C_{12}}$$

$$F_{Z1} = \frac{1}{2\pi \times R_7 \times C_{11}}$$

$$F_{Z2} = \frac{1}{2\pi \times C_{10} \times (R_6 + R_8)} \cong \frac{1}{2\pi \times C_{10} \times R_6}$$

Cross Over Frequency:

$$F_O = R_7 \times C_{10} \times \frac{V_{IN}}{V_{OSC}} \times \frac{1}{2\pi \times Lo \times Co} \qquad \text{---(15)}$$

Where:
V_{IN} = Maximum Input Voltage
V_{OSC} = Oscillator Ramp Voltage
Lo = Output Inductor
Co = Total Output Capacitors

The stability requirement will be satisfied by placing the poles and zeros of the compensation network according to following design rules. The consideration has been taken to satisfy condition (14) regarding transconductance error amplifier.

1) Select the crossover frequency:
$F_O < F_{ESR}$ and $F_O \leq (1/10 \sim 1/6) \times f_S$

2) Select R_7, so that $R_7 >> \frac{2}{g_m}$

3) Place first zero before LC's resonant frequency pole.
$F_{Z1} \cong 75\% F_{LC}$

$$C_{11} = \frac{1}{2\pi \times F_{Z1} \times R_7}$$

4) Place third pole at the half of the switching frequency.

$$F_{P3} = \frac{f_S}{2}$$

$$C_{12} = \frac{1}{2\pi \times R_7 \times F_{P3}}$$

$C_{12} > 50pF$
If not, change R_7 selection.

5) Place R_7 in equation (15) and calculate C_{10}:

$$C_{10} \leq \frac{2\pi \times Lo \times F_O \times Co}{R_7} \times \frac{V_{OSC}}{V_{IN}}$$

6) Place second pole at the ESR zero.

$F_{P2} = F_{ESR}$

$$R_8 = \frac{1}{2\pi \times C_{10} \times F_{P2}}$$

Check if $R_8 > \frac{1}{gm}$

If R_8 is too small, increase R_7 and start from step 2.

7) Place second zero around the resonant frequency.

$F_{Z2} = F_{LC}$

$$R_6 = \frac{1}{2\pi \times C_{10} \times F_{Z2}} - R_8$$

8) Use equation (1) to calculate R_5:

$$R_5 = \frac{V_{REF}}{V_{OUT} - V_{REF}} \times R_6$$

These design rules will give a crossover frequency approximately one-tenth of the switching frequency. The higher the band width, the potentially faster the load transient speed. The gain margin will be large enough to provide high DC-regulation accuracy (typically -5dB to -12dB). The phase margin should be greater than 45° for overall stability.

IC Quiescent Power Dissipation

Power dissipation for IC controller is a function of applied voltage, gate driver loads and switching frequency. The IC's maximum power dissipation occurs when the IC operating with single 12V supply voltage (Vcc=12V and Vc≅24V) at 400KHz switching frequency and maximum gate loads.

This IC's power dissipation results to an excessive temperature rise and should be considered when using IRU3038 for such an application.

Layout Consideration

The layout is very important when designing high frequency switching converters. Layout will affect noise pickup and can cause a good design to perform with less than expected results.

Start to place the power components. Make all the connections in the top layer with wide, copper filled areas. The inductor, output capacitor and the MOSFET should be close to each other as possible. This helps to reduce the EMI radiated by the power traces due to the high switching currents through them. Place input capacitor directly to the drain of the high-side MOSFET. To reduce the ESR, replace the single input capacitor with two parallel units. The feedback part of the system should be kept away from the inductor and other noise sources and be placed close to the IC. In multilayer PCB, use one layer as power ground plane and have a separate control circuit ground (analog ground), to which all signals are referenced. The goal is to localize the high current path to a separate loop that does not interfere with the more sensitive analog control function. These two grounds must be connected together on the PC board layout at a single point.

TYPICAL PERFORMANCE CHARACTERISTICS

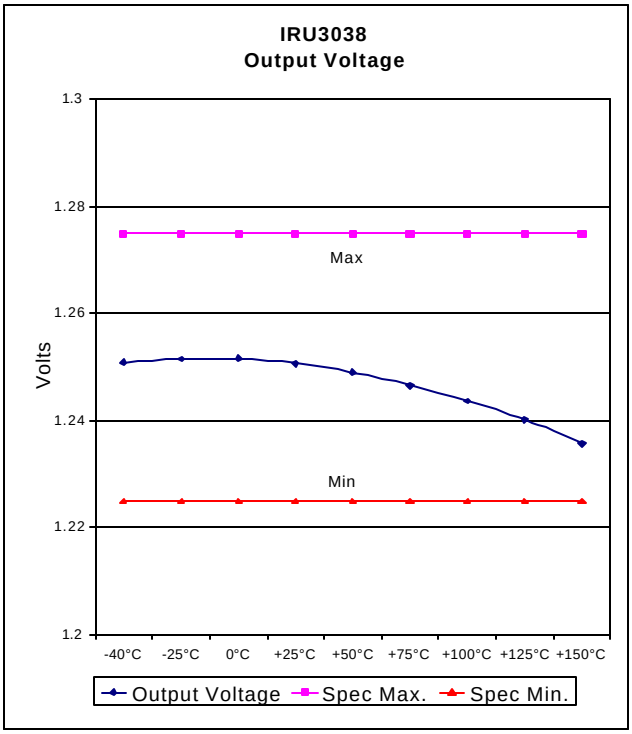


Figure 8 - Output voltage of IRU3038.

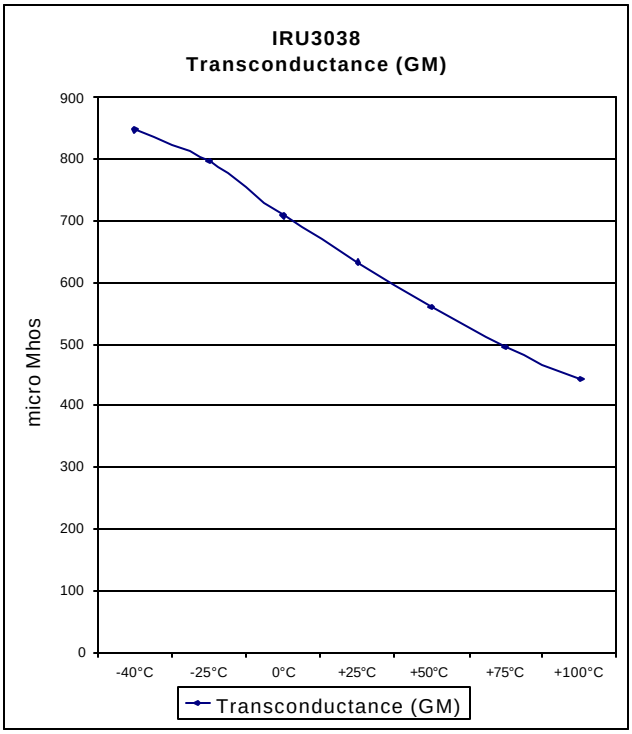


Figure 9 - Transconductance of IRU3038.

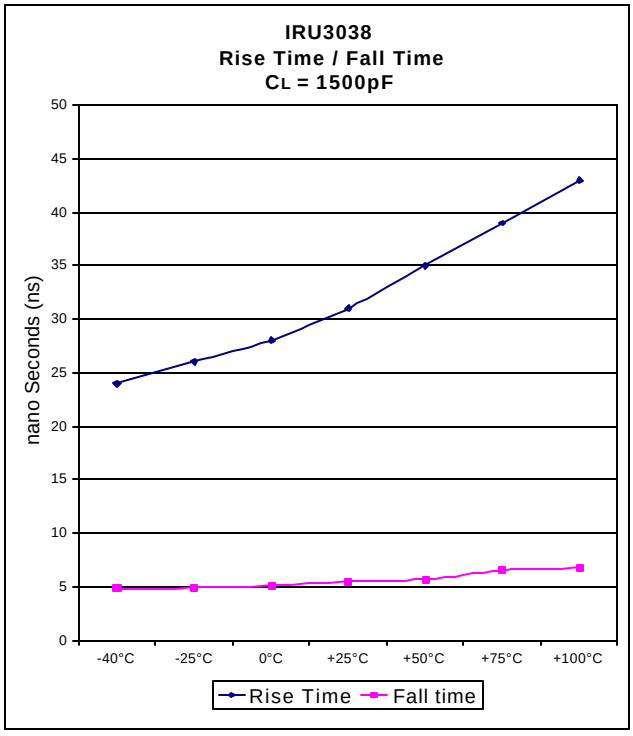


Figure 10 - Rise and fall time of IRU3038.

TYPICAL APPLICATION

Single Supply 5V Input

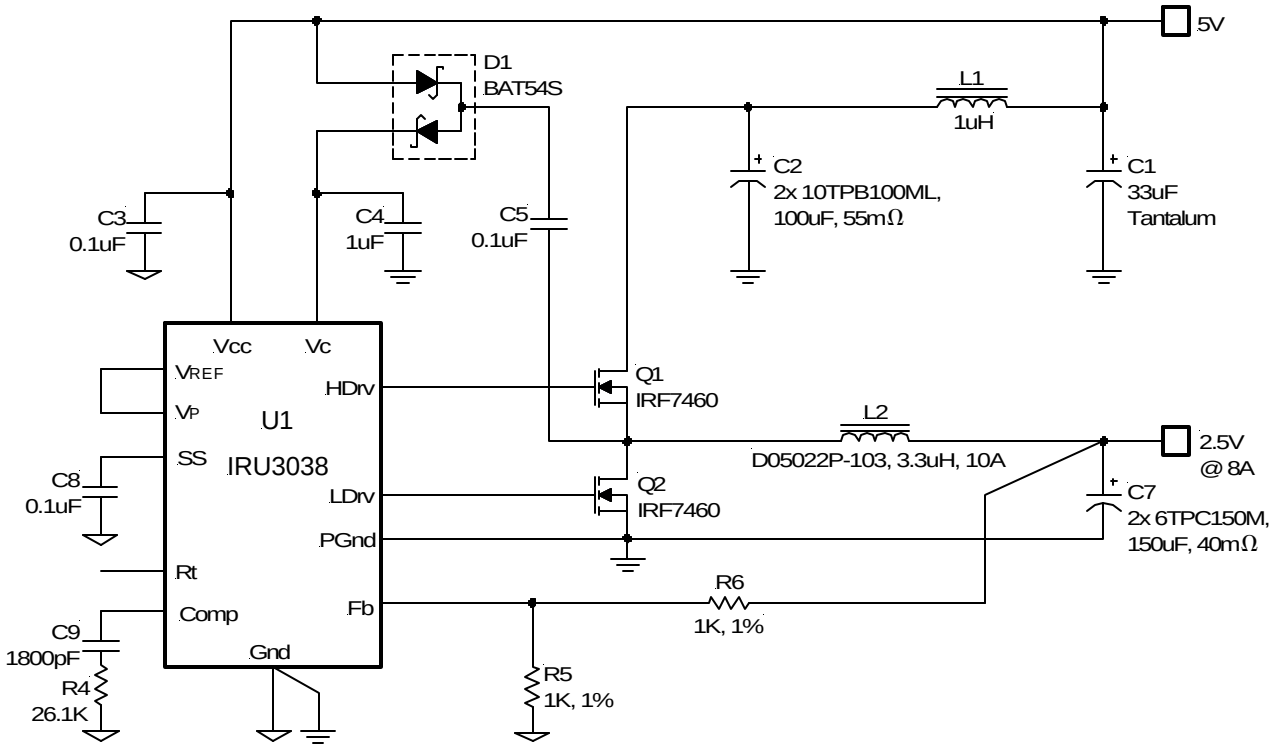


Figure 11 - Typical application of IRU3038 in an on-board DC-DC converter using a single 5V supply.

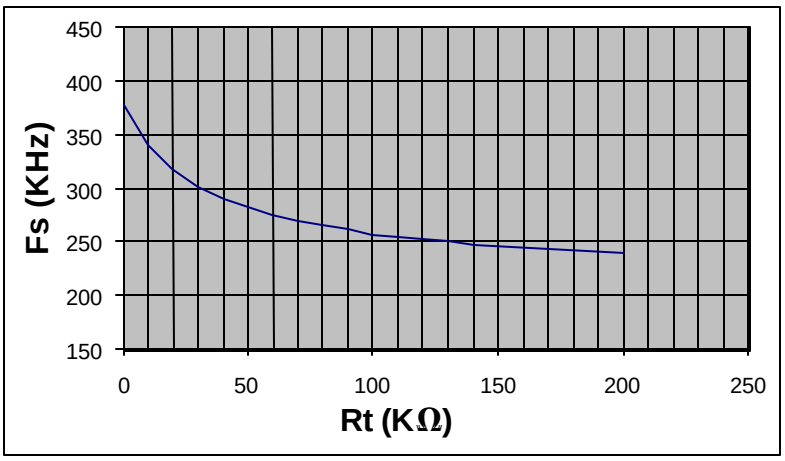


Figure 12 - Switching frequency vs. Rt.

TYPICAL APPLICATION

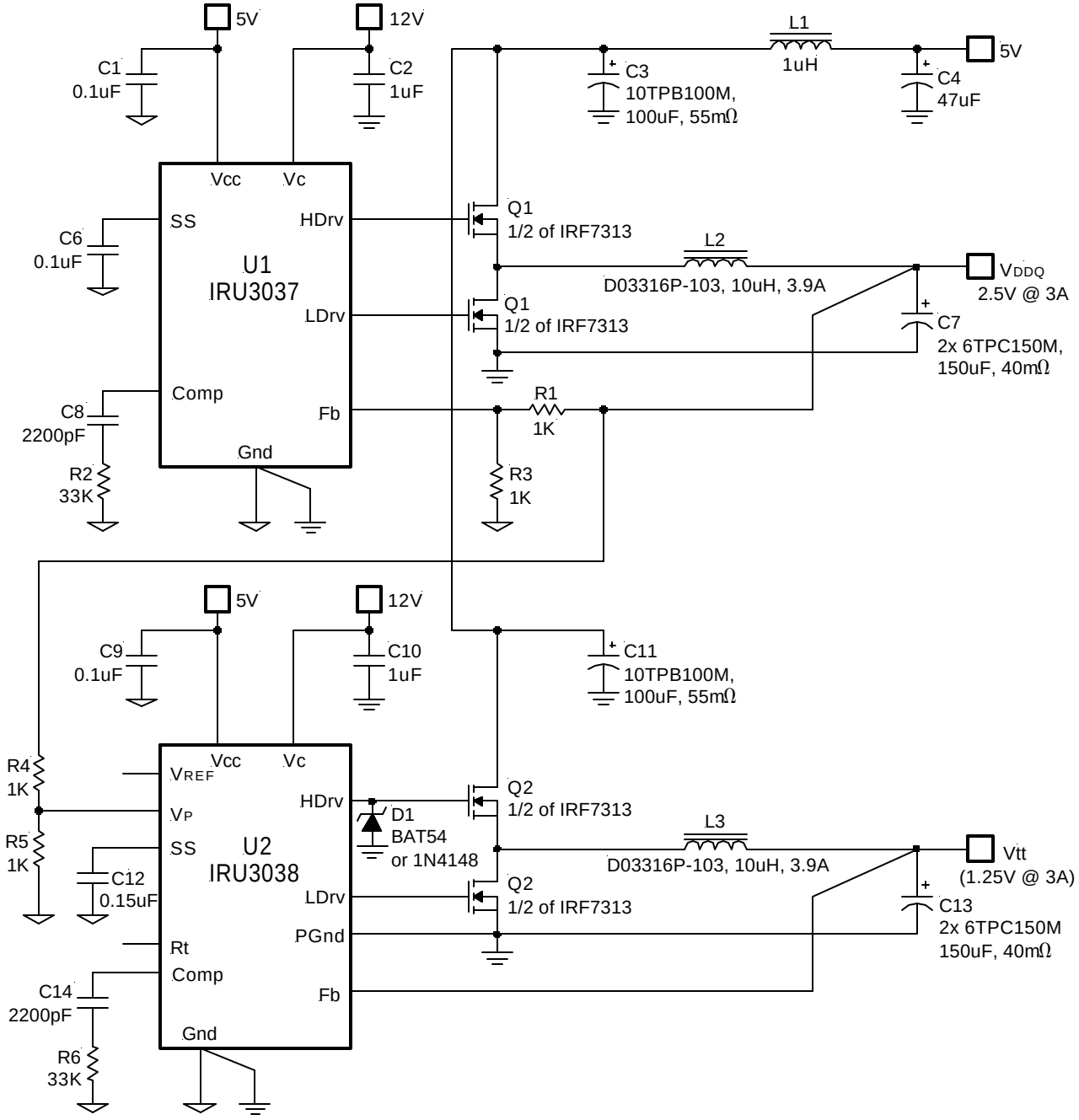


Figure 13 - Typical application of IRU3038 for DDR memory when the termination voltage tracks the core voltage generated by IRU3037.

DEMO-BOARD APPLICATION

5V to 2.5V @ 8A

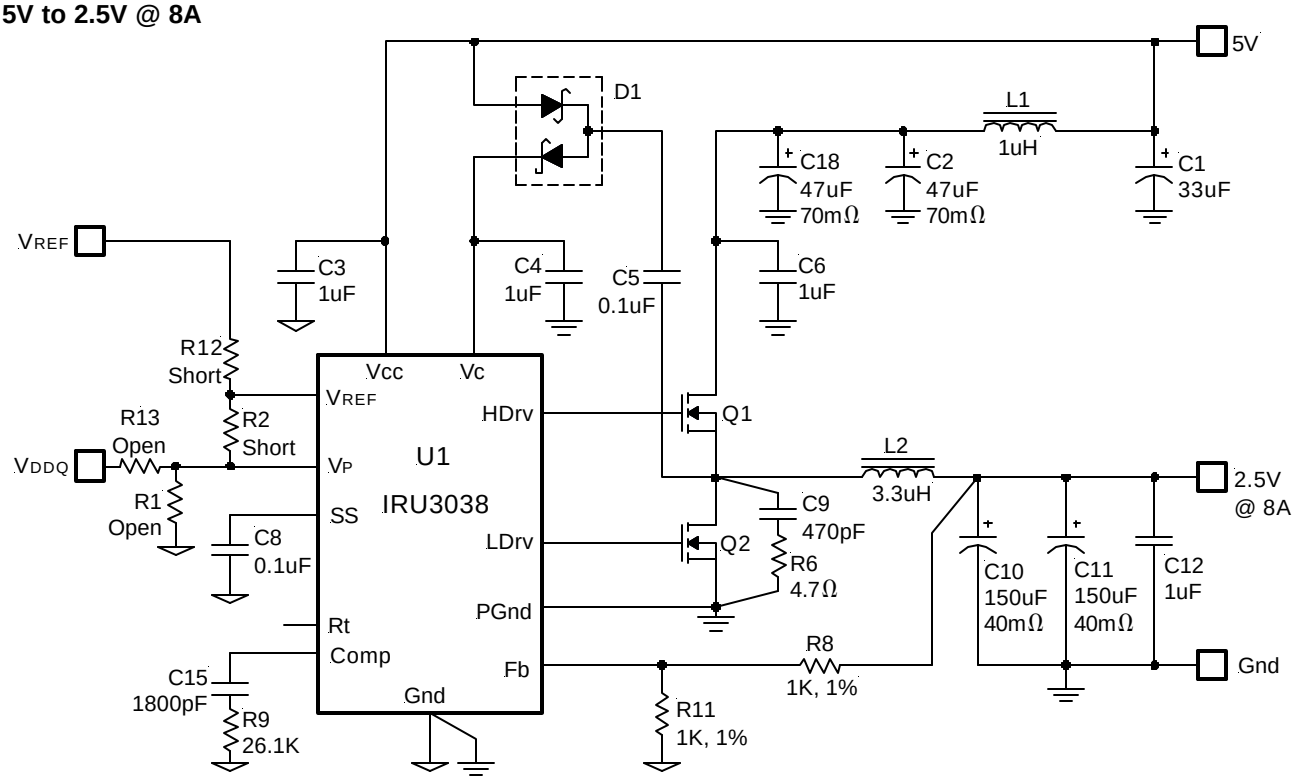


Figure 14 - Demo-board application of IRU3038.

Application Parts List

Ref Desig	Description	Value	Qty	Part#	Manuf	Web site (www.)
Q1, Q2	MOSFET	20V, 10mΩ, 12A	2	IRF7460	IR	irf.com
U1	Controller	Synchronous PWM	1	IRU3038	IR	
D1	Diode	Fast Switching, Schottky	1	BAT54S	IR	
L1	Inductor	1µH, 10A	1	D03316P-102HC	Coilcraft	coilcraft.com
L2	Inductor	3.3µH, 12A	1	D05022P-332HC	Coilcraft	
C1	Cap, Tantalum	33µF, 16V	1	ECS-T1CD336R	Panasonic	maco.panasonic.co.jp
C2,C18	Cap, Poscap	47µF, 16V, 70mΩ	2	16TPB47M	Sanyo	sanyo.com/industrial
C10,C11	Cap, Poscap	150µF, 6.3V, 40mΩ	2	6TPC150M	Sanyo	
C5,C8	Cap, Ceramic	0.1µF, Y5V, 25V	2	ECJ-2VF1E104Z	Panasonic	maco.panasonic.co.jp
C4	Cap, Ceramic	1µF, X7R, 25V	1	ECJ-3YB1E105K	Panasonic	
C15	Cap, Ceramic	1800pF, X7R, 50V	1	ECJ-2VB1H182K	Panasonic	
C9	Cap, Ceramic	470pF, X7R	1	ECJ-2VB2D471K	Panasonic	
C3,C6,C12	Cap, Ceramic	1µF, Y5V, 16V	3	ECJ-2VF1C105Z	Panasonic	
R9	Resistor	26.1K, 5%	1			
R6	Resistor	4.7Ω, 5%	1			
R8,R11	Resistor	1K, 1%	2			

TYPICAL PERFORMANCE CHARACTERISTICS

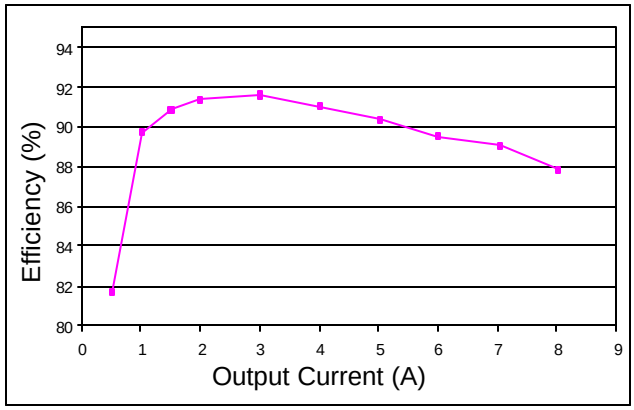


Figure 15 - Efficiency for IRU3038 Evaluation Board. V_{IN}=5V, V_{OUT}=2.5V

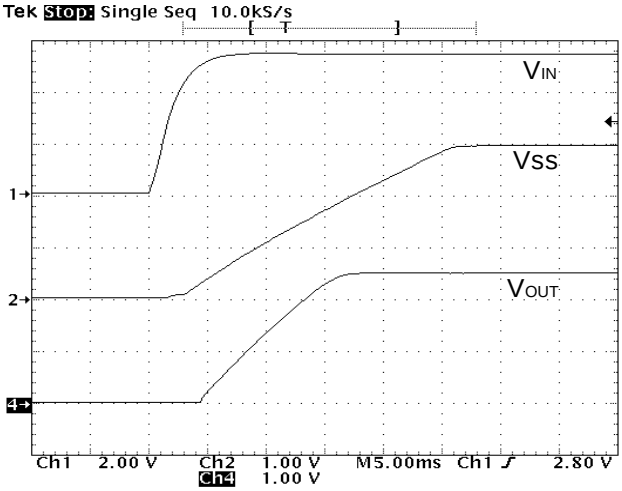


Figure 16 - Start-up time @ I_{OUT}=5A.

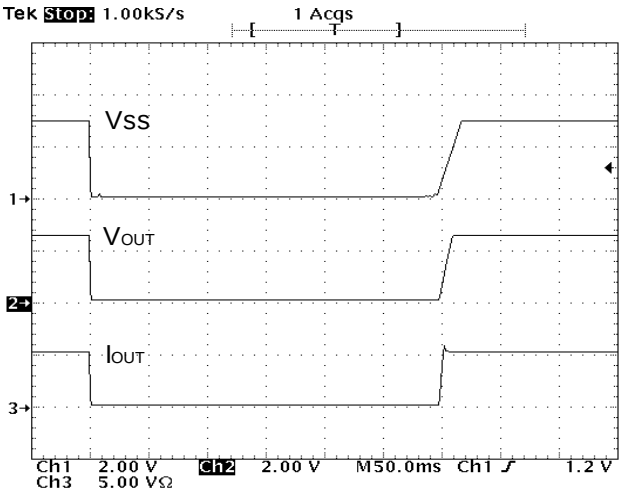


Figure 17 - Shutdoown the output by pulling down the soft-start.

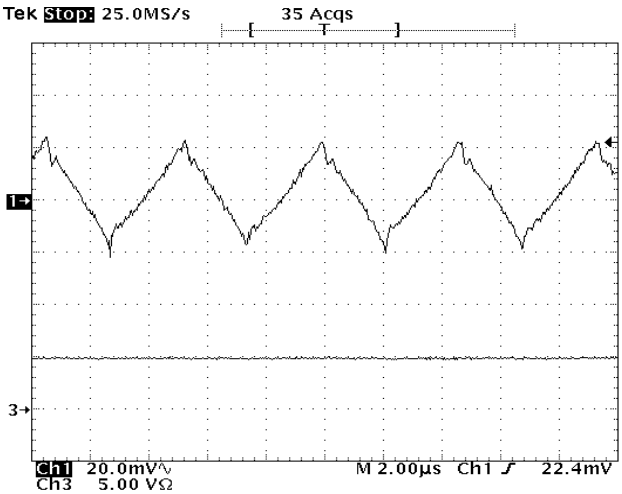


Figure 18 - 3.3V output voltage ripple @ I_{OUT}=5A.

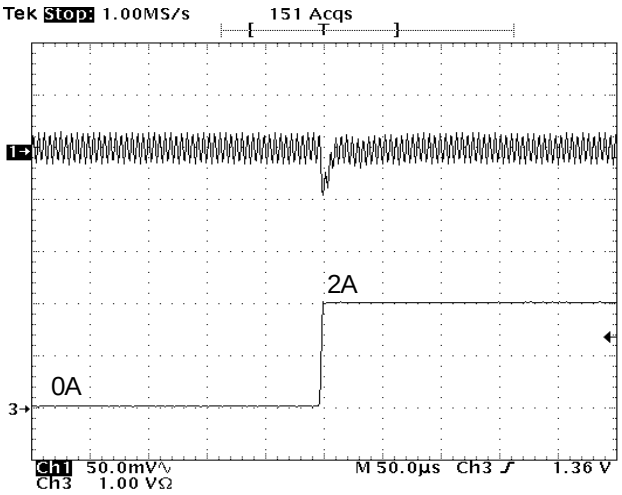


Figure 19 - Transient response @ I_{OUT}=0 to 2A.

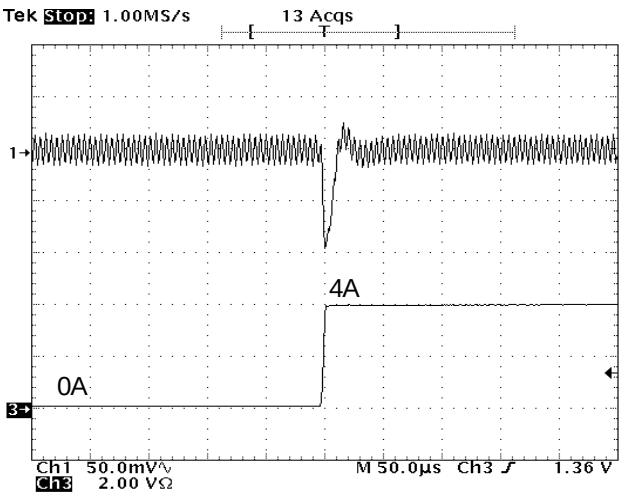
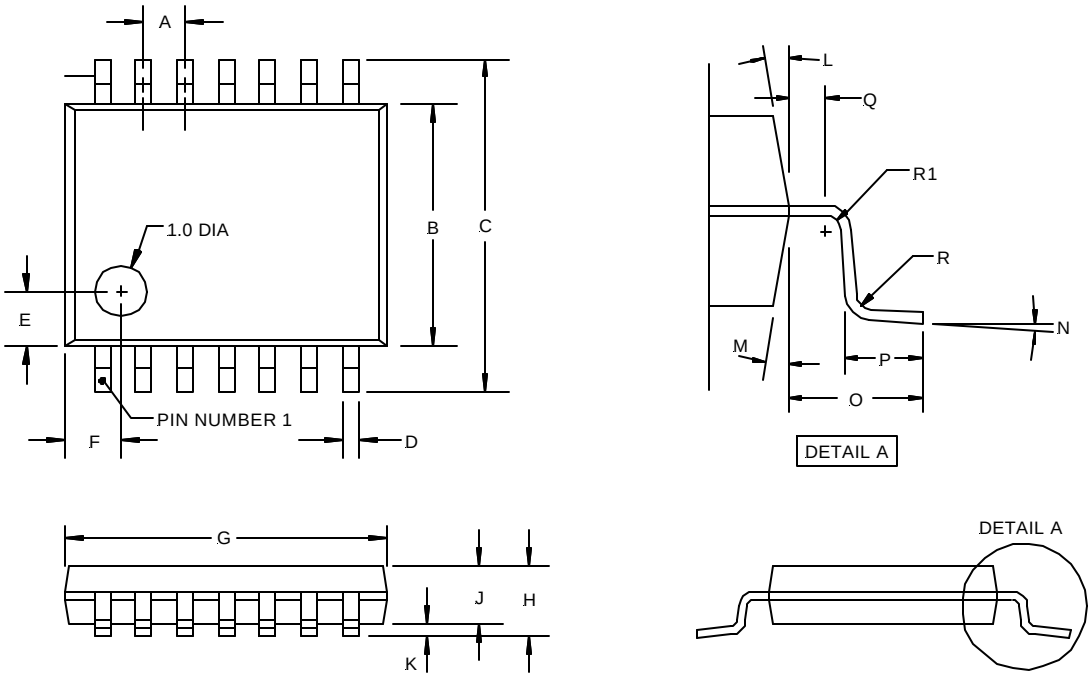


Figure 20 - Transient response @ I_{OUT}=0 to 4A.

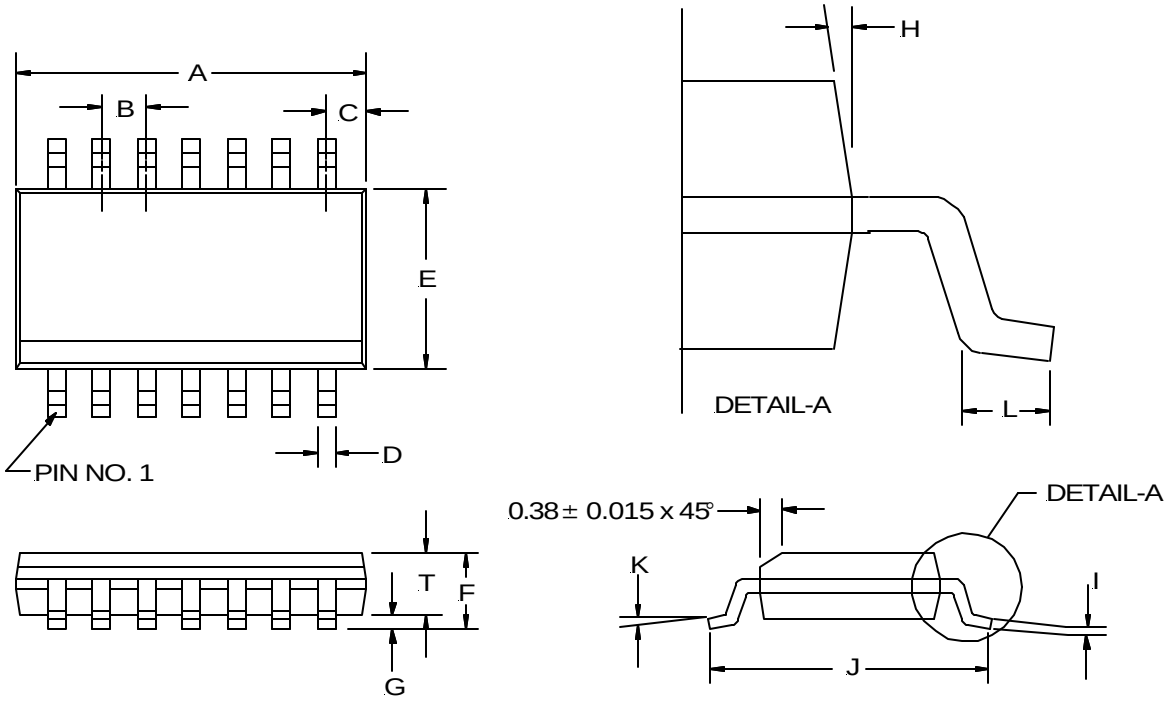
(F) TSSOP Package
14-Pin



SYMBOL	14-PIN		
DESIG	MIN	NOM	MAX
A		0.65 BSC	
B	4.30	4.40	4.50
C		6.40 BSC	
D	0.19	---	0.30
E		1.00	
F		1.00	
G	4.90	5.00	5.10
H	---	---	1.10
J	0.85	0.90	0.95
K	0.05	---	0.15
L		12° REF	
M		12° REF	
N	0°	---	8°
O		1.00 REF	
P	0.50	0.60	0.75
Q		0.20	
R	0.09	---	---
R1	0.09	---	---

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

(S) SOIC Package
14-Pin Surface Mount, Narrow Body



14-PIN		
SYMBOL	**MIN**	**MAX**
A	8.56	8.74
B	1.27 BSC	
C	0.51 REF	
D	0.36	0.46
E	3.81	3.99
F	1.52	1.72
G	0.10	0.25
H	7° BSC	
I	0.19	0.25
J	5.80	6.20
K	0°	8°
L	0.41	1.27
T	1.37	1.57

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

PACKAGE SHIPMENT METHOD

PKG DESIG	PACKAGE DESCRIPTION	PIN COUNT	PARTS PER TUBE	PARTS PER REEL	T & R Orientation
F	TSSOP Plastic	14	100	2500	Fig A
S	SOIC, Narrow Body	14	55	2500	Fig B

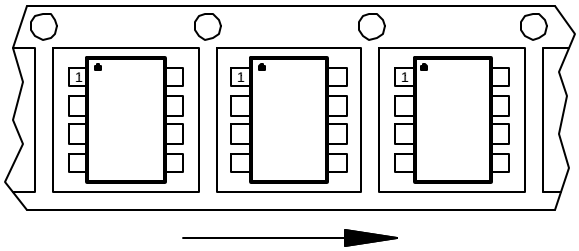


Figure A

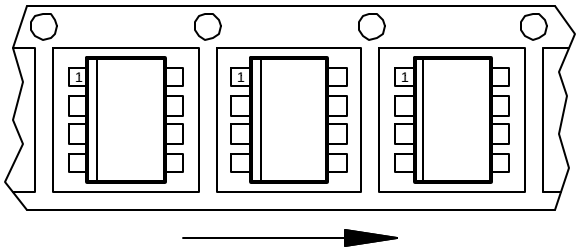


Figure B

International
IOR Rectifier

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