

## Low-Voltage, Single and Dual Supply, High Performance, Quad SPST, Analog Switches

The Intersil ISL43140–ISL43142 devices are CMOS, precision, quad analog switches designed to operate from a single +2V to +12V supply or from a ±2V to ±6V supply. Targeted applications include battery powered equipment that benefit from the devices' low power consumption (1μW), low leakage currents (1nA max), and fast switching speeds ( $t_{ON} = 30\text{ns}$ ,  $t_{OFF} = 18\text{ns}$ ). A 12Ω maximum  $R_{ON}$  flatness ensures signal fidelity, while channel-to-channel mismatch is guaranteed to be less than 2.5Ω. The 3mm x 3mm Quad No-Lead Flatpack (QFN) package alleviates board space limitations, making this newest line of low-voltage switches an ideal solution.

The ISL43140/ISL43141/ISL43142 are quad single-pole/single-throw (SPST) devices. The ISL43140 has four normally closed (NC) switches; the ISL43141 has four normally open (NO) switches; the ISL43142 has two NO and two NC switches and can be used as a dual SPDT, or a dual 2:1 multiplexer.

Table 1 summarizes the performance of this family.

**TABLE 1. FEATURES AT A GLANCE**

	<b>ISL43140</b>	<b>ISL43141</b>	<b>ISL43142</b>
Number of Switches	4	4	4
Configuration	All NC	All NO	2 NC / 2 NO
10.8V $R_{ON}$	50Ω	50Ω	50Ω
10.8V $t_{ON} / t_{OFF}$	30ns / 18ns	30ns / 18ns	30ns / 18ns
±4.5V $R_{ON}$	50Ω	50Ω	50Ω
±4.5V $t_{ON} / t_{OFF}$	40ns / 15ns	40ns / 15ns	40ns / 15ns
4.5V $R_{ON}$	110Ω	110Ω	110Ω
4.5V $t_{ON} / t_{OFF}$	50ns / 20ns	50ns / 20ns	50ns / 20ns
2.7V $R_{ON}$	200Ω	200Ω	200Ω
2.7V $t_{ON} / t_{OFF}$	120ns / 25ns	120ns / 25ns	120ns / 25ns
Packages	16 Ld SOIC (N), 16 Ld 3x3 QFN, 16 Ld TSSOP		

## Features

- Fully Specified at ±5V, 12V, 5V, and 3V Supplies for 10% Tolerances
- Four Separately Controlled SPST Switches
- Pin Compatible with DG411/DG412/DG413
- ON Resistance ( $R_{ON}$ ) ..... 50Ω
- $R_{ON}$  Matching Between Channels.....2Ω
- Low Charge Injection ..... 5pC (Max)
- Low Power Consumption ( $P_D$ ).....<1μW
- Low Leakage Current (Max at 85°C) ..... 5nA
- Fast Switching Action
  - $t_{ON}$  ..... 30ns
  - $t_{OFF}$  ..... 18ns
- Guaranteed Break-Before-Make (ISL43142 only)
- Minimum 2000V ESD Protection per Method 3015.7
- TTL, CMOS Compatible

## Applications

- Battery Powered, Handheld, and Portable Equipment
  - Cellular/Mobile Phones
  - Pagers
  - Laptops, Notebooks, Palmtops
- Communications Systems
  - Military Radios
  - RF "Tee" Switches
- Test Equipment
  - Ultrasound
  - Electrocardiograph
- Heads-Up Displays
- Audio and Video Switching
- General Purpose Circuits
  - +3V/+5V DACs and ADCs
  - Digital Filters
  - Operational Amplifier Gain Switching Networks
  - High Frequency Analog Switching
  - High Speed Multiplexing

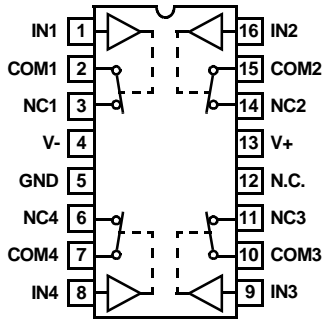
## Related Literature

- Technical Brief TB363 "Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)"

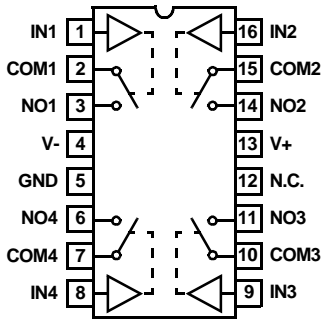
# ISL43140, ISL43141, ISL43142

## Pinouts (Note 1)

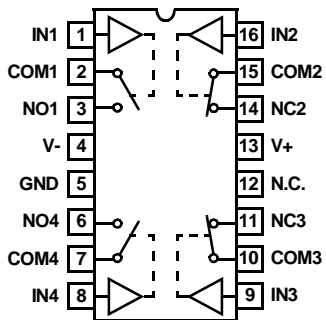
**ISL43140 (SOIC, TSSOP)**  
TOP VIEW



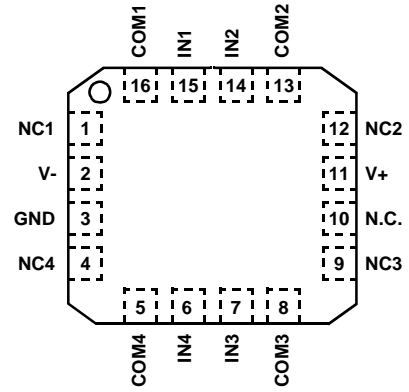
**ISL43141 (SOIC, TSSOP)**  
TOP VIEW



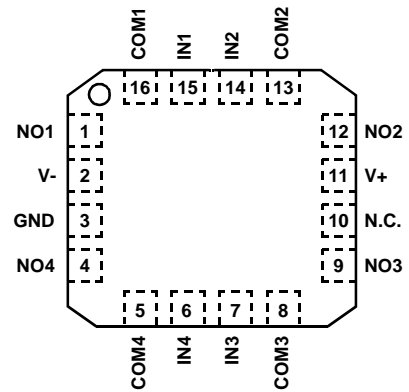
**ISL43142 (SOIC, TSSOP)**  
TOP VIEW



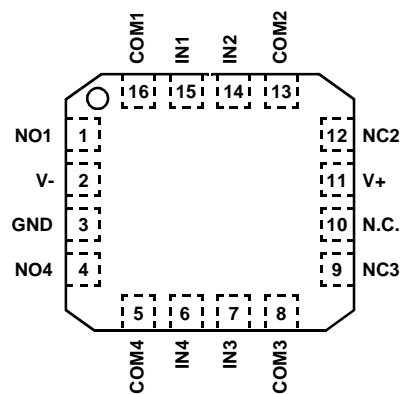
**ISL43140 (QFN)**  
TOP VIEW



**ISL43141 (QFN)**  
TOP VIEW



**ISL43142 (QFN)**  
TOP VIEW



**NOTE:**

1. Switches Shown for Logic "0" Input.

### Truth Table

LOGIC	ISL43140	ISL43141	ISL43142	
	SW 1, 2, 3, 4	SW 1, 2, 3, 4	SW 1, 4	SW 2, 3
0	ON	OFF	OFF	ON
1	OFF	ON	ON	OFF

NOTE: Logic "0" ≤ 0.8V. Logic "1" ≥ 2.4V.

### Pin Descriptions

PIN	FUNCTION
V+	Positive Power Supply Input
V-	Negative Power Supply Input. Connect to GND for Single Supply Configurations.
GND	Ground Connection
IN	Digital Control Input
COM	Analog Switch Common Pin
NO	Analog Switch Normally Open Pin
NC	Analog Switch Normally Closed Pin
N.C.	No Internal Connection

### Ordering Information

PART NO. (BRAND) (NOTE 2)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
ISL43140IB	-40 to 85	16 Ld SOIC (N)	M16.15
ISL43140IR* (140I)	-40 to 85	16 Ld QFN	L16.3x3
ISL43140IV	-40 to 85	16 Ld TSSOP	M16.173
ISL43141IB	-40 to 85	16 Ld SOIC (N)	M16.15
ISL43141IR* (141I)	-40 to 85	16 Ld QFN	L16.3x3
ISL43141IV	-40 to 85	16 Ld TSSOP	M16.173
ISL43142IB	-40 to 85	16 Ld SOIC (N)	M16.15
ISL43142IR* (142I)	-40 to 85	16 Ld QFN	L16.3x3
ISL43142IV	-40 to 85	16 Ld TSSOP	M16.173

NOTES:

- Most surface mount devices are available on tape and reel; add "-T" to suffix.

\* In Development.

**Absolute Maximum Ratings**

V+ to V-	-0.3 to 15V
V+ to GND	-0.3 to 15V
V- to GND	-15 to 0.3V
All Other Pins (Note 3)	((V-) - 0.3V) to ((V+) + 0.3V)
Continuous Current (Any Terminal)	10mA
Peak Current, IN, NO, NC, or COM	
(Pulsed 1ms, 10% Duty Cycle, Max)	20mA
ESD Rating (Per MIL-STD-883 Method 3015)	>2kV

**Operating Conditions**

Temperature Range	
ISL4314XIX	-40°C to 85°C

**Thermal Information**

Thermal Resistance (Typical, Note 4)	$\theta_{JA}$ (°C/W)
16 Ld SOIC Package	115
16 Ld QFN Package	75
16 Ld TSSOP Package	150
Maximum Junction Temperature (Plastic Package)	150°C
Moisture Sensitivity (See Technical Brief TB363)	
All Other Packages	Level 1
QFN Package	Level 2
Maximum Storage Temperature Range	-65°C to 150°C
Maximum Lead Temperature (Soldering 10s)	300°C
(SOIC and TSSOP - Lead Tips Only)	

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

3. Signals on NC, NO, COM, or IN exceeding V+ or V- are clamped by internal diodes. Limit forward diode current to maximum current ratings.
4.  $\theta_{JA}$  is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

**Electrical Specifications: ±5V Supply** Test Conditions  $V_{SUPPLY} = \pm 4.5V$  to  $\pm 5.5V$ , GND = 0V,  $V_{INH} = 2.4V$ ,  $V_{INL} = 0.8V$  (Note 5), Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	(NOTE 6) MIN	TYP	(NOTE 6) MAX	UNITS
<b>ANALOG SWITCH CHARACTERISTICS</b>						
Analog Signal Range, $V_{ANALOG}$		Full	V-	-	V+	V
ON Resistance, $R_{ON}$	$V_S = \pm 4.5V$ , $I_{COM} = 1.0mA$ , $V_{NO}$ or $V_{NC} = \pm 3V$ , See Figure 5	25	-	50	65	$\Omega$
		Full	-	-	75	$\Omega$
$R_{ON}$ Matching Between Channels, $\Delta R_{ON}$	$V_S = \pm 4.5V$ , $I_{COM} = 1.0mA$ , $V_{NO}$ or $V_{NC} = \pm 3V$	25	-	2	2.5	$\Omega$
		Full	-	-	5	$\Omega$
$R_{ON}$ Flatness, $R_{FLAT(ON)}$	$V_S = \pm 4.5V$ , $I_{COM} = 1.0mA$ , $V_{NO}$ or $V_{NC} = \pm 3V$ , Note 8	25	-	10	12	$\Omega$
		Full	-	-	13	$\Omega$
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	$V_S = \pm 5.5V$ , $V_{COM} = \pm 4.5V$ , $V_{NO}$ or $V_{NC} = \mp 4.5V$ , Note 7	25	-1	0.01	1	nA
		Full	-5	-	5	nA
COM OFF Leakage Current, $I_{COM(OFF)}$	$V_S = \pm 5.5V$ , $V_{COM} = \pm 4.5V$ , $V_{NO}$ or $V_{NC} = \mp 4.5V$ , Note 7	25	-1	0.01	1	nA
		Full	-5	-	5	nA
COM ON Leakage Current, $I_{COM(ON)}$	$V_S = \pm 5.5V$ , $V_{COM} = V_{NO}$ or $V_{NC} = \pm 4.5V$ , Note 7	25	-2	0.01	2	nA
		Full	-10	-	10	nA
<b>DIGITAL INPUT CHARACTERISTICS</b>						
Input Voltage High, $V_{INH}$		Full	2.4	1.6	-	V
Input Voltage Low, $V_{INL}$		Full	-	1.6	0.8	V
Input Current, $I_{INH}$ , $I_{INL}$	$V_S = \pm 5.5V$ , $V_{IN} = 0V$ or $V+$	Full	-0.5	0.03	0.5	$\mu A$
<b>DYNAMIC CHARACTERISTICS</b>						
Turn-ON Time, $t_{ON}$	$V_S = \pm 4.5V$ , $V_{NO}$ or $V_{NC} = \pm 3V$ , $R_L = 300\Omega$ , $C_L = 35pF$ , $V_{IN} = 0$ to 3V, See Figure 1	25	-	40	80	ns
		Full	-	-	100	ns
Turn-OFF Time, $t_{OFF}$	$V_S = \pm 4.5V$ , $V_{NO}$ or $V_{NC} = \pm 3V$ , $R_L = 300\Omega$ , $C_L = 35pF$ , $V_{IN} = 0$ to 3V, See Figure 1	25	-	15	30	ns
		Full	-	-	40	ns
Break-Before-Make Time Delay (ISL43142), $t_D$	$V_S = \pm 5.5V$ , $V_{NO}$ or $V_{NC} = \pm 3V$ , $R_L = 300\Omega$ , $C_L = 35pF$ , $V_{IN} = 0$ to 3V, See Figure 3	Full	5	20	-	ns
Charge Injection, Q	$C_L = 1.0nF$ , $V_G = 0V$ , $R_G = 0\Omega$ , See Figure 2	25	-	1	5	pC
NO or NC OFF Capacitance, $C_{OFF}$	$f = 1MHz$ , $V_{NO}$ or $V_{NC} = V_{COM} = 0V$ , See Figure 7	25	-	7	-	pF
COM OFF Capacitance, $C_{COM(OFF)}$	$f = 1MHz$ , $V_{NO}$ or $V_{NC} = V_{COM} = 0V$ , See Figure 7	25	-	7	-	pF
COM ON Capacitance, $C_{COM(ON)}$	$f = 1MHz$ , $V_{NO}$ or $V_{NC} = V_{COM} = 0V$ , See Figure 7	25	-	14	-	pF

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**Electrical Specifications: ±5V Supply** Test Conditions  $V_{SUPPLY} = \pm 4.5V$  to  $\pm 5.5V$ ,  $GND = 0V$ ,  $V_{INH} = 2.4V$ ,  $V_{INL} = 0.8V$  (Note 5), Unless Otherwise Specified (Continued)

PARAMETER	TEST CONDITIONS	TEMP (°C)	(NOTE 6) MIN	TYP	(NOTE 6) MAX	UNITS
OFF Isolation	$R_L = 50\Omega$ , $C_L = 15pF$ , $f = 100kHz$ ,	25	-	>90	-	dB
Crosstalk, Note 9	$V_{NO}$ or $V_{NC} = 1V_{RMS}$ , See Figures 4, 6, and 19	25	-	<-90	-	dB
All Hostile Crosstalk	$R_L = 50\Omega$ , $C_L = 15pF$ , $f = 10MHz$ , $V_{NO}$ or $V_{NC} = 1V_{RMS}$ , See Figure 19	25	-	-60	-	dB
Power Supply Rejection Ratio	$R_L = 50\Omega$ , $C_L = 15pF$ , $f = 1MHz$ , See Figure 20	25	-	60	-	dB
<b>POWER SUPPLY CHARACTERISTICS</b>						
Power Supply Range		Full	±2	-	±6	V
Positive Supply Current, I+	$V_S = \pm 5.5V$ , $V_{IN} = 0V$ or $V+$ , Switch On or Off	25	-1	0.05	1	μA
Negative Supply Current, I-		Full	-1	-	1	μA
		25	-1	0.05	1	μA
		Full	-1	-	1	μA

NOTES:

5.  $V_{IN}$  = Input voltage to perform proper function.
6. The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
7. Leakage parameter is 100% tested at high temp, and guaranteed by correlation at 25°C.
8. Flatness is defined as the delta between the maximum and minimum  $R_{ON}$  values over the specified voltage range.
9. Between any two switches.

**Electrical Specifications: 12V Supply** Test Conditions:  $V+ = +10.8V$  to  $+13.2V$ ,  $V- = GND = 0V$ ,  $V_{INH} = 5V$ ,  $V_{INL} = 0.8V$  (Note 5), Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	(NOTE 6) MIN	TYP	(NOTE 6) MAX	UNITS
<b>ANALOG SWITCH CHARACTERISTICS</b>						
Analog Signal Range, $V_{ANALOG}$		Full	0	-	$V+$	V
ON Resistance, $R_{ON}$	$V+ = 10.8V$ , $I_{COM} = 1.0mA$ , $V_{NO}$ or $V_{NC} = 9V$ , See Figure 5	25	-	50	65	Ω
		Full	-	60	75	Ω
$R_{ON}$ Matching Between Channels, $\Delta R_{ON}$	$V+ = 10.8V$ , $I_{COM} = 1.0mA$ , $V_{NO}$ or $V_{NC} = 9V$	25	-	2	2.5	Ω
		Full	-	-	5	Ω
$R_{ON}$ Flatness, $R_{FLAT(ON)}$	$V+ = 10.8V$ , $I_{COM} = 1.0mA$ , $V_{NO}$ or $V_{NC} = 3V, 6V, 9V$ , Note 8	25	-	8	12	Ω
		Full	-	9	13	Ω
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	$V+ = 13.2V$ , $V_{COM} = 1V, 10V$ , $V_{NO}$ or $V_{NC} = 10V, 1V$ , Note 7	25	-1	-	1	nA
		Full	-5	-	5	nA
COM OFF Leakage Current, $I_{COM(OFF)}$	$V+ = 13.2V$ , $V_{COM} = 10V, 1V$ , $V_{NO}$ or $V_{NC} = 1V, 10V$ , Note 7	25	-1	-	1	nA
		Full	-5	-	5	nA
COM ON Leakage Current, $I_{COM(ON)}$	$V+ = 13.2V$ , $V_{COM} = 1V, 10V$ , or $V_{NO}$ or $V_{NC} = 1V, 10V$ , Note 7	25	-2	-	2	nA
		Full	-10	-	10	nA
<b>DIGITAL INPUT CHARACTERISTICS</b>						
Input Voltage High, $V_{INH}$		Full	3.5	3.1	-	V
Input Voltage Low, $V_{INL}$		Full	-	-	0.8	V
Input Current, $I_{INH}$ , $I_{INL}$	$V+ = 13.2V$ , $V_{IN} = 0V$ or $V+$	Full	-1	-	1	μA
<b>DYNAMIC CHARACTERISTICS</b>						
Turn-ON Time, $t_{ON}$	$V+ = 10.8V$ , $V_{NO}$ or $V_{NC} = 10V$ , $R_L = 300\Omega$ , $C_L = 35pF$ , $V_{IN} = 0$ to $3.3V$ , See Figure 1	25	-	30	70	ns
		Full	-	34	100	ns
Turn-OFF Time, $t_{OFF}$	$V+ = 10.8V$ , $V_{NO}$ or $V_{NC} = 10V$ , $R_L = 300\Omega$ , $C_L = 35pF$ , $V_{IN} = 0$ to $3.3V$ , See Figure 1	25	-	18	50	ns
		Full	-	20	75	ns
Break-Before-Make Time Delay (ISL43142), $t_D$	$V+ = 13.2V$ , $V_{NO}$ or $V_{NC} = 10V$ , $R_L = 300\Omega$ , $C_L = 35pF$ , $V_{IN} = 0$ to $3.3V$ , See Figure 3	Full	0	8	-	ns

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**Electrical Specifications: 12V Supply** Test Conditions:  $V_+ = +10.8V$  to  $+13.2V$ ,  $V_- = GND = 0V$ ,  $V_{INH} = 5V$ ,  $V_{INL} = 0.8V$  (Note 5), Unless Otherwise Specified (Continued)

PARAMETER	TEST CONDITIONS	TEMP (°C)	(NOTE 6) MIN	TYP	(NOTE 6) MAX	UNITS
Charge Injection, Q	$C_L = 1.0nF$ , $V_G = 0V$ , $R_G = 0\Omega$ , See Figure 2	25	-	5	15	pC
OFF Isolation	$R_L = 50\Omega$ , $C_L = 15pF$ , $f = 100kHz$ , $V_{NO}$ or $V_{NC} = 1V_{RMS}$ , See Figures 4, 6, and 19	25	-	>90	-	dB
Crosstalk, Note 9		25	-	<-90	-	dB
All Hostile Crosstalk	$R_L = 50\Omega$ , $C_L = 15pF$ , $f = 10MHz$ , $V_{NO}$ or $V_{NC} = 1V_{RMS}$ , See Figure 19	25	-	-60	-	dB
Power Supply Rejection Ratio	$R_L = 50\Omega$ , $C_L = 15pF$ , $f = 1MHz$ , See Figure 20	25	-	60	-	dB
NO or NC OFF Capacitance, $C_{OFF}$	$f = 1MHz$ , $V_{NO}$ or $V_{NC} = V_{COM} = 0V$ , See Figure 7	25	-	7	-	pF
COM OFF Capacitance, $C_{COM(OFF)}$	$f = 1MHz$ , $V_{NO}$ or $V_{NC} = V_{COM} = 0V$ , See Figure 7	25	-	7	-	pF
COM ON Capacitance, $C_{COM(ON)}$	$f = 1MHz$ , $V_{NO}$ or $V_{NC} = V_{COM} = 0V$ , See Figure 7	25	-	14	-	pF
<b>POWER SUPPLY CHARACTERISTICS</b>						
Positive Supply Current, $I_+$	$V_+ = 13.2V$ , $V_{IN} = 0V$ or $V_+$ , Switch On or Off	25	-1	0.05	1	$\mu A$
		Full	-1	-	1	$\mu A$
Negative Supply Current, $I_-$		25	-1	0.05	1	$\mu A$
		Full	-1	-	1	$\mu A$

**Electrical Specifications: 5V Supply** Test Conditions:  $V_+ = +4.5V$  to  $+5.5V$ ,  $V_- = GND = 0V$ ,  $V_{INH} = 2.4V$ ,  $V_{INL} = 0.8V$  (Note 5), Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (NOTE 6)	TYP	MAX (NOTE 6)	UNITS
<b>ANALOG SWITCH CHARACTERISTICS</b>						
Analog Signal Range, $V_{ANALOG}$		Full	0	-	$V_+$	V
ON Resistance, $R_{ON}$	$V_+ = 4.5V$ , $I_{COM} = 1.0mA$ , $V_{NO}$ or $V_{NC} = 3.5V$ , See Figure 5	25	-	110	120	$\Omega$
		Full	-	-	150	$\Omega$
$R_{ON}$ Matching Between Channels, $\Delta R_{ON}$	$V_+ = 4.5V$ , $I_{COM} = 1.0mA$ , $V_{NO}$ or $V_{NC} = 3.5V$	25	-	1.5	2	$\Omega$
		Full	-	-	5	$\Omega$
$R_{ON}$ Flatness, $R_{FLAT(ON)}$	$V_+ = 4.5V$ , $I_{COM} = 1.0mA$ , $V_{NO}$ or $V_{NC} = 1.5V$ to $4.5V$ , Note 8	25	-	12	16	$\Omega$
		Full	-	-	20	$\Omega$
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	$V_+ = 5.5V$ , $V_{COM} = 1V$ , $4.5V$ , $V_{NO}$ or $V_{NC} = 4.5V$ , $1V$ , Note 7	25	-1	0.01	1	nA
		Full	-5	-	5	nA
COM OFF Leakage Current, $I_{COM(OFF)}$	$V_+ = 5.5V$ , $V_{COM} = 1V$ , $4.5V$ , $V_{NO}$ or $V_{NC} = 4.5V$ , $1V$ , Note 7	25	-1	0.01	1	nA
		Full	-5	-	5	nA
COM ON Leakage Current, $I_{COM(ON)}$	$V_+ = 5.5V$ , $V_{COM} = 1V$ , $4.5V$ , Note 7	25	-2	-	2	nA
		Full	-10	-	10	nA
<b>DIGITAL INPUT CHARACTERISTICS</b>						
Input Voltage High, $V_{INH}$		Full	2.4	1.6	-	V
Input Voltage Low, $V_{INL}$		Full	-	1.6	0.8	V
Input Current, $I_{INH}$ , $I_{INL}$	$V_+ = 5.5V$ , $V_{IN} = 0V$ or $V_+$	Full	-0.5	0.03	0.5	$\mu A$
<b>DYNAMIC CHARACTERISTICS</b>						
Turn-ON Time, $t_{ON}$	$V_+ = 4.5V$ , $V_{NO}$ or $V_{NC} = 3V$ , $R_L = 300\Omega$ , $C_L = 35pF$ , $V_{IN} = 0$ to $3V$ , See Figure 1	25	-	50	100	ns
		Full	-	-	150	ns
Turn-OFF Time, $t_{OFF}$	$V_+ = 4.5V$ , $V_{NO}$ or $V_{NC} = 3V$ , $R_L = 300\Omega$ , $C_L = 35pF$ , $V_{IN} = 0$ to $3V$ , See Figure 1	25	-	20	50	ns
		Full	-	-	75	ns
Break-Before-Make Time Delay (ISL43142), $t_D$	$V_+ = 5.5V$ , $V_{NO}$ or $V_{NC} = 3V$ , $R_L = 300\Omega$ , $C_L = 35pF$ , $V_{IN} = 0$ to $3V$ , See Figure 3	Full	10	30	-	ns
Charge Injection, Q	$C_L = 1.0nF$ , $V_G = 0V$ , $R_G = 0\Omega$ , See Figure 2	25	-	1	5	pC
OFF Isolation	$R_L = 50\Omega$ , $C_L = 15pF$ , $f = 100kHz$ , $V_{NO}$ or $V_{NC} = 1V_{RMS}$ , See Figures 4, 6, and 19	25	-	>90	-	dB
Crosstalk, Note 9		25	-	<-90	-	dB

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### Electrical Specifications: 5V Supply

Test Conditions:  $V_+ = +4.5V$  to  $+5.5V$ ,  $V_- = GND = 0V$ ,  $V_{INH} = 2.4V$ ,  $V_{INL} = 0.8V$  (Note 5), Unless Otherwise Specified (Continued)

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (NOTE 6)	TYP	MAX (NOTE 6)	UNITS
All Hostile Crosstalk	$R_L = 50\Omega$ , $C_L = 15pF$ , $f = 10MHz$ , $V_{NO}$ or $V_{NC} = 1V_{RMS}$ , See Figure 19	25	-	-60	-	dB
Power Supply Rejection Ratio	$R_L = 50\Omega$ , $C_L = 15pF$ , $f = 1MHz$ , See Figure 20	25	-	60	-	dB
NO or NC OFF Capacitance, $C_{OFF}$	$f = 1MHz$ , $V_{NO}$ or $V_{NC} = V_{COM} = 0V$ , See Figure 7	25	-	7	-	pF
COM OFF Capacitance, $C_{COM(OFF)}$	$f = 1MHz$ , $V_{NO}$ or $V_{NC} = V_{COM} = 0V$ , See Figure 7	25	-	7	-	pF
COM ON Capacitance, $C_{COM(ON)}$	$f = 1MHz$ , $V_{NO}$ or $V_{NC} = V_{COM} = 0V$ , See Figure 7	25	-	14	-	pF
<b>POWER SUPPLY CHARACTERISTICS</b>						
Positive Supply Current, $I_+$	$V_+ = 5.5V$ , $V_{IN} = 0V$ or $V_+$ , Switch On or Off	25	-1	0.05	1	$\mu A$
		Full	-1	-	1	$\mu A$
Negative Supply Current, $I_-$		25	-1	0.05	1	$\mu A$
		Full	-1	-	1	$\mu A$

### Electrical Specifications: 3V to 3.3V Supply

Test Conditions:  $V_+ = +2.7V$  to  $+3.6V$ ,  $V_- = GND = 0V$ ,  $V_{INH} = 2.4V$ ,  $V_{INL} = 0.8V$  (Note 5), Unless Otherwise Specified

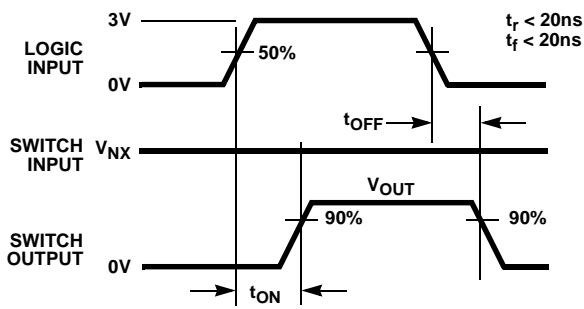
PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (NOTE 6)	TYP	MAX (NOTE 6)	UNITS
<b>ANALOG SWITCH CHARACTERISTICS</b>						
Analog Signal Range, $V_{ANALOG}$		Full	0	-	$V_+$	V
ON Resistance, $R_{ON}$	$V_+ = 2.7V$ , $I_{COM} = 1.0mA$ , $V_{NO}$ or $V_{NC} = 1V$ , See Figure 5	25	-	200	250	$\Omega$
		Full	-	-	270	$\Omega$
$R_{ON}$ Matching Between Channels, $\Delta R_{ON}$	$V_+ = 2.7V$ , $I_{COM} = 1.0mA$ , $V_{NO}$ or $V_{NC} = 1V$	25	-	2	4	$\Omega$
		Full	-	-	6	$\Omega$
$R_{ON}$ Flatness, $R_{FLAT(ON)}$	$V_+ = 2.7V$ , $I_{COM} = 1.0mA$ , $V_{NO}$ or $V_{NC} = 0.5V$ to $1.5V$ , Note 8	25	-	80	100	$\Omega$
		Full	-	-	120	$\Omega$
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	$V_+ = 3.6V$ , $V_{COM} = 1V$ , $2.6V$ , $V_{NO}$ or $V_{NC} = 2.6V$ , $1V$ , Note 7	25	-1	0.01	1	nA
		Full	-5	-	5	nA
COM OFF Leakage Current, $I_{COM(OFF)}$	$V_+ = 3.6V$ , $V_{COM} = 1V$ , $2.6V$ , $V_{NO}$ or $V_{NC} = 2.6V$ , $1V$ , Note 7	25	-1	0.01	1	nA
		Full	-5	-	5	nA
COM ON Leakage Current, $I_{COM(ON)}$	$V_+ = 3.6V$ , $V_{COM} = 1V$ , $2.6V$ , Note 7	25	-2	-	2	nA
		Full	-10	-	10	nA
<b>DIGITAL INPUT CHARACTERISTICS</b>						
Input Voltage High, $V_{INH}$		Full	2.4	1.6	-	V
Input Voltage Low, $V_{INL}$		Full	-	1.6	0.8	V
Input Current, $I_{INH}$ , $I_{INL}$	$V_+ = 3.6V$ , $V_{IN} = 0V$ or $V_+$	Full	-0.5	0.03	0.5	$\mu A$
<b>DYNAMIC CHARACTERISTICS</b>						
Turn-ON Time, $t_{ON}$	$V_+ = 2.7V$ , $V_{NO}$ or $V_{NC} = 1.5V$ , $R_L = 300\Omega$ , $C_L = 35pF$ , $V_{IN} = 0$ to $V_+$ , See Figure 1	25	-	120	180	ns
		Full	-	-	220	ns
Turn-OFF Time, $t_{OFF}$	$V_+ = 2.7V$ , $V_{NO}$ or $V_{NC} = 1.5V$ , $R_L = 300\Omega$ , $C_L = 35pF$ , $V_{IN} = 0$ to $V_+$ , See Figure 1	25	-	25	45	ns
		Full	-	-	60	ns
Break-Before-Make Time Delay (ISL43142), $t_D$	$V_+ = 3.6V$ , $V_{NO}$ or $V_{NC} = 1.5V$ , $R_L = 300\Omega$ , $C_L = 35pF$ , $V_{IN} = 0$ to $3V$ , See Figure 3	25	15	50	-	ns
Charge Injection, Q	$C_L = 1.0nF$ , $V_G = 0V$ , $R_G = 0\Omega$ , See Figure 2	25	-	0.5	5	pC
OFF Isolation	$R_L = 50\Omega$ , $C_L = 15pF$ , $f = 100kHz$ , $V_{NO}$ or $V_{NC} = 1V_{RMS}$ , See Figures 4, 6, and 19	25	-	>90	-	dB
Crosstalk, Note 9		25	-	<-90	-	dB
All Hostile Crosstalk	$R_L = 50\Omega$ , $C_L = 15pF$ , $f = 10MHz$ , $V_{NO}$ or $V_{NC} = 1V_{RMS}$ , See Figure 19	25	-	-60	-	dB
Power Supply Rejection Ratio	$R_L = 50\Omega$ , $C_L = 15pF$ , $f = 1MHz$ , See Figure 20	25	-	60	-	dB

**Electrical Specifications: 3V to 3.3V Supply**

Test Conditions:  $V_+ = +2.7V$  to  $+3.6V$ ,  $V_- = GND = 0V$ ,  $V_{INH} = 2.4V$ ,  $V_{INL} = 0.8V$  (Note 5), Unless Otherwise Specified (Continued)

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (NOTE 6)	TYP	MAX (NOTE 6)	UNITS
NO or NC OFF Capacitance, $C_{OFF}$	$f = 1MHz$ , $V_{NO}$ or $V_{NC} = V_{COM} = 0V$ , See Figure 7	25	-	7	-	pF
COM OFF Capacitance, $C_{COM(OFF)}$	$f = 1MHz$ , $V_{NO}$ or $V_{NC} = V_{COM} = 0V$ , See Figure 7	25	-	7	-	pF
COM ON Capacitance, $C_{COM(ON)}$	$f = 1MHz$ , $V_{NO}$ or $V_{NC} = V_{COM} = 0V$ , See Figure 7	25	-	14	-	pF
<b>POWER SUPPLY CHARACTERISTICS</b>						
Positive Supply Current, $I_+$	$V_+ = 3.6V$ , $V_{IN} = 0V$ or $V_+$ , Switch On or Off	25	-1	0.05	1	$\mu A$
		Full	-1	-	1	$\mu A$
Negative Supply Current, $I_-$		25	-1	0.05	1	$\mu A$
		Full	-1	-	1	$\mu A$

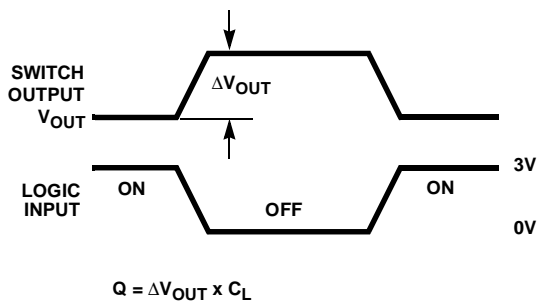
**Test Circuits and Waveforms**



Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 1A. MEASUREMENT POINTS

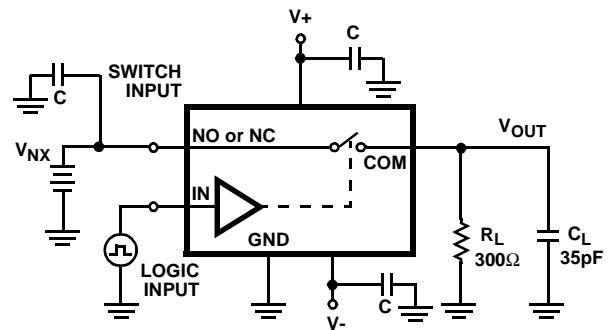
FIGURE 1. SWITCHING TIMES



Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 2A. MEASUREMENT POINTS

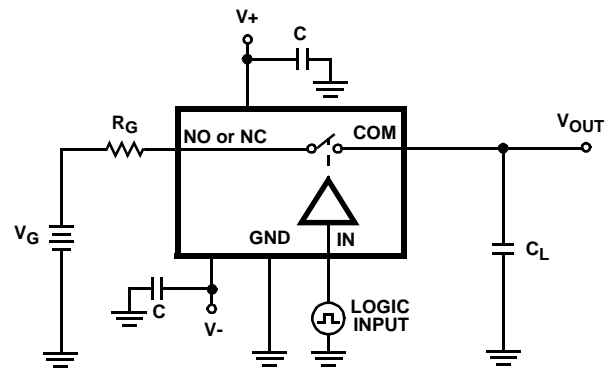
FIGURE 2. CHARGE INJECTION



Repeat test for all switches.  $C_L$  includes fixture and stray capacitance.

$$V_{OUT} = V_{(NO \text{ or } NC)} \frac{R_L}{R_L + R_{(ON)}}$$

FIGURE 1B. TEST CIRCUIT



Repeat test for all switches.  $C_L$  includes fixture and stray capacitance.

FIGURE 2B. TEST CIRCUIT

Test Circuits and Waveforms (Continued)

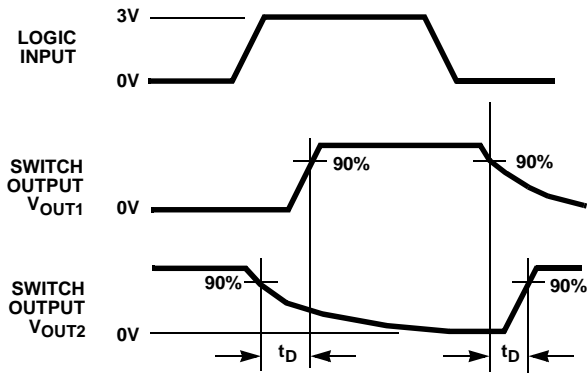
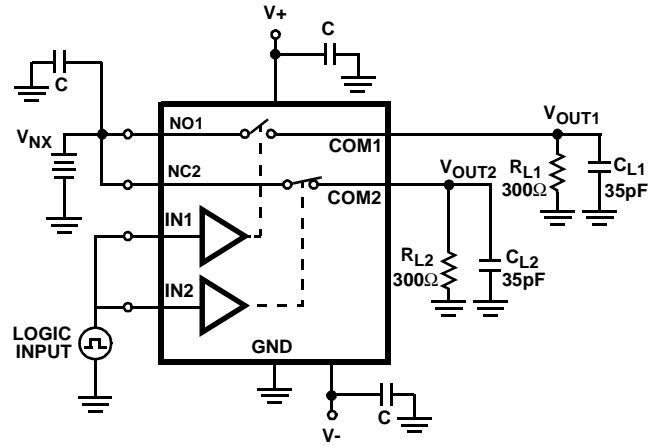


FIGURE 3A. MEASUREMENT POINTS

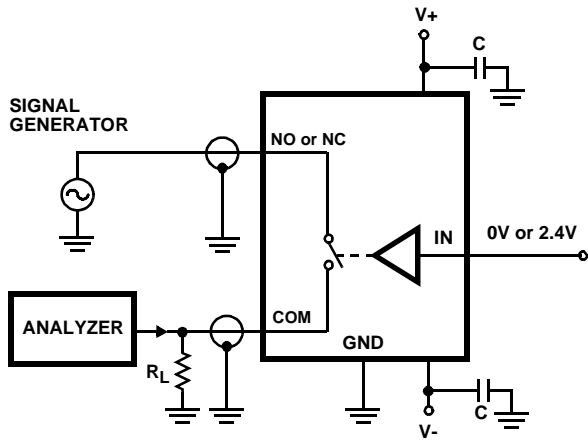
FIGURE 3. BREAK-BEFORE-MAKE TIME (ISL43142 ONLY)



$C_L$  includes fixture and stray capacitance.

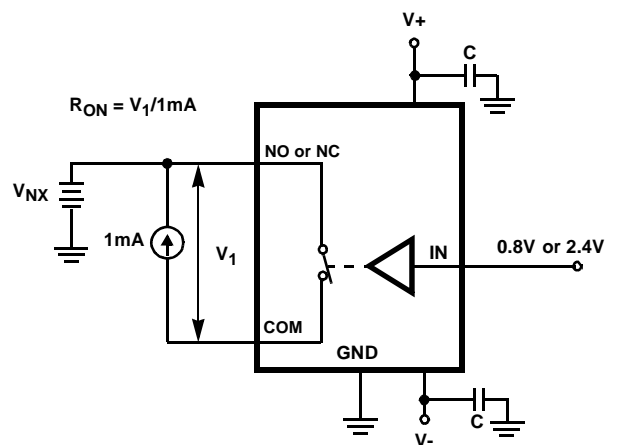
Reconfigure accordingly to test SW3 and SW4.

FIGURE 3B. TEST CIRCUIT



Repeat test for all switches.

FIGURE 4. OFF ISOLATION TEST CIRCUIT



Repeat test for all switches.

FIGURE 5.  $R_{ON}$  TEST CIRCUIT

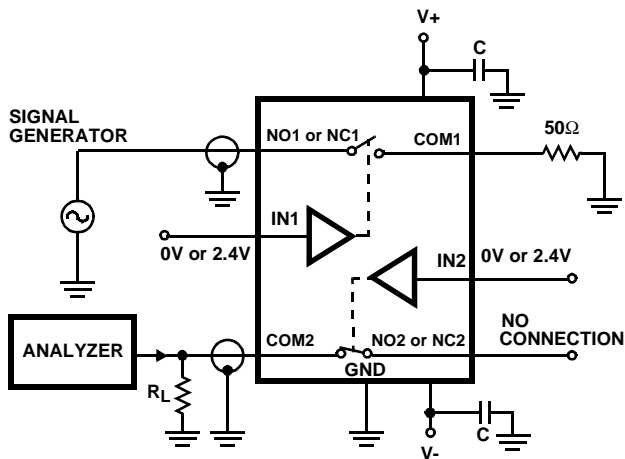


FIGURE 6. CROSSTALK TEST CIRCUIT

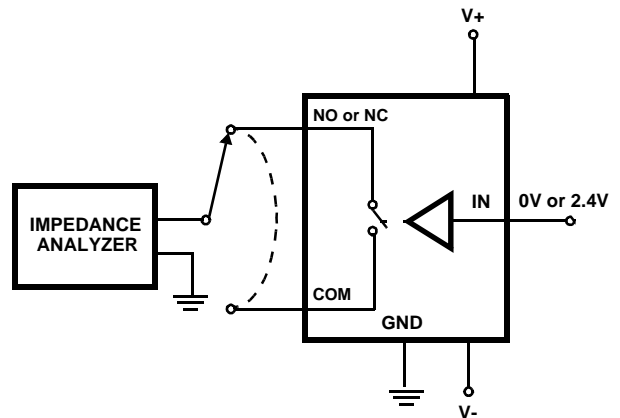


FIGURE 7. CAPACITANCE TEST CIRCUIT

## Detailed Description

The ISL43140–ISL43142 quad analog switches offer precise switching capability from a bipolar  $\pm 2V$  to  $\pm 6V$  or a single 2V to 12V supply with low on-resistance ( $50\Omega$ ) and high speed switching ( $t_{ON} = 40ns$ ,  $t_{OFF} = 15ns$ ). The devices are especially well suited to portable battery powered equipment thanks to the low operating supply voltage (2V), low power consumption ( $1\mu W$ ), low leakage currents (1nA max), and the tiny QFN packaging. High frequency applications also benefit from the wide bandwidth, and the very high off isolation and crosstalk rejection.

### Supply Sequencing And Overvoltage Protection

With any CMOS device, proper power supply sequencing is required to protect the device from excessive input currents which might permanently damage the IC. All I/O pins contain ESD protection diodes from the pin to  $V+$  and to  $V-$  (see Figure 8). To prevent forward biasing these diodes,  $V+$  and  $V-$  must be applied before any input signals, and input signal voltages must remain between  $V+$  and  $V-$ . If these conditions cannot be guaranteed, then one of the following two protection methods should be employed.

Logic inputs can easily be protected by adding a  $1k\Omega$  resistor in series with the input (see Figure 8). The resistor limits the input current below the threshold that produces permanent damage, and the sub-microamp input current produces an insignificant voltage drop during normal operation.

Adding a series resistor to the switch input defeats the purpose of using a low  $R_{ON}$  switch, so two small signal diodes can be added in series with the supply pins to provide overvoltage protection for all pins (see Figure 8). These additional diodes limit the analog signal from 1V below  $V+$  to 1V above  $V-$ . The low leakage current performance is unaffected by this approach, but the switch resistance may increase, especially at low supply voltages.

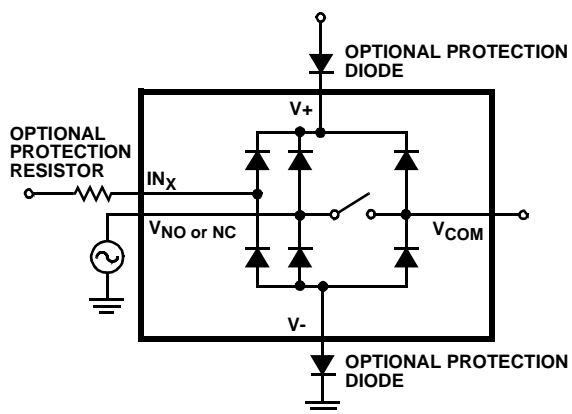


FIGURE 8. OVERVOLTAGE PROTECTION

### Power-Supply Considerations

The ISL4314X construction is typical of most CMOS analog switches, in that they have three supply pins:  $V+$ ,  $V-$ , and GND.  $V+$  and  $V-$  drive the internal CMOS switches and set their analog voltage limits, so there are no connections between the analog signal path and GND. Unlike switches with a 13V maximum supply voltage, the ISL4314X 15V maximum supply voltage provides plenty of room for the 10% tolerance of 12V supplies ( $\pm 6V$  or 12V single supply), as well as room for overshoot and noise spikes.

This family of switches performs equally well when operated with bipolar or single voltage supplies. The addition of the GND pin allows for asymmetrical bipolar supplies (e.g. +5V and -3V). The minimum recommended supply voltage is 2V or  $\pm 2V$ . It is important to note that the input signal range, switching times, and on-resistance degrade at lower supply voltages. Refer to the electrical specification tables and *Typical Performance Curves* for details.

$V+$  and GND power the internal logic (thus setting the digital switching point) and level shifters. The level shifters convert the logic levels to switched  $V+$  and  $V-$  signals to drive the analog switch gate terminals, so switch parameters - especially  $R_{ON}$  - are strongly influenced by  $V-$ .

### Logic-Level Thresholds

$V+$  and GND power the internal logic stages, so  $V-$  has no affect on logic thresholds. This switch family is TTL compatible (0.8V and 2.4V) over a  $V+$  supply range of 2.5V to 10V (see Figure 17). At 12V the  $V_{IH}$  level is about 2.7V, so for best results use a logic family the provides a  $V_{OH}$  greater than 3V.

The digital input stages draw supply current whenever the digital input voltage is not at one of the supply rails. Driving the digital input signals from GND to  $V+$  with a fast transition time minimizes power dissipation.

### High-Frequency Performance

In  $50\Omega$  systems, signal response is reasonably flat even past 100MHz (see Figure 18). Figure 18 also illustrates that the frequency response is very consistent over a wide  $V+$  range, and for varying analog signal levels.

An off switch acts like a capacitor and passes higher frequencies with less attenuation, resulting in signal feedthrough from a switch's input to its output. Off Isolation is the resistance to this feedthrough, while Crosstalk indicates the amount of feedthrough from one switch to another. Figure 19 details the high Off Isolation and Crosstalk rejection provided by this family. At 10MHz, off isolation is about 50dB in  $50\Omega$  systems, decreasing approximately 20dB per decade as frequency increases. Higher load impedances decrease Off Isolation and Crosstalk rejection due to the voltage divider action of the switch OFF impedance and the load impedance.

**Leakage Considerations**

Reverse ESD protection diodes are internally connected between each analog-signal pin and both V+ and V-. One of these diodes conducts if any analog signal exceeds V+ or V-.

Virtually all the analog leakage current comes from the ESD diodes to V+ or V-. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or V- and the analog signal. This means their leakages

will vary as the signal varies. The difference in the two diode leakages to the V+ and V- pins constitutes the analog-signal-path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of the same or opposite polarity. There is no connection between the analog signal paths and GND.

**Typical Performance Curves**  $T_A = 25^\circ\text{C}$ , Unless Otherwise Specified

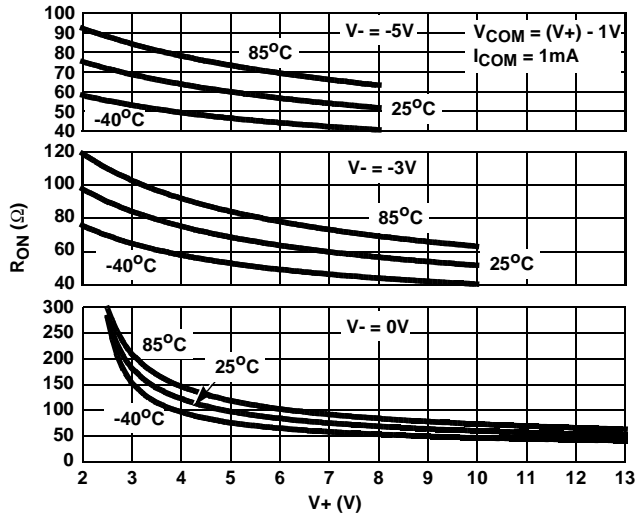


FIGURE 9. ON RESISTANCE vs POSITIVE SUPPLY VOLTAGE

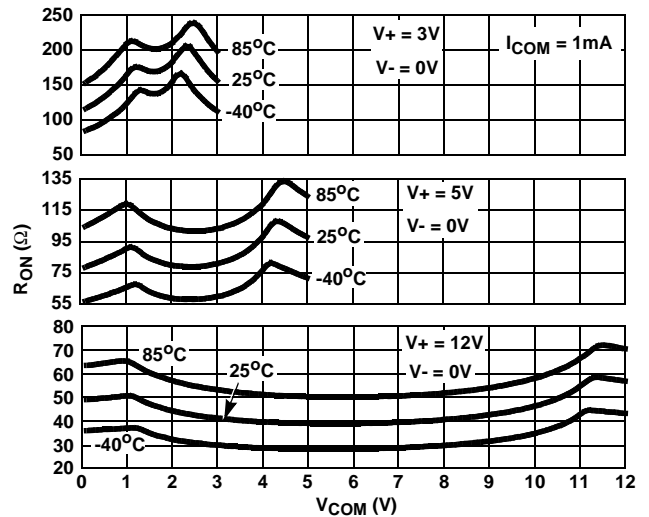


FIGURE 10. ON RESISTANCE vs SWITCH VOLTAGE

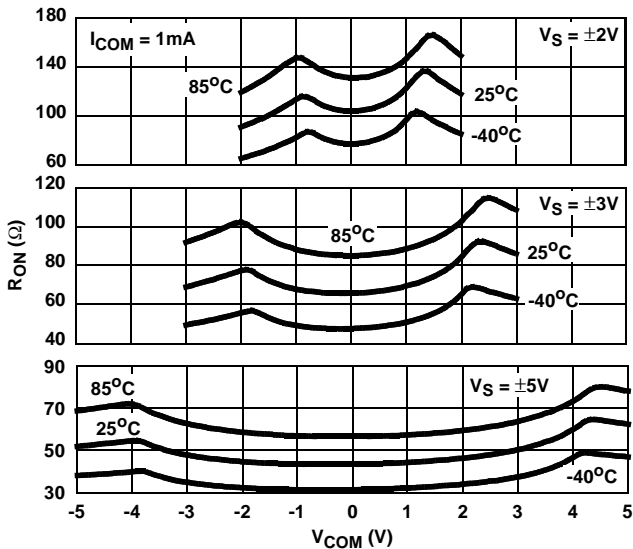


FIGURE 11. ON RESISTANCE vs SWITCH VOLTAGE

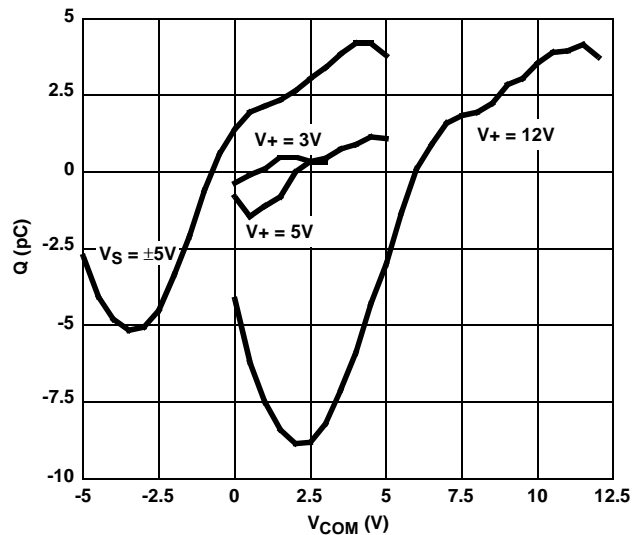


FIGURE 12. CHARGE INJECTION vs SWITCH VOLTAGE

Typical Performance Curves  $T_A = 25^\circ\text{C}$ , Unless Otherwise Specified (Continued)

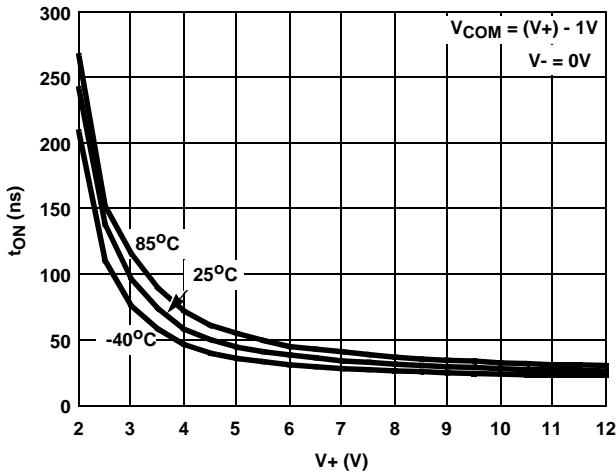


FIGURE 13. TURN - ON TIME vs POSITIVE SUPPLY VOLTAGE

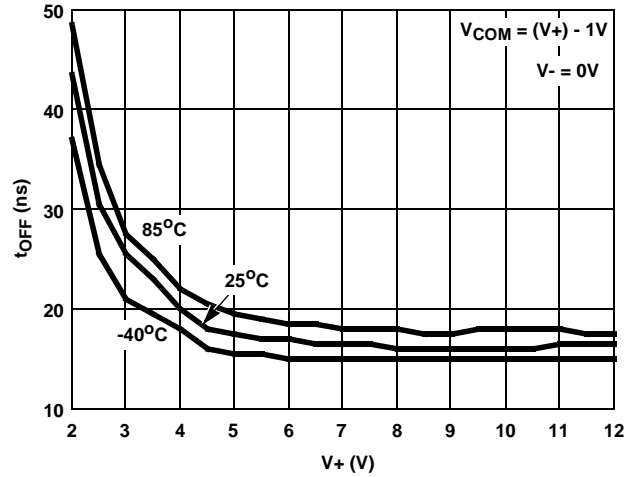


FIGURE 14. TURN - OFF TIME vs POSITIVE SUPPLY VOLTAGE

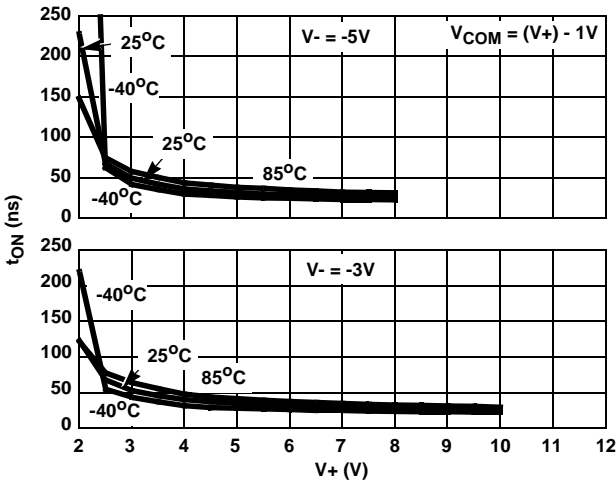


FIGURE 15. TURN - ON TIME vs POSITIVE SUPPLY VOLTAGE

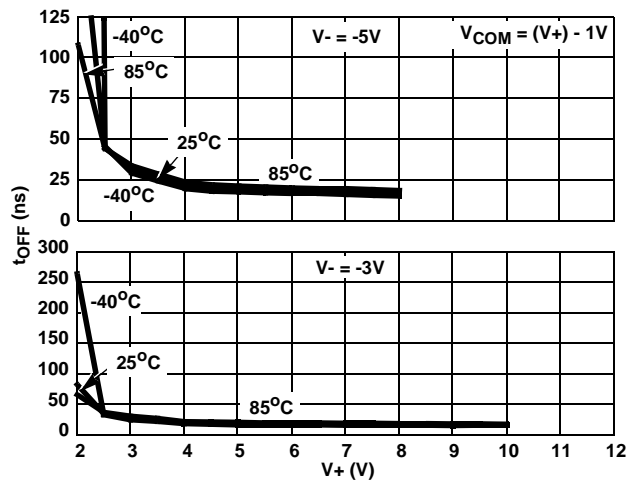


FIGURE 16. TURN - OFF TIME vs POSITIVE SUPPLY VOLTAGE

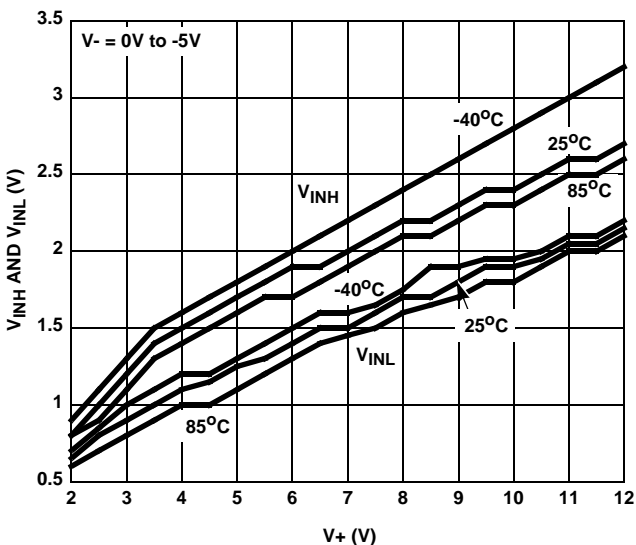


FIGURE 17. DIGITAL SWITCHING POINT vs POSITIVE SUPPLY VOLTAGE

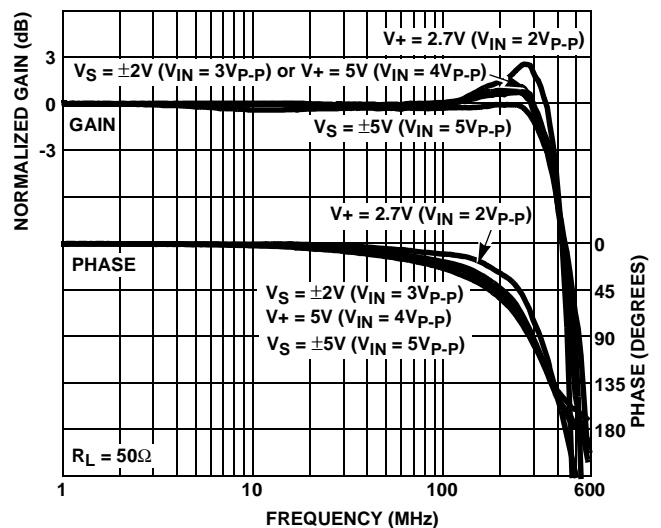


FIGURE 18. FREQUENCY RESPONSE

**Typical Performance Curves**  $T_A = 25^\circ\text{C}$ , Unless Otherwise Specified (Continued)

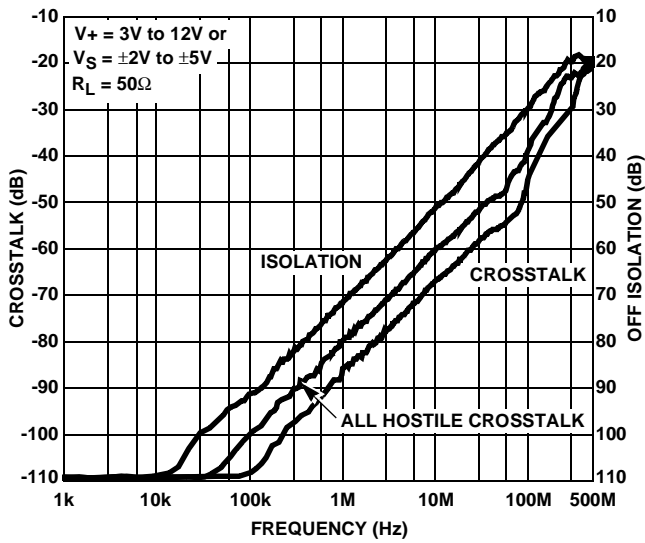


FIGURE 19. CROSSTALK AND OFF ISOLATION

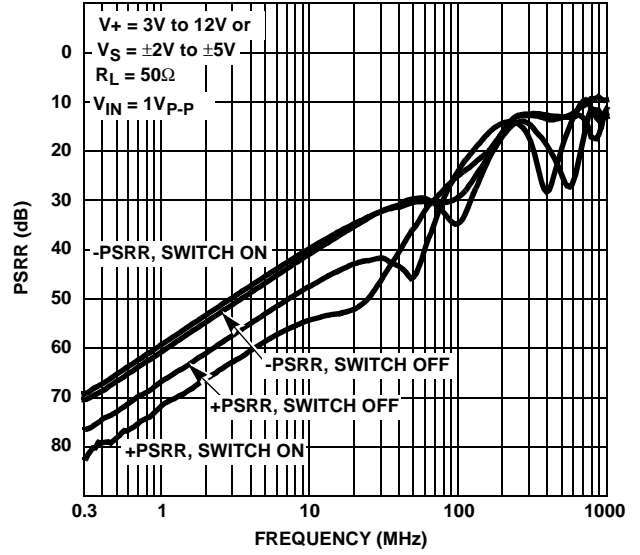


FIGURE 20.  $\pm$ PSRR vs FREQUENCY

**Die Characteristics**

**SUBSTRATE POTENTIAL (POWERED UP):**

$V_-$

**TRANSISTOR COUNT:**

ISL43140: 188

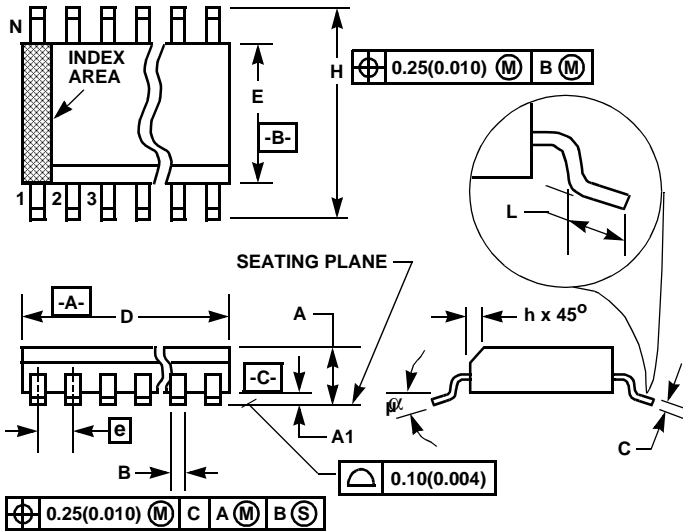
ISL43141: 188

ISL43142: 188

**PROCESS:**

Si Gate CMOS

**Small Outline Plastic Packages (SOIC)**



**M16.15 (JEDEC MS-012-AC ISSUE C)**  
**16 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE**

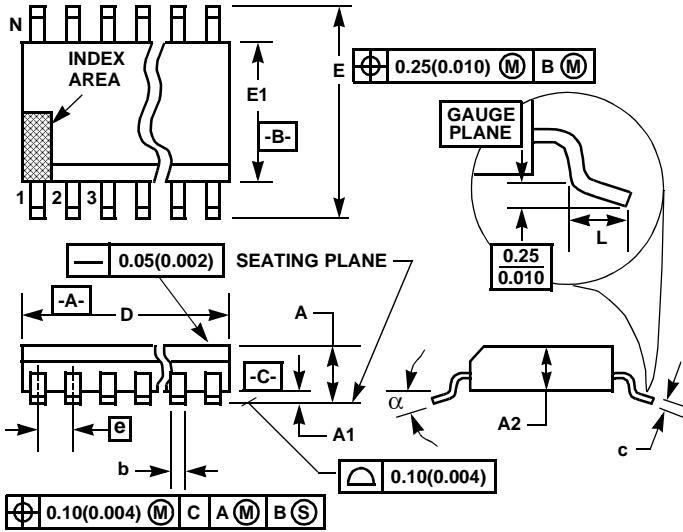
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.3859	0.3937	9.80	10.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
$\alpha$	0°	8°	0°	8°	-

**NOTES:**

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Rev. 0 12/93

Thin Shrink Small Outline Plastic Packages (TSSOP)



M16.173

16 LEAD THIN SHRINK SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.047	-	1.20	-
A1	0.002	0.006	0.05	0.15	-
A2	0.031	0.051	0.80	1.05	-
b	0.0075	0.0118	0.19	0.30	9
c	0.0035	0.0079	0.09	0.20	-
D	0.193	0.201	4.90	5.10	3
E1	0.169	0.177	4.30	4.50	4
e	0.026 BSC		0.65 BSC		-
E	0.246	0.256	6.25	6.50	-
L	0.0177	0.0295	0.45	0.75	6
N	16		16		7
α	0°	8°	0°	8°	-

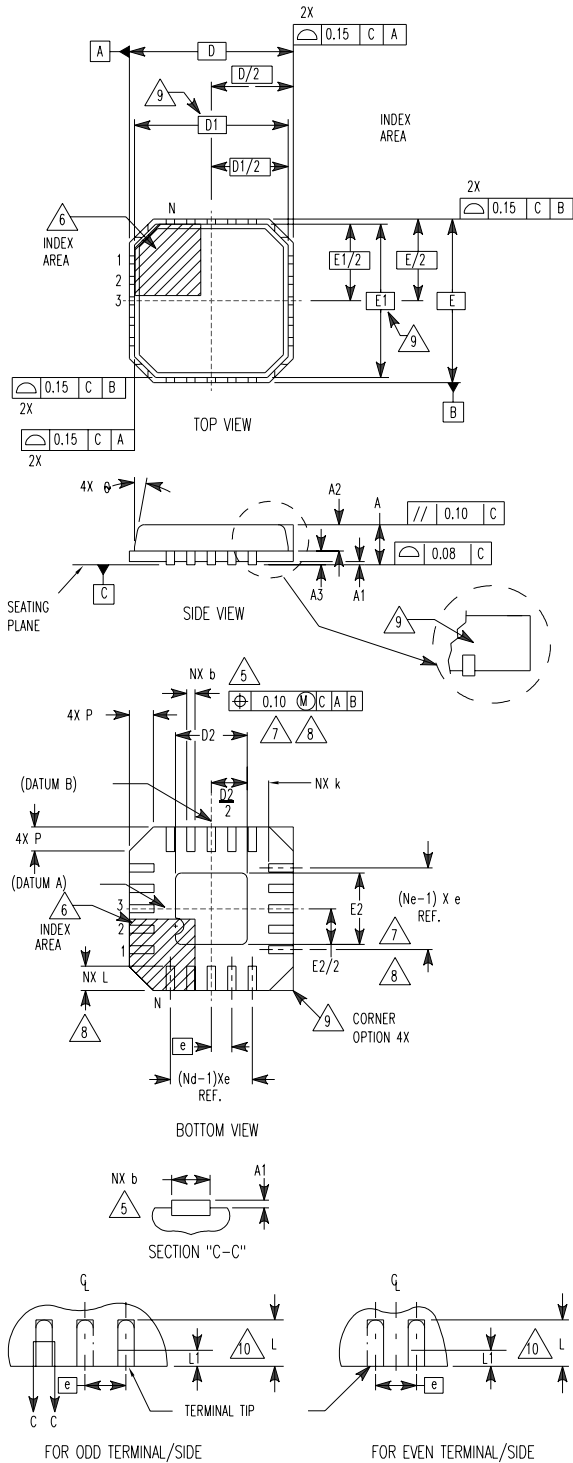
Rev. 0 6/98

NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-153-AB, Issue E.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E1" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of "b" dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact. (Angles in degrees)

**Quad Flat No-Lead Plastic Package (QFN)  
Micro Lead Frame Plastic Package (MLFP)**

**L16.3x3  
16 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE  
(COMPLIANT TO JEDEC MO-220VEED-2 ISSUE C)**



SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3	0.20 REF			9
b	0.18	0.23	0.30	5, 8
D	3.00 BSC			-
D1	2.75 BSC			9
D2	1.35	1.50	1.65	7, 8
E	3.00 BSC			-
E1	2.75 BSC			9
E2	1.35	1.50	1.65	7, 8
e	0.50 BSC			-
k	0.25	-	-	-
L	0.30	0.40	0.50	8
L1	-	-	0.15	10
N	16			2
Nd	4			3
Ne	4			3
P	-	-	0.60	9
θ	-	-	12	9

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**NOTES:**

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.

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