ISP1105/1106/1107

Advanced Universal Serial Bus transceivers

Rev. 06 — 30 November 2001 **Product data**

1. General description

The ISP1105/1106/1107 range of Universal Serial Bus (USB) transceivers are fully compliant with the *Universal Serial Bus Specification Rev. 1.1*. They are ideal for portable electronics devices such as mobile phones, digital still cameras, Personal Digital Assistants (PDA) and Information Appliances (IA).

They allow USB Application Specific ICs (ASICs) and Programmable Logic Devices (PLDs) with power supply voltages from 1.65 V to 3.6 V to interface with the physical layer of the Universal Serial Bus. They have an integrated 5 V to 3.3 V voltage regulator for direct powering via the USB supply V_{BUS}.

The ISP1105/1106/1107 range can be used as a USB device transceiver or a USB host transceiver. They can transmit and receive serial data at both full-speed (12 Mbit/s) and low-speed (1.5 Mbit/s) data rates.

ISP1105 allows single/differential input modes selectable by a MODE input and it is available in HBCC16 package. ISP1106 allows only differential input mode and is available in both TSSOP16 and HBCC16 packages. ISP1107 allows only single-ended input mode and is available in both TSSOP16 and HBCC16 packages.

2. Features

- Complies with *Universal Serial Bus Specification Rev. 1.1*
- Integrated bypassable 5 V to 3.3 V voltage regulator for powering via USB V_{BUS}
- V_{BUS} disconnection indication through VP and VM
- Used as a USB device transceiver or a USB host transceiver
- Supports full-speed (12 Mbit/s) and low-speed (1.5 Mbit/s) serial data rates
- Stable RCV output during SE0 condition
- Two single-ended receivers with hysteresis
- Low-power operation
- Supports an I/O voltage range from 1.65 V to 3.6 V
- 4 kV on-chip ESD protection
- Full industrial operating temperature range −40 to +85 °C
- Available in small TSSOP16 (except ISP1105) and HBCC16 packages.

3. Applications

- Portable electronic devices, such as:
  - Mobile phone
  - Digital still camera
  - Personal Digital Assistant (PDA)
  - Information Appliance (IA).

4. Ordering information

Table 1: Ordering information

Type number	Package		
	Name	Description	Version
ISP1105W[1] ISP1106W ISP1107W	HBCC16	plastic, heatsink bottom chip carrier; 16 terminals; body 3 × 3 × 0.65 mm	SOT639-2
ISP1106DH ISP1107DH	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

[1] The ground terminal of ISP1105W is connected to the exposed diepad (heatsink).

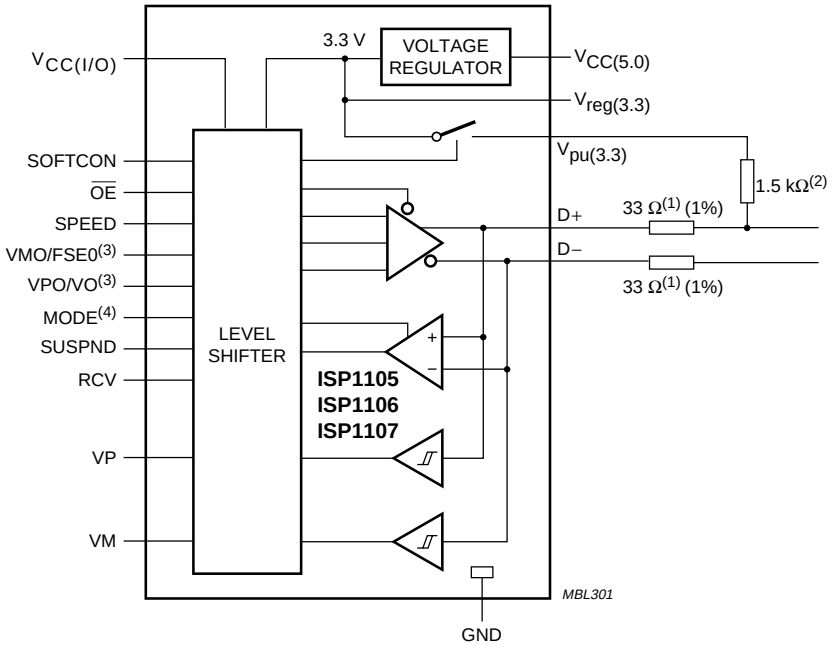
4.1 Ordering options

Table 2: Selection guide

Product	Package(s)	Description
ISP1105	HBCC16	Supports both single-ended and differential input modes[1]
ISP1106	TSSOP16 or HBCC16	Supports only the differential input mode[2]
ISP1107	TSSOP16 or HBCC16	Supports only the single-ended input mode[3]

[1] Refer to Table 5 and Table 6.
[2] Refer to Table 6.
[3] Refer to Table 5.

5. Functional diagram



(1) Use a 39 Ω resistor (1%) for a USB v2.0 compliant output impedance range.

(2) Connect to D− for low-speed operation.

(3) Pin function depends on device type see Section 7.2.

(4) Only for ISP1105.

Fig 1. Functional diagram (combined ISP1105, ISP1106 and ISP1107).

6. Pinning information

6.1 Pinning

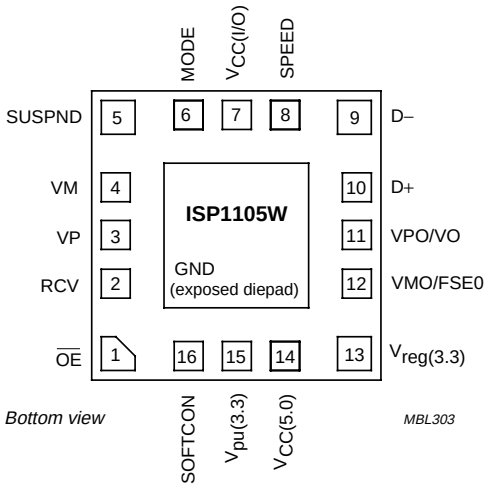
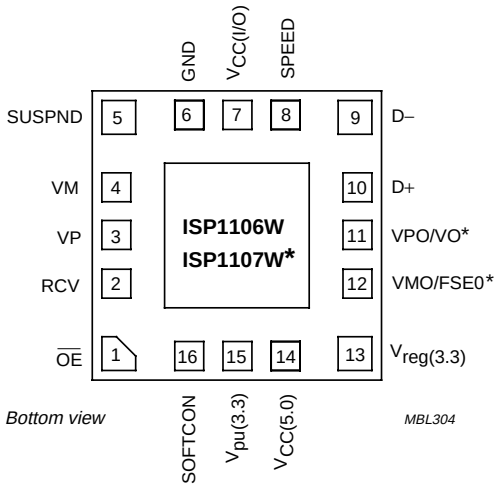
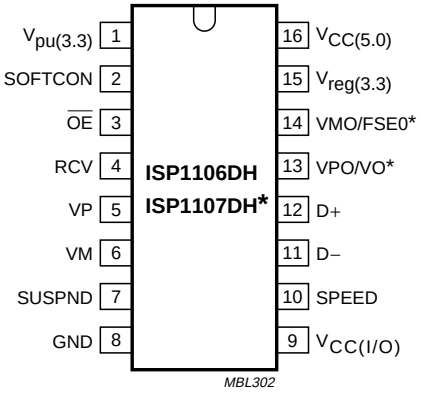


Fig 2. Pinning diagram HBCC16 (ISP1105).



The asterisk (*) denotes that the signal names VO and FSE0 apply to the ISP1107W.

Fig 3. Pinning diagram HBCC16 (ISP1106 and ISP1107).



The asterisk (*) denotes that the signal names VO and FSE0 apply to the ISP1107DH.

Fig 4. Pinning diagram TSSOP16 (ISP1106 and ISP1107).

6.2 Pin description

Table 3: Pin description

Symbol[1]	Pin			Type	Description
	ISP1105 HBCC16	ISP1106/7 HBCC16	ISP1106/7 TSSOP16		
$\overline{OE}$	1	1	3	I	input for output enable (CMOS level with respect to $V_{CC(I/O)}$, active LOW); enables the transceiver to transmit data on the USB bus
RCV	2	2	4	O	differential data receiver output (CMOS level with respect to $V_{CC(I/O)}$); driven LOW when input SUSPND is HIGH; the output state of RCV is preserved and stable during an SE0 condition
VP	3	3	5	O	single-ended D+ receiver output (CMOS level with respect to $V_{CC(I/O)}$); for external detection of single-ended zero (SE0), error conditions, speed of connected device; driven HIGH when no supply voltage is connected to $V_{CC(5.0)}$ and $V_{reg(3.3)}$
VM	4	4	6	O	single-ended D– receiver output (CMOS level with respect to $V_{CC(I/O)}$); for external detection of single-ended zero (SE0), error conditions, speed of connected device; driven HIGH when no supply voltage is connected to $V_{CC(5.0)}$ and $V_{reg(3.3)}$
SUSPND	5	5	7	I	suspend input (CMOS level with respect to $V_{CC(I/O)}$); a HIGH level enables low-power state while the USB bus is inactive and drives output RCV to a LOW level
MODE	6			I	mode input (CMOS level with respect to $V_{CC(I/O)}$); a HIGH level enables the differential input mode (VPO, VMO) whereas a LOW level enables a single-ended input mode (VO, FSE0). see Table 5 and Table 6
GND	-[2]	6	8	-	ground supply
$V_{CC(I/O)}$	7	7	9	-	supply voltage for digital I/O pins (1.65 to 3.6 V). When $V_{CC(I/O)}$ is not connected, the (D+, D–) pins are in three-state. This supply pin is totally independent of $V_{CC(5.0)}$ and $V_{reg(3.3)}$ and must never exceed the $V_{reg(3.3)}$ voltage.
SPEED	8	8	10	I	speed selection input (CMOS level with respect to $V_{CC(I/O)}$); adjusts the slew rate of differential data outputs D+ and D– according to the transmission speed: **LOW:** low-speed (1.5 Mbit/s) **HIGH:** full-speed (12 Mbit/s)
D–	9	9	11	AI/O	negative USB data bus connection (analog, differential); for low-speed mode connect to pin $V_{pu(3.3)}$ via a 1.5 kΩ resistor
D+	10	10	12	AI/O	positive USB data bus connection (analog, differential); for full-speed mode connect to pin $V_{pu(3.3)}$ via a 1.5 kΩ resistor
VPO/VO	11	11	13	I	driver data input (CMOS level with respect to $V_{CC(I/O)}$, Schmitt trigger); see Table 5 and Table 6
VMO/FSE0	12	12	14	I	driver data input (CMOS level with respect to $V_{CC(I/O)}$, Schmitt trigger); see Table 5 and Table 6

Table 3: Pin description…*continued*

Symbol[1]	Pin			Type	Description
	ISP1105 HBCC16	ISP1106/7 HBCC16	ISP1106/7 TSSOP16		
$V_{reg(3.3)}$	13	13	15	-	**Internal regulator option:** regulated supply voltage output (3.0 to 3.6 V) during 5 V operation; a decoupling capacitor of at least 0.1 µF is required **Regulator bypass option:** used as a supply voltage input for 3.3 V operation. (3.3 V ±10%)
$V_{CC(5.0)}$	14	14	16	-	**Internal regulator option:** supply voltage input (4.0 to 5.5 V); can be connected directly to USB supply V_{BUS} **Regulator bypass option:** connect to $V_{reg(3.3)}$
$V_{pu(3.3)}$	15	15	1	-	pull-up supply voltage (3.3 V ±10%); connect an external 1.5 kΩ resistor on D+ (full-speed) or D– (low-speed); pin function is controlled by input SOFTCON: **SOFTCON = LOW —** $V_{pu(3.3)}$ floating (high impedance); ensures zero pull-up current **SOFTCON = HIGH —** $V_{pu(3.3)}$ = 3.3 V; internally connected to $V_{reg(3.3)}$
SOFTCON	16	16	2	I	software controlled USB connection input; a HIGH level applies 3.3 V to pin $V_{pu(3.3)}$, which is connected to an external 1.5 kΩ pull-up resistor; this allows USB connect/disconnect signalling to be controlled by software

[1] Symbol names with an overscore (e.g. $\overline{NAME}$) indicate active LOW signals.

[2] Down bonded to the exposed diepad.

7. Functional description

7.1 Function selection

Table 4: Function table

SUSPND	$\overline{OE}$	(D+, D–)	RCV	VP/VM	Function
L	L	driving & receiving	active	active	normal driving (differential receiver active)
L	H	receiving[1]	active	active	receiving
H	L	driving	inactive[2]	active	driving during ‘suspend’[3] (differential receiver inactive)
H	H	high-Z[1]	inactive[2]	active	low-power state

[1] Signal levels on (D+, D–) are determined by other USB devices and external pull-up/down resistors.

[2] In ‘suspend’ mode (SUSPND = HIGH) the differential receiver is inactive and output RCV is always LOW. Out-of-suspend (‘K’) signalling is detected via the single-ended receivers VP and VM.

[3] During suspend, the slew-rate control circuit of low-speed operation is disabled. The (D+, D–) lines are still driven to their intended states, without slew-rate control. This is permitted because driving during suspend is used to signal remote wake-up by driving a ‘K’ signal (one transition from idle to ‘K’ state) for a period of 1 to 15 ms.

7.2 Operating functions

Table 5: Driving function using single-ended input data interface ($\overline{OE}$ = L) [for ISP1107 and ISP1105 (MODE = L)]

FSE0	VO	Data
L	L	differential logic 0
L	H	differential logic 1
H	L	SE0
H	H	SE0

Table 6: Driving function using differential input data interface ($\overline{OE}$ = L) [for ISP1106 and ISP1105 (MODE = H)]

VMO	VPO	Data
L	L	SE0
L	H	differential logic 1
H	L	differential logic 0
H	H	illegal state

Table 7: Receiving function ($\overline{OE}$ = H)

(D+, D–)	RCV	VP[1]	VM[1]
differential logic 0	L	L	H
differential logic 1	H	H	L
SE0	RCV*[2]	L	L

[1] VP = VM = H indicates the sharing mode ($V_{CC(5.0)}$/$V_{reg(3.3)}$ is disconnected).

[2] RCV* denotes the signal level on output RCV just before SE0 state occurs. This level is stable during the SE0 period.

7.3 Power supply configurations

The ISP1105/1106/1107 can be used with different power supply configurations, which can be changed dynamically. An overview is given in Table 9.

Normal mode — Both $V_{CC(I/O)}$ and $V_{CC(5.0)}$ or ($V_{CC(5.0)}$ and $V_{reg(3.3)}$) are connected. For 5 V operation, $V_{CC(5.0)}$ is connected to a 5 V source (4.0 to 5.5 V). The internal voltage regulator then produces 3.3 V for the USB connections. For 3.3 V operation, both $V_{CC(5.0)}$ and $V_{reg(3.3)}$ are connected to a 3.3 V source (3.0 to 3.6 V). $V_{CC(I/O)}$ is independently connected to a voltage source (1.65 V to 3.6 V), depending on the supply voltage of the external circuit.

Disable mode — $V_{CC(I/O)}$ is not connected, $V_{CC(5.0)}$ or ($V_{CC(5.0)}$ and $V_{reg(3.3)}$) are connected. In this mode, the internal circuits of the ISP1105/1106/1107 ensure that the (D+, D–) pins are in three-state and the power consumption drops to the low-power (suspended) state level. Some hysteresis is built into the detection of $V_{CC(I/O)}$ lost.

Sharing mode — $V_{CC(I/O)}$ is connected, ($V_{CC(5.0)}$ and $V_{reg(3.3)}$) are not connected. In this mode, the (D+, D–) pins are made three-state and the ISP1105/1106/1107 allows external signals of up to 3.6 V to share the (D+, D–) lines. The internal circuits of the ISP1105/1106/1107 ensure that virtually no current (maximum 10 μA) is drawn via the (D+, D–) lines. The power consumption through pin $V_{CC(I/O)}$ drops to the

low-power (suspended) state level. Both the VP and VM pins are driven HIGH to indicate this mode. Pin RCV is made LOW. Some hysteresis is built into the detection of $V_{reg(3.3)}$ lost.

Table 8: Pin states in Disable or Sharing mode

Pins	Disable mode state	Sharing mode state
$V_{CC(5.0)}/V_{reg(3.3)}$	5 V input / 3.3 V output 3.3 V input / 3.3 V input	not present
$V_{CC(I/O)}$	not present	1.65 V to 3.6 V input
$V_{pu(3.3)}$	high impedance (off)	high impedance (off)
(D+, D–)	high impedance	high impedance
(VP, VM)	invalid[1]	H
RCV	invalid[1]	L
Inputs (VO/VPO, FSE0/VMO, SPEED, MODE[2], SUSPND, $\overline{OE}$, SOFTCON)	high impedance	high impedance

[1] High impedance or driven LOW.

[2] ISP1105 only.

Table 9: Power supply configuration overview

$V_{CC(5.0)}$ or $V_{reg(3.3)}$	$V_{CC(I/O)}$	Configuration	Special characteristics
connected	connected	Normal mode	-
connected	not connected	Disable mode	(D+, D–) and $V_{pu(3.3)}$ high impedance; VP, VM, RCV: invalid[1]
not connected	connected	Sharing mode	(D+, D–) and $V_{pu(3.3)}$ high impedance; VP, VM driven HIGH; RCV driven LOW

[1] High impedance or driven LOW.

7.4 Power supply input options

The ISP1105/1106/1107 range has two power supply input options:

Internal regulator — $V_{CC(5.0)}$ is connected to 4.0 to 5.5 V. The internal regulator is used to supply the internal circuitry with 3.3 V (nominal). The $V_{reg(3.3)}$ pin becomes a 3.3 V output reference.

Regulator bypass — $V_{CC(5.0)}$ and $V_{reg(3.3)}$ are connected to the same supply. The internal regulator is bypassed and the internal circuitry is supplied directly from the $V_{reg(3.3)}$ power supply. The voltage range is 3.0 to 3.6 V to comply with the USB specification.

The supply voltage range for each input option is specified in Table 10.

Table 10: Power supply input options

Input option	$V_{CC(5.0)}$	$V_{reg(3.3)}$	$V_{CC(I/O)}$
Internal regulator	supply input for internal regulator (4.0 to 5.5 V)	voltage reference output (3.3 V, 300 µA)	supply input for digital I/O pins (1.65 V to 3.6 V)
Regulator bypass	connected to $V_{reg(3.3)}$ with maximum voltage drop of 0.3 V (2.7 to 3.6 V)	supply input (3.0 V to 3.6 V)	supply input for digital I/O pins (1.65 V to 3.6 V)

8. Limiting values

Table 11: Absolute maximum ratings

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(5.0)}$	supply voltage		–0.5	+6.0	V
$V_{CC(I/O)}$	I/O supply voltage		–0.5	+4.6	V
$V_{reg(3.3)}$	regulated supply voltage		–0.5	+4.6	V
V_I	DC input voltage		–0.5	$V_{CC(I/O)}$ + 0.5	V
$I_{latchup}$	latch-up current	V_I = –1.8 to 5.4 V	-	100	mA
V_{esd}	electrostatic discharge voltage[1]	I_{LI} < 1 µA			
		pins D+, D–, $V_{CC(5.0)}$, $V_{reg(3.3)}$, GND	-	±4000	V
		other pins	-	±2000	V
T_{stg}	storage temperature		–40	+125	°C

[1] Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ resistor (Human Body Model). Refer to *EIA/JEDEC Standard specification EIA/JESD22-A114-A*.

Table 12: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC(5.0)}$	supply voltage (Internal regulator option)	5 V operation	4.0	5.0	5.5	V
$V_{reg(3.3)}$	supply voltage (Regulator bypass option)	3.3 V operation	3.0	3.3	3.6	V
$V_{CC(I/O)}$	I/O supply voltage		1.65	-	3.6	V
V_I	input voltage		0	-	$V_{CC(I/O)}$	V
$V_{I(AI/O)}$	input voltage on analog I/O pins (D+/D–)		0	-	3.6	V
T_{amb}	operating ambient temperature		–40	-	+85	°C

9. Static characteristics

Table 13: Static characteristics: supply pins

V_{CC} = 4.0 to 5.5 V or $V_{reg(3.3)}$ = 3.0 to 3.6 V; $V_{CC(I/O)}$ = 1.65 to 3.6 V; V_{GND} = 0 V; see Table 10 for valid voltage level combinations; T_{amb} = −40 to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{reg(3.3)}$	regulated supply voltage output	Internal regulator option; $I_{load} \leq 300$ µA	[1]	3.0[2]	3.3	3.6	V
I_{CC}	operating supply current	full-speed transmitting and receiving at 12 Mbit/s; C_L = 50 pF on D+/D−		-	4	8[3]	mA
$I_{CC(I/O)}$	operating I/O supply current	full-speed transmitting and receiving at 12 Mbit/s		-	1	2[3]	mA
$I_{CC(idle)}$	supply current during full-speed idle and SE0	full-speed idle: $V_{D+} > 2.7$ V, $V_{D-} < 0.3$ V; SE0: $V_{D+} < 0.3$ V, $V_{D-} < 0.3$ V	[4]	-	-	500	µA
$I_{CC(I/O)(static)}$	static I/O supply current	full-speed idle, SE0 or suspend		-	-	20	µA
$I_{CC(susp)}$	suspend supply current	SUSPND = HIGH	[4]	-	-	20	µA
$I_{CC(dis)}$	disable mode supply current	$V_{CC(I/O)}$ not connected	[4]	-	-	20	µA
$I_{CC(I/O)(sharing)}$	sharing mode I/O supply current	$V_{CC(5.0)}$ or $V_{reg(3.3)}$ not connected		-	-	20	µA
$I_{Dx(sharing)}$	sharing mode load current on pins D+ and D−	$V_{CC(5.0)}$ or $V_{reg(3.3)}$ not connected; SOFTCON = LOW; V_{Dx} = 3.6 V		-	-	10	µA
$V_{th(reg3.3)}$	regulated supply voltage detection threshold	$1.65 \text{ V} \leq V_{CC(I/O)} \leq V_{reg(3.3)}$; $2.7 \text{ V} \leq V_{reg(3.3)} \leq 3.6$ V					
		supply lost		-	-	0.8	V
		supply present		2.4[5]	-	-	V
$V_{hys(reg3.3)}$	regulated supply voltage detection hysteresis	$V_{CC(I/O)}$ = 1.8 V		-	0.45	-	V
$V_{th(I/Osup)}$	I/O supply voltage detection threshold	$V_{reg(3.3)}$ = 2.7 to 3.6 V					
		supply lost		-	-	0.5	V
		supply present		1.4	-	-	V
$V_{hys(I/Osup)}$	I/O supply voltage detection hysteresis	$V_{reg(3.3)}$ = 3.3 V		-	0.45	-	V

[1] I_{load} includes the pull-up resistor current via pin $V_{pu(3.3)}$.

[2] In ‘suspend’ mode, the minimum voltage is 2.7 V.

[3] Characterized only, not tested in production.

[4] Excluding any load current and $V_{pu(3.3)}/V_{sw}$ source current to the 1.5 kΩ and 15 kΩ pull-up and pull-down resistors (200 µA typ.).

[5] When $V_{CC(I/O)} < 2.7$ V, the minimum value for $V_{th(reg3.3)(present)}$ is 2.0 V.

Table 14: Static characteristics: digital pins

$V_{CC(I/O)}$ = 1.65 to 3.6 V; V_{GND} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC(I/O)}$ = 1.65 to 3.6 V						
Input levels						
V_{IL}	LOW-level input voltage		-	-	$0.3V_{CC(I/O)}$	V
V_{IH}	HIGH-level input voltage		$0.6V_{CC(I/O)}$	-	-	V
Output levels						
V_{OL}	LOW-level output voltage	I_{OL} = 100 µA	-	-	0.15	V
		I_{OL} = 2 mA	-	-	0.4	V
V_{OH}	HIGH-level output voltage	I_{OH} = 100 µA	$V_{CC(I/O)}$ − 0.15	-	-	V
		I_{OH} = 2 mA	$V_{CC(I/O)}$ − 0.4	-	-	V
Leakage current						
I_{LI}	input leakage current		-	-	±1	µA
Example 1: $V_{CC(I/O)}$ = 1.8 V ± 0.15 V						
Input levels						
V_{IL}	LOW-level input voltage		-	-	0.5	V
V_{IH}	HIGH-level input voltage		1.2	-	-	V
Output levels						
V_{OL}	LOW-level output voltage	I_{OL} = 100 µA	-	-	0.15	V
		I_{OL} = 2 mA	-	-	0.4	V
V_{OH}	HIGH-level output voltage	I_{OH} = 100 µA	1.5	-	-	V
		I_{OH} = 2 mA	1.25	-	-	V
Example 2: $V_{CC(I/O)}$ = 2.5 V ± 0.2 V						
Input levels						
V_{IL}	LOW-level input voltage		-	-	0.7	V
V_{IH}	HIGH-level input voltage		1.7	-	-	V
Output levels						
V_{OL}	LOW-level output voltage	I_{OL} = 100 µA	-	-	0.15	V
		I_{OL} = 2 mA	-	-	0.4	V
V_{OH}	HIGH-level output voltage	I_{OH} = 100 µA	2.15	-	-	V
		I_{OH} = 2 mA	1.9	-	-	V
Example 3: $V_{CC(I/O)}$ = 3.3 V ± 0.3 V						
Input levels						
V_{IL}	LOW-level input voltage		-	-	0.9	V
V_{IH}	HIGH-level input voltage		2.15	-	-	V
Output levels						
V_{OL}	LOW-level output voltage	I_{OL} = 100 µA	-	-	0.15	V
		I_{OL} = 2 mA	-	-	0.4	V
V_{OH}	HIGH-level output voltage	I_{OH} = 100 µA	2.85	-	-	V
		I_{OH} = 2 mA	2.6	-	-	V
Capacitance						
C_{IN}	input capacitance	pin to GND	-	-	10	pF

Table 15: Static characteristics: analog I/O pins (D+, D–)

V_{CC} = 4.0 to 5.5 V or $V_{reg(3.3)}$ = 3.0 to 3.6 V; V_{GND} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Input levels							
Differential receiver							
V_{DI}	differential input sensitivity	$\|V_{I(D+)} - V_{I(D-)}\|$		0.2	-	-	V
V_{CM}	differential common mode voltage	includes V_{DI} range		0.8	-	2.5	V
Single-ended receiver							
V_{IL}	LOW-level input voltage			-	-	0.8	V
V_{IH}	HIGH-level input voltage			2.0	-	-	V
V_{hys}	hysteresis voltage			0.4	-	0.7	V
Output levels							
V_{OL}	LOW-level output voltage	R_L = 1.5 kΩ to +3.6 V		-	-	0.3	V
V_{OH}	HIGH-level output voltage	R_L = 15 kΩ to GND		2.8[1]	-	3.6	V
Leakage current							
I_{LZ}	OFF-state leakage current			-	-	±1	µA
Capacitance							
C_{IN}	transceiver capacitance	pin to GND		-	-	20	pF
Resistance							
Z_{DRV}	driver output impedance	steady-state drive	[2]	34	39	44	Ω
Z_{DRV2}	driver output impedance for USB 2.0	steady-state drive	[3]	40.5	45	49.5	Ω
Z_{INP}	input impedance			10	-	-	MΩ
R_{SW}	internal switch resistance at pin $V_{pu(3.3)}$			-	-	10	Ω
Termination							
V_{TERM}[4]	termination voltage for upstream port pull-up (R_{PU})			3.0[5]	-	3.6	V

[1] $V_{OH(min)} = V_{reg(3.3)} - 0.2$ V.

[2] Includes external resistors of 33 Ω ±1% on both D+ and D–.

[3] Includes external resistors of 39 Ω ±1% on both D+ and D–. This range complies with *Universal Serial Bus Specification Rev. 2.0*.

[4] This voltage is available at pins $V_{reg(3.3)}$ and $V_{pu(3.3)}$.

[5] In ‘suspend’ mode the minimum voltage is 2.7 V.

10. Dynamic characteristics

Table 16: Dynamic characteristics: analog I/O pins (D+, D–)[1]

V_{CC} = 4.0 to 5.5 V or $V_{reg(3.3)}$ = 3.0 to 3.6 V; $V_{CC(I/O)}$ = 1.65 to 3.6 V; V_{GND} = 0 V; see Table 10 for valid voltage level combinations; T_{amb} = −40 to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Driver characteristics							
Full-speed mode (SPEED = HIGH)							
t_{FR}	rise time	C_L = 50 to 125 pF; 10 to 90% of $\|V_{OH} - V_{OL}\|$; see Figure 5		4	-	20	ns
t_{FF}	fall time	C_L = 50 to 125 pF; 90 to 10% of $\|V_{OH} - V_{OL}\|$; see Figure 5		4	-	20	ns
FRFM	differential rise/fall time matching (t_{FR}/t_{FF})	excluding the first transition from Idle state		90	-	111.1	%
V_{CRS}	output signal crossover voltage	excluding the first transition from Idle state; see Figure 8	[2]	1.3	-	2.0	V
Low-speed mode (SPEED = LOW)							
t_{LR}	rise time	C_L = 50 to 600 pF; 10 to 90% of $\|V_{OH} - V_{OL}\|$; see Figure 5		75	-	300	ns
t_{LF}	fall time	C_L = 50 to 600 pF; 90 to 10% of $\|V_{OH} - V_{OL}\|$; see Figure 5		75	-	300	ns
LRFM	differential rise/fall time matching (t_{LR}/t_{LF})	excluding the first transition from Idle state		80	-	125	%
V_{CRS}	output signal crossover voltage	excluding the first transition from idle state; see Figure 8	[2]	1.3	-	2.0	V
Driver timing							
Full-speed mode (SPEED = HIGH)							
$t_{PLH(drv)}$	driver propagation delay	LOW-to-HIGH; see Figure 8		-	-	18	ns
$t_{PHL(drv)}$	(VO/VPO, FSE0/VMO to D+,D–)	HIGH-to-LOW; see Figure 8		-	-	18	ns
t_{PHZ}	driver disable delay	HIGH-to-OFF; see Figure 6		-	-	15	ns
t_{PLZ}	($\overline{OE}$ to D+,D–)	LOW-to-OFF; see Figure 6		-	-	15	ns
t_{PZH}	driver enable delay	OFF-to-HIGH; see Figure 6		-	-	15	ns
t_{PZL}	($\overline{OE}$ to D+,D–)	OFF-to-LOW; see Figure 6		-	-	15	ns
Low-speed mode (SPEED = LOW)							

Not specified: low-speed delay timings are dominated by the slow rise/fall times t_{LR} and t_{LF}.

Table 16: Dynamic characteristics: analog I/O pins (D+, D–)[1] *…continued*

V_{CC} = 4.0 to 5.5 V or $V_{reg(3.3)}$ = 3.0 to 3.6 V; $V_{CC(I/O)}$ = 1.65 to 3.6 V; V_{GND} = 0 V; see Table 10 for valid voltage level combinations; T_{amb} = −40 to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Receiver timings (full-speed and low-speed mode)						
Differential receiver						
$t_{PLH(rcv)}$	propagation delay	LOW-to-HIGH; see Figure 7	-	-	15	ns
$t_{PHL(rcv)}$	(D+,D– to RCV)	HIGH-to-LOW; see Figure 7	-	-	15	ns
Single-ended receiver						
$t_{PLH(se)}$	propagation delay	LOW-to-HIGH; see Figure 7	-	-	18	ns
$t_{PHL(se)}$	(D+,D– to VP, VM)	HIGH-to-LOW; see Figure 7	-	-	18	ns

[1] Test circuit: see Figure 11.

[2] Characterized only, not tested. Limits guaranteed by design.

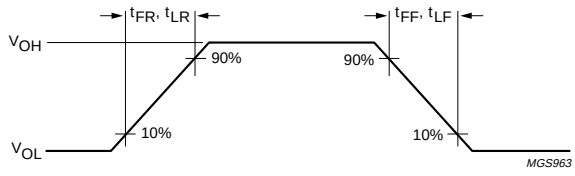


Fig 5. Rise and fall times.

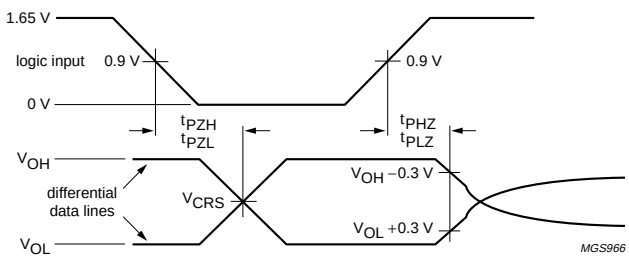


Fig 6. Timing of $\overline{OE}$ to D+, D–.

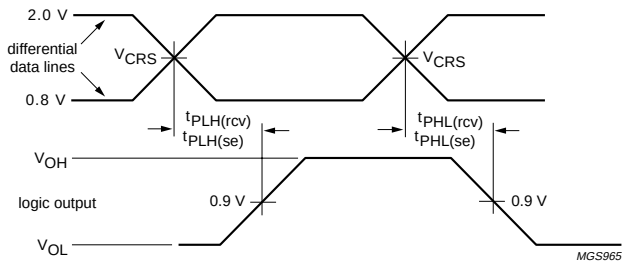


Fig 7. Timing of D+, D– to RCV, VP, VM.

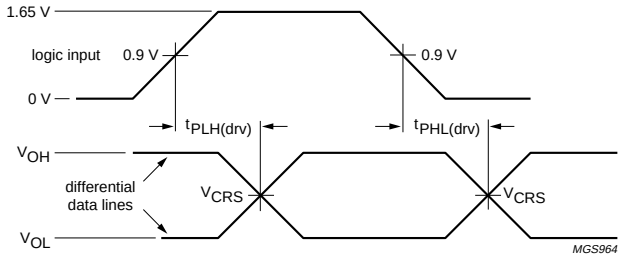
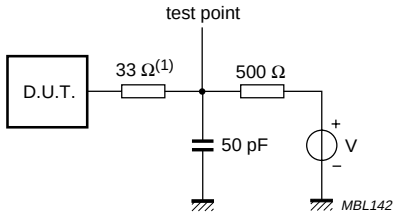


Fig 8. Timing of VO/VPO, FSE0/VMO to D+, D–.

11. Test information



V = 0 V for t_{PZH}, t_{PHZ}

V = $V_{reg(/3.3)}$ for t_{PZL}, t_{PLZ}

(1) Complies with USB 1.1. For USB 2.0 a resistor of 39 Ω must be used.

Fig 9. Load for enable and disable times.

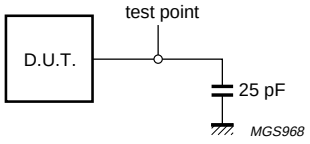
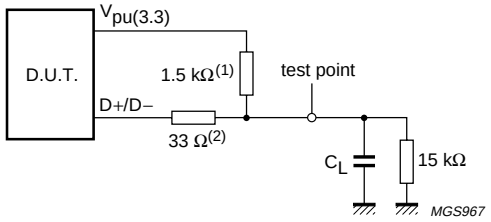


Fig 10. Load for VM, VP and RCV.



Load capacitance:

C_L = 50 pF or 125 pF (full-speed mode, minimum or maximum timing)

C_L = 50 pF or 600 pF (low-speed mode, minimum or maximum timing)

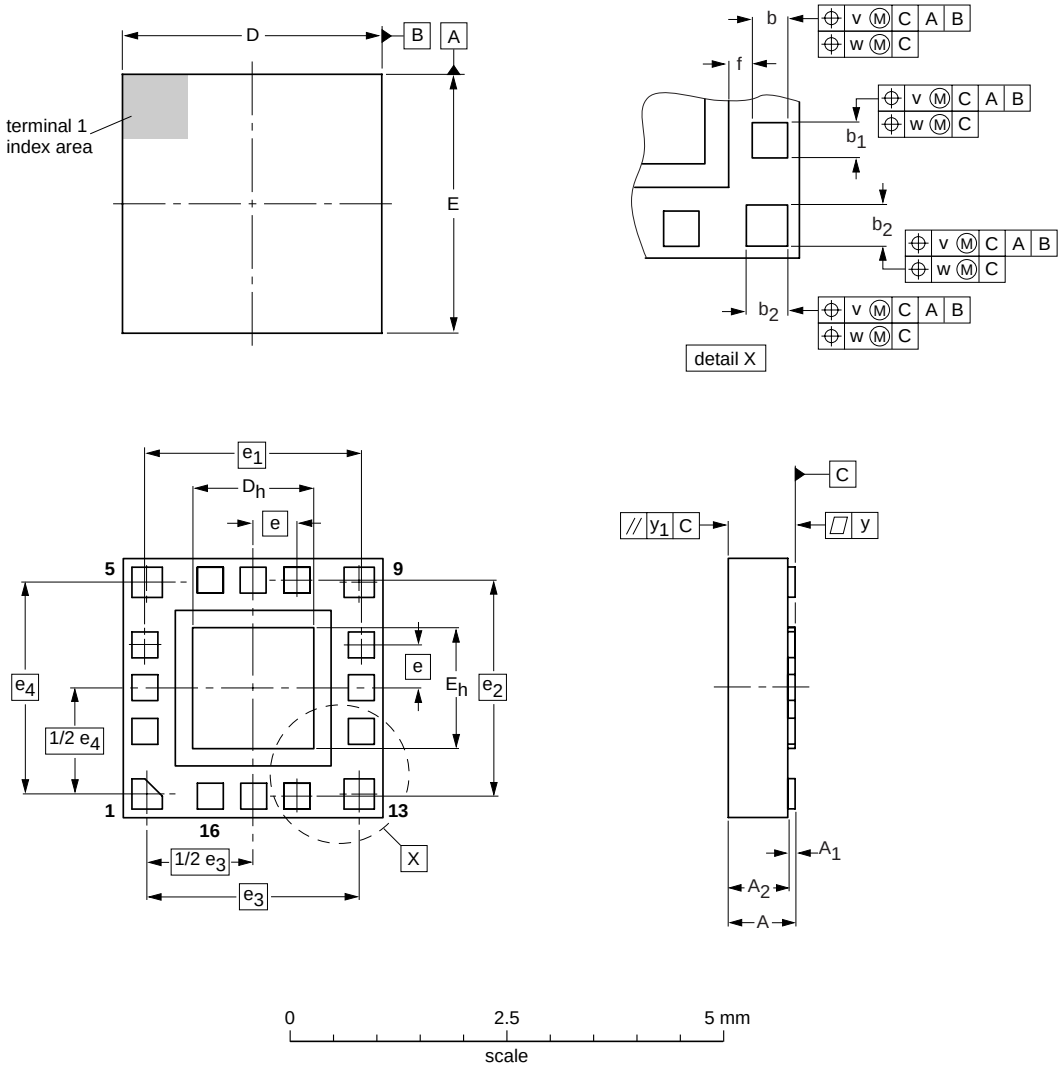
(1) Full-speed mode: connected to D+, low-speed mode: connected to D–.

(2) Complies with USB 1.1. For USB 2.0 a resistor of 39 Ω must be used.

Fig 11. Load for D+, D–.

12. Package outline

HBCC16: plastic thermal enhanced bottom chip carrier; 16 terminals; body 3 x 3 x 0.65 mm **SOT639-2**



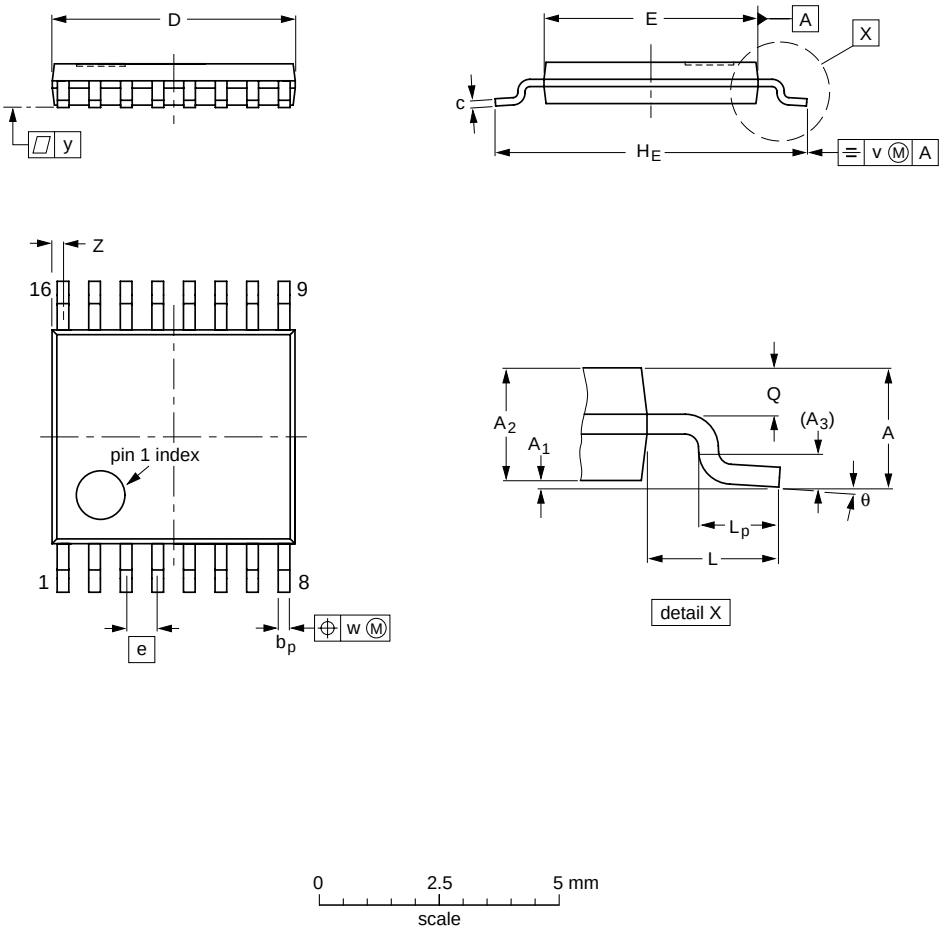
DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	b	b_1	b_2	D	D_h	E	E_h	e	e_1	e_2	e_3	e_4	f	v	w	y	y_1
mm	0.8	0.10 0.05	0.7 0.6	0.33 0.27	0.33 0.27	0.38 0.32	3.1 2.9	1.45 1.35	3.1 2.9	1.45 1.35	0.5	2.5	2.5	2.45	2.45	0.23 0.17	0.08	0.1	0.05	0.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT639-2		MO-217				01-11-13

Fig 12. HBCC16 package outline.

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT403-1		MO-153				~~95-04-04~~ 99-12-27

Fig 13. TSSOP16 package outline.

13. Packaging

The ISP1105/1106/1107W (HBCC16 package) is delivered on a Type A carrier tape, see Figure 14. The tape dimensions are given in Table 17.

The reel diameter is 330 mm. The reel is made of polystyrene (PS) and is not designed for use in a baking process.

The cumulative tolerance of 10 successive sprocket holes is ±0.02 mm. The camber must not exceed 1 mm in 100 mm.

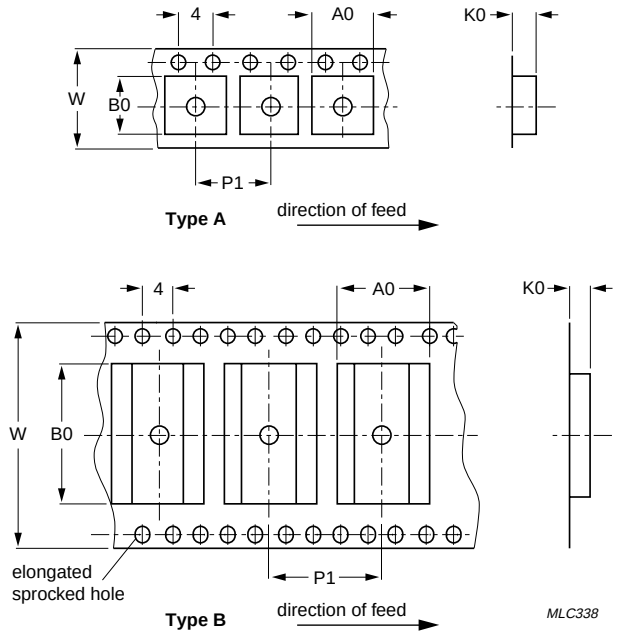


Fig 14. Carrier tape dimensions.

Table 17: Type A carrier tape dimensions for ISP1105/1106/1107W

Dimension	Value	Unit
A_0	3.3	mm
B_0	3.3	mm
K_0	1.1	mm
P_1	8.0	mm
W	12.0 ±0.3	mm

14. Soldering

14.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

14.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C small/thin packages.

14.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C. A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

14.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

14.5 Package related soldering information

Table 18: Suitability of surface mount IC packages for wave and reflow soldering methods

Package	Soldering method	
	Wave	Reflow[1]
BGA, HBGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, SMS	not suitable[2]	suitable
PLCC[3], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[3][4]	suitable
SSOP, TSSOP, VSO	not recommended[5]	suitable

[1] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[2] These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).

[3] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

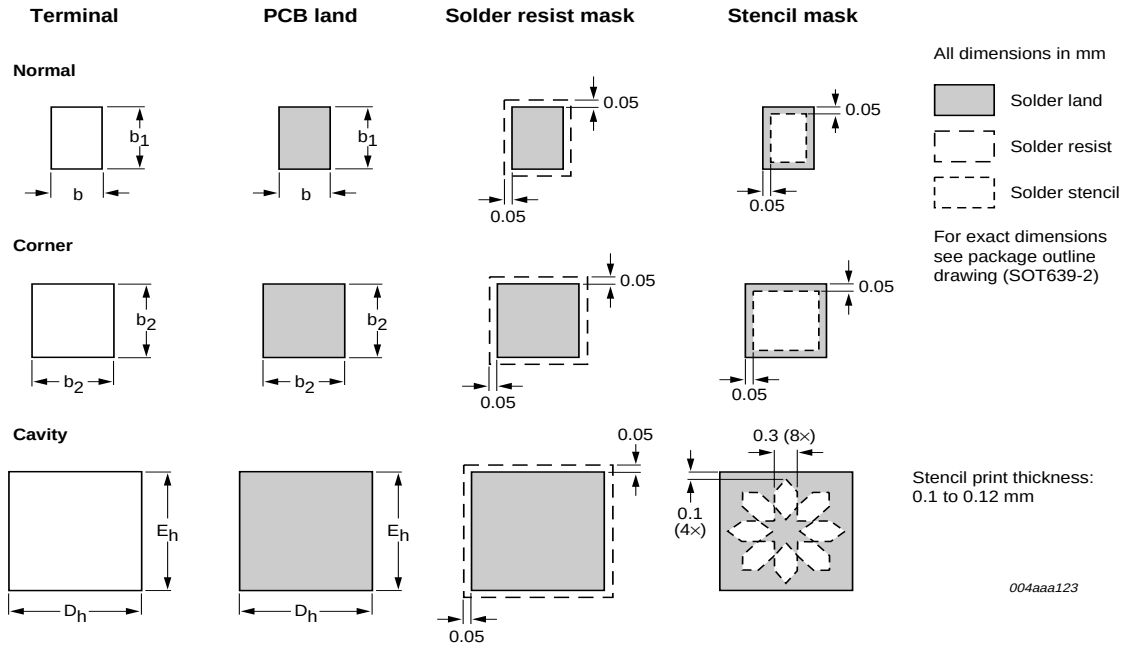
[4] Wave soldering is only suitable for LQFP, QFP and TQFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[5] Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

15. Additional soldering information

15.1 (H)BCC packages: footprint

The surface material of the terminals on the resin protrusion consists of a 4-layer metal structure (Au, Pd, Ni and Pd). The Au + Pd layer (0.1 µm min.) ensures solderability, the Ni layer (5 µm min.) prevents diffusion, and the Pd layer on top (0.5 µm min.) ensures effective wire bonding.



Cavity: exposed diepad, either functioning as heatsink or as ground connection; only for HBCC packages.

Fig 15. (H)BCC footprint and solder resist mask dimensions.

15.2 (H)BCC packages: reflow soldering profile

The conditions for reflow soldering of (H)BCC packages are as follows:

- **Preheating time**: minimum 90 s at T = 145 to 155 °C
- **Soldering time**: minimum 90 s (BCC) or minimum 100 s (HBCC) at T > 183 °C
- **Peak temperature**:
  - Ambient temperature: $T_{amb(max)}$ = 260 °C
  - Device surface temperature: $T_{case(max)}$ = 255 °C.

16. Revision history

Table 19: Revision history

Rev	Date	CPCN	Description
06	20011130	-	**Product data; sixth version. Supersedes ISP1105_1106_1107-05 of 3 Sept 2001 (9397 750 08643). Modifications:** • Changed the HBCC16 package version from SOT639-1 to SOT639-2 in: – Table 1 “Ordering information” on page 2. – Section 12 “Package outline” on page 16. – Figure 15 “(H)BCC footprint and solder resist mask dimensions.” on page 21. • Section 7.4 “Power supply input options”: Removed the last sentence “The internal regulator is not used in single-ended mode and is shutdown.” from the Internal regulator definition.
05	20010903	-	**Product data; fifth version. Supersedes ISP1105_1106_1107-04 of 2 Aug 2001 (9397 750 08643). Modifications:** • Replaced front-page logo with new USB basic-speed logo.
04	20010802	-	**Preliminary data; fourth version. Supersedes ISP1105_1106_1107-03 of 4 July 2001 (9397 750 08515). Modifications:** • Section 1 “General description”: removed backward compatibility with PDIUSBP11A. • Section 2 “Features”: – Removed backward compatibility with PDIUSBP11A. – Added ‘on-chip’ for the ESD protection. – Changed the I/O voltage range from ‘1.8 V, 2.5 V or 3.3 V’ into ‘1.65 V to 3.6 V’. • Section 6.2 “Pin description”: changed the description for pin $V_{CC(I/O)}$. • Section 7.3 “Power supply configurations”: changed $V_{CC(I/O)}$ range from ‘1.8 V, 2.5 V or 3.3 V’ into ‘1.65 to 3.6 V’ in the description of Normal mode, in Table 8 and in Table 10. • Table 13 “Static characteristics: supply pins”: removed table note for I_{CC} referencing the *USB On-The-Go specification*. • Table 14 “Static characteristics: digital pins”: changed the commonly supported types of $V_{CC(I/O)}$ into examples. • Section 15.1 “(H)BCC packages: footprint”: added paragraph on terminal composition. • Section 15.2 “(H)BCC packages: reflow soldering profile”: changed peak temperature from 220 °C ±5 °C to 260 °C (ambient) and 255 °C (device surface).
03	20010704	-	**Preliminary data; third version. Supersedes ISP1107-02 of 5 February 2001 (9397 750 07879). Modification:** • ISP1107, ISP1106 and ISP1105 combined into one datasheet.
02	20010205	-	**Objective specification; second version. Supersedes ISP1107-01 of 23 February 2000 (9397 750 06899). ISP1107 stand-alone datasheet only.**
01	20000223	-	**Objective specification; initial version. ISP1107 stand-alone datasheet only.**

17. Data sheet status

Data sheet status[1]	Product status[2]	Definition
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

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