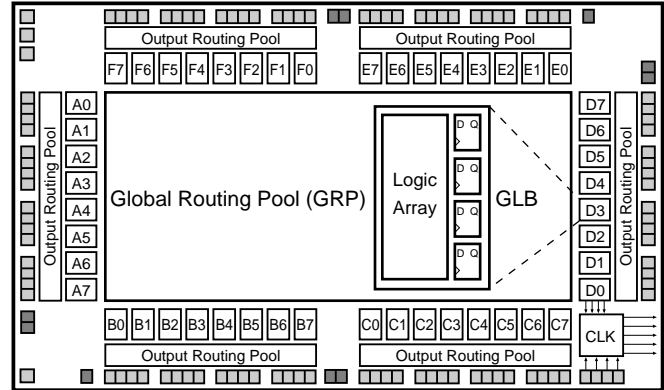


## Features

- **HIGH-DENSITY PROGRAMMABLE LOGIC**
  - 8000 PLD Gates
  - 96 I/O Pins, 12 Dedicated Inputs, 2 Global Output Enables
  - 288 Registers
  - High-Speed Global Interconnect
  - Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.
  - Small Logic Block Size for Random Logic
  - Security Cell Prevents Unauthorized Copying
- **HIGH PERFORMANCE E<sup>2</sup>CMOS<sup>®</sup> TECHNOLOGY**
  - $f_{max} = 50$  MHz Maximum Operating Frequency
  - $t_{pd} = 22$  ns Propagation Delay
  - TTL Compatible Inputs and Outputs
  - Electrically Erasable and Reprogrammable
  - Non-Volatile E<sup>2</sup>CMOS Technology
  - 100% Tested at Time of Manufacture
- **IN-SYSTEM PROGRAMMABLE**
  - In-System Programmable<sup>™</sup> (ISP<sup>™</sup>) 5-Volt Only
  - Increased Manufacturing Yields, Reduced Time-to-Market, and Improved Product Quality
  - Reprogram Soldered Devices for Faster Debugging
- **COMBINES EASE OF USE AND THE FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**
  - Complete Programmable Device Can Combine Glue Logic and Structured Designs
  - Four Dedicated Clock Input Pins
  - Synchronous and Asynchronous Clocks
  - Flexible Pin Placement
  - Optimized Global Routing Pool Provides Global Interconnectivity
- **ispDesignEXPERT<sup>™</sup> – LOGIC COMPILER AND COMPLETE ISP DEVICE DESIGN SYSTEMS FROM HDL SYNTHESIS THROUGH IN-SYSTEM PROGRAMMING**
  - Superior Quality of Results
  - Tightly Integrated with Leading CAE Vendor Tools
  - Productivity Enhancing Timing Analyzer, Explore Tools, Timing Simulator and ispANALYZER<sup>™</sup>
  - PC and UNIX Platforms

## Functional Block Diagram



0139G1A-isp

## Description

The ispLSI 1048C/883 is a High-Density Programmable Logic Device processed in full compliance to MIL-STD-883. This military grade device contains 288 Registers, 96 Universal I/O pins, 12 Dedicated Input pins, two Global Output Enables (GOE), four Dedicated Clock Input pins and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements. The ispLSI 1048C/883 features 5-Volt in-system programming and in-system diagnostic capabilities. It is the first device which offers non-volatile reprogrammability of the logic, and the interconnect to provide truly reconfigurable systems. Compared to the ispLSI 1048, the ispLSI 1048C/883 offers two additional dedicated inputs and two new Global Output Enable pins.

The basic unit of logic on the ispLSI 1048C/883 device is the Generic Logic Block (GLB). The GLBs are labeled A0, A1 .. F7 in figure 1. There are a total of 48 GLBs in the ispLSI 1048C/883 devices. Each GLB has 18 inputs, a programmable AND/OR/XOR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any other GLB on the device.



## Absolute Maximum Ratings <sup>1</sup>

Supply Voltage  $V_{CC}$  ..... -0.5 to +7.0V  
 Input Voltage Applied ..... -2.5 to  $V_{CC} + 1.0V$   
 Off-State Output Voltage Applied ..... -2.5 to  $V_{CC} + 1.0V$   
 Storage Temperature ..... -65 to 150°C  
 Case Temp. with Power Applied ..... -55 to 125°C  
 Max. Junction Temp. ( $T_J$ ) with Power Applied ... 150°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

## DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	MAX.	UNITS		
$V_{CC}$	Supply Voltage	Military/883	$T_C = -55^{\circ}C$ to $+125^{\circ}C$	4.5	5.5	
$V_{IL}$	Input Low Voltage	0		0.8		V
$V_{IH}$	Input High Voltage	2.0		$V_{CC} + 1$		V

0005A mil.eps

## Capacitance ( $T_A=25^{\circ}C$ , $f=1.0$ MHz)

SYMBOL	PARAMETER	MAXIMUM <sup>1</sup>	UNITS	TEST CONDITIONS
$C_1$	Dedicated Input Capacitance	10	pf	$V_{CC}=5.0V$ , $V_{IN}=2.0V$
$C_2$	I/O and Clock Capacitance	10	pf	$V_{CC}=5.0V$ , $V_{I/O}$ , $V_Y=2.0V$

1. Characterized but not 100% tested.

Table 2- 0006mil

## Data Retention Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention	20	—	Years
Erase/Reprogram Cycles	10000	—	Cycles

Table 2- 0008B

**Switching Test Conditions**

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Time	≤ 3ns 10% to 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See figure 2

3-state levels are measured 0.5V from steady-state active level.

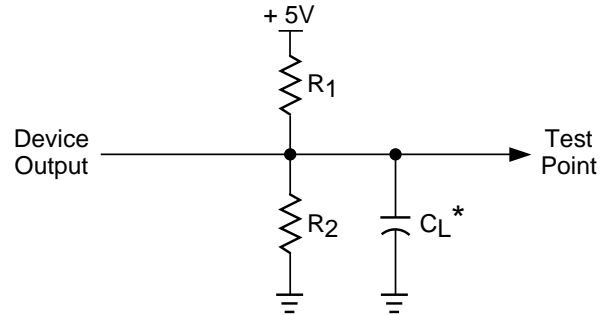
Table 2- 0003

**Output Load Conditions (see figure 2)**

Test Condition		R1	R2	CL
A		470Ω	390Ω	35pF
B	Active High	∞	390Ω	35pF
	Active Low	470Ω	390Ω	35pF
C	Active High to Z at $V_{OH} - 0.5V$	∞	390Ω	5pF
	Active Low to Z at $V_{OL} + 0.5V$	470Ω	390Ω	5pF

Table 2- 0004A

**Figure 2. Test Load**



\*CL includes Test Fixture and Probe Capacitance.

**DC Electrical Characteristics**

**Over Recommended Operating Conditions**

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. <sup>3</sup>	MAX.	UNITS
<b>V<sub>OL</sub></b>	Output Low Voltage	$I_{OL} = 8 \text{ mA}$	–	–	0.4	V
<b>V<sub>OH</sub></b>	Output High Voltage	$I_{OH} = -4 \text{ mA}$	2.4	–	–	V
<b>I<sub>IL</sub></b>	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} \text{ (MAX.)}$	–	–	-10	μA
<b>I<sub>IH</sub></b>	Input or I/O High Leakage Current	$3.5V \leq V_{IN} \leq V_{CC}$	–	–	10	μA
<b>I<sub>IL-isp</sub></b>	isp Input Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} \text{ (MAX.)}$	–	–	-150	μA
<b>I<sub>IL-PU</sub></b>	I/O Active Pull-Up Current	$0V \leq V_{IN} \leq V_{IL}$	–	–	-150	μA
<b>I<sub>OS</sub><sup>1</sup></b>	Output Short Circuit Current	$V_{CC} = 5V, V_{OUT} = 0.5V$	–	–	-200	mA
<b>I<sub>CC</sub><sup>2,4</sup></b>	Operating Power Supply Current	$V_{IL} = 0.5V, V_{IH} = 3.0V$ $f_{TOGGLE} = 1 \text{ MHz}$	–	165	260	mA

1. One output at a time for a maximum duration of one second.  $V_{out} = 0.5V$  was selected to avoid test problems by tester ground degradation. Characterized but not 100% tested.
2. Measured using twelve 16-bit counters.
3. Typical values are at  $V_{CC} = 5V$  and  $T_A = 25^\circ C$ .
4. Maximum  $I_{CC}$  varies widely with specific device configuration and operating frequency. Refer to the Power Consumption section of this datasheet and Thermal Management section of the Lattice Semiconductor Data Book or CD-ROM to estimate maximum  $I_{CC}$ .

0007A-48C mil

## External Timing Parameters

### Over Recommended Operating Conditions

PARAMETER	TEST COND. # <sup>2</sup>	DESCRIPTION <sup>1</sup>	-50		UNITS
			MIN.	MAX.	
t <sub>pd1</sub>	A	1	Data Propagation Delay, 4PT bypass, ORP bypass		ns
t <sub>pd2</sub>	A	2	Data Propagation Delay		ns
f <sub>max</sub> (Int.)	A	3	Clock Frequency with Internal Feedback <sup>3</sup>		MHz
f <sub>max</sub> (Ext.)	–	4	Clock Frequency with External Feedback ( $\frac{1}{t_{su2} + t_{co1}}$ )		MHz
f <sub>max</sub> (Tog.)	–	5	Clock Frequency, Max Toggle ( $\frac{1}{t_{wh} + t_{wl}}$ )		MHz
t <sub>su1</sub>	–	6	GLB Reg. Setup Time before Clock, 4PT bypass		ns
t <sub>co1</sub>	A	7	GLB Reg. Clock to Output Delay, ORP bypass		ns
t <sub>h1</sub>	–	8	GLB Reg. Hold Time after Clock, 4 PT bypass		ns
t <sub>su2</sub>	–	9	GLB Reg. Setup Time before Clock		ns
t <sub>co2</sub>	–	10	GLB Reg. Clock to Output Delay		ns
t <sub>h2</sub>	–	11	GLB Reg. Hold Time after Clock		ns
t <sub>r1</sub>	A	12	Ext. Reset Pin to Output Delay		ns
t <sub>rw1</sub>	–	13	Ext. Reset Pulse Duration		ns
t <sub>ptoen</sub>	B	14	Input to Output Enable		ns
t <sub>ptoedis</sub>	C	15	Input to Output Disable		ns
t <sub>goen</sub>	B	16	Global OE Output Enable		ns
t <sub>goedis</sub>	C	17	Global OE Output Disable		ns
t <sub>wh</sub>	–	20	Ext. Sync. Clock Pulse Duration, High		ns
t <sub>wl</sub>	–	21	Ext. Sync. Clock Pulse Duration, Low		ns
t <sub>su3</sub>	–	22	I/O Reg. Setup Time before Ext. Sync. Clock (Y2, Y3)		ns
t <sub>h3</sub>	–	23	I/O Reg. Hold Time after Ext. Sync. Clock (Y2, Y3)		ns

1. Unless noted otherwise, all parameters use a GRP load of 4 GLBs, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-Bit counter using GRP feedback.
4. Reference Switching Test Conditions section.

Table 2- 0030-48C/50 mil

## Internal Timing Parameters<sup>1</sup>

PARAMETER	# <sup>2</sup>	DESCRIPTION	-50		UNITS
			MIN.	MAX.	
<b>Inputs</b>					
t <sub>iobp</sub>	24	I/O Register Bypass	–	4.3	ns
t <sub>iolat</sub>	25	I/O Latch Delay	–	5.5	ns
t <sub>iosu</sub>	26	I/O Register Setup Time before Clock	9.1	–	ns
t <sub>ioh</sub>	27	I/O Register Hold Time after Clock	0.3	–	ns
t <sub>ioco</sub>	28	I/O Register Clock to Out Delay	–	4.6	ns
t <sub>ior</sub>	29	I/O Register Reset to Out Delay	–	5.1	ns
t <sub>din</sub>	30	Dedicated Input Delay	–	7.4	ns
<b>GRP</b>					
t <sub>grp1</sub>	31	GRP Delay, 1 GLB Load	–	6.2	ns
t <sub>grp4</sub>	32	GRP Delay, 4 GLB Loads	–	6.7	ns
t <sub>grp8</sub>	33	GRP Delay, 8 GLB Loads	–	8.0	ns
t <sub>grp16</sub>	34	GRP Delay, 16 GLB Loads	–	10.5	ns
t <sub>grp48</sub>	35	GRP Delay, 48 GLB Loads	–	22.7	ns
<b>GLB</b>					
t <sub>4ptbp</sub>	36	4 Product Term Bypass Path Delay	–	5.5	ns
t <sub>1ptxor</sub>	37	1 Product Term/XOR Path Delay	–	6.7	ns
t <sub>20ptxor</sub>	38	20 Product Term/XOR Path Delay	–	7.5	ns
t <sub>xoradj</sub>	39	XOR Adjacent Path Delay <sup>3</sup>	–	8.9	ns
t <sub>gbp</sub>	40	GLB Register Bypass Delay	–	1.2	ns
t <sub>gsu</sub>	41	GLB Register Setup Time before Clock	3.9	–	ns
t <sub>gh</sub>	42	GLB Register Hold Time after Clock	7.3	–	ns
t <sub>gco</sub>	43	GLB Register Clock to Output Delay	–	2.3	ns
t <sub>gro</sub>	44	GLB Register Reset to Output Delay	–	2.8	ns
t <sub>ptre</sub>	45	GLB Product Term Reset to Register Delay	–	11.1	ns
t <sub>ptoe</sub>	46	GLB Product Term Output Enable to I/O Cell Delay	–	9.6	ns
t <sub>ptck</sub>	47	GLB Product Term Clock Delay	3.4	8.2	ns
<b>ORP</b>					
t <sub>orp</sub>	48	ORP Delay	–	3.4	ns
t <sub>orpbp</sub>	49	ORP Bypass Delay	–	1.4	ns

1. Internal Timing Parameters are not tested and are for reference only.

Table 2- 0036-48C/50MIL

2. Refer to Timing Model in this data sheet for further details.

3. The XOR adjacent path can only be used by hard macros.

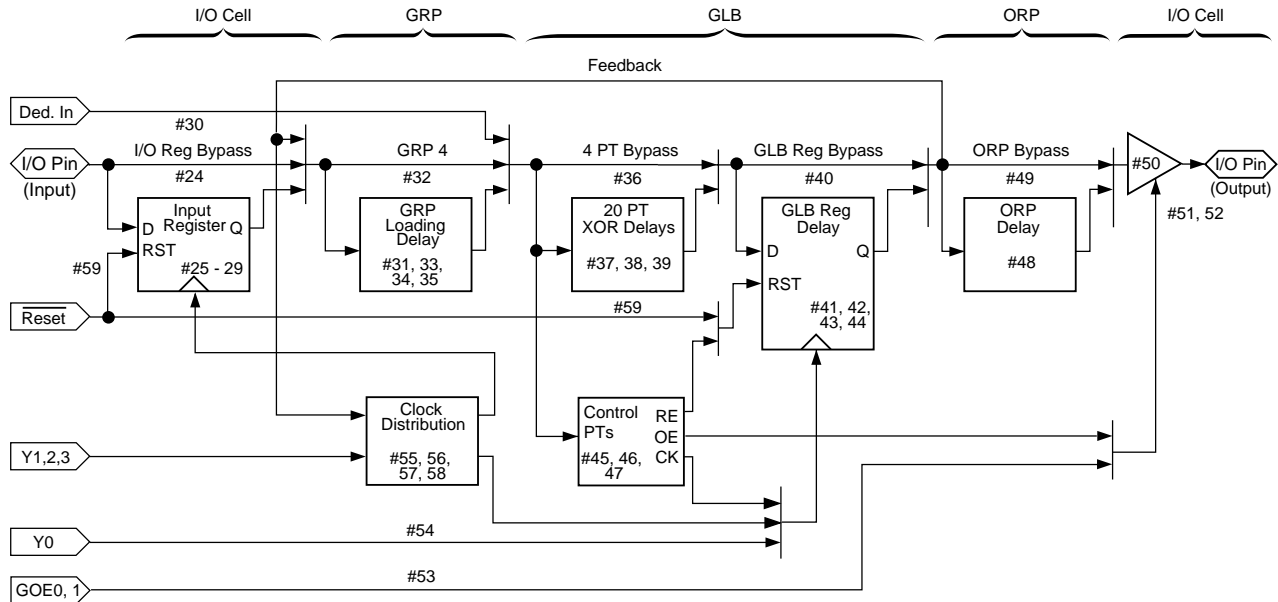
**Internal Timing Parameters<sup>1</sup>**

PARAMETER	# <sup>2</sup>	DESCRIPTION	-50		UNITS
			MIN.	MAX.	
<b>Outputs</b>					
t <sub>ob</sub>	50	Output Buffer Delay	–	2.9	ns
t <sub>oen</sub>	51	I/O Cell OE to Output Enabled	–	6.9	ns
t <sub>odis</sub>	52	I/O Cell OE to Output Disabled	–	6.9	ns
t <sub>goe</sub>	53	Global OE	–	13.6	ns
<b>Clocks</b>					
t <sub>gy0</sub>	54	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	7.4	7.4	ns
t <sub>gy1/2</sub>	55	Clock Delay, Y1 or Y2 to Global GLB Clock Line	6.1	8.7	ns
t <sub>gcp</sub>	56	Clock Delay, Clock GLB to Global GLB Clock Line	2.6	7.6	ns
t <sub>ioy2/3</sub>	57	Clock Delay, Y2 or Y3 to I/O Cell Global Clock Line	6.1	8.7	ns
t <sub>iocp</sub>	58	Clock Delay, Clock GLB to I/O Cell Global Clock Line	2.6	7.6	ns
<b>Global Reset</b>					
t <sub>gr</sub>	59	Global Reset to GLB and I/O Registers	–	11.4	ns

1. Internal Timing Parameters are not tested and are for reference only.  
 2. Refer to Timing Model in this data sheet for further details.

Table 2- 0037-48C/50mil

**ispLSI 1048C/883 Timing Model**



0491A/48

**Derivations of  $t_{su}$ ,  $t_h$  and  $t_{co}$  from the Product Term Clock<sup>1</sup>**

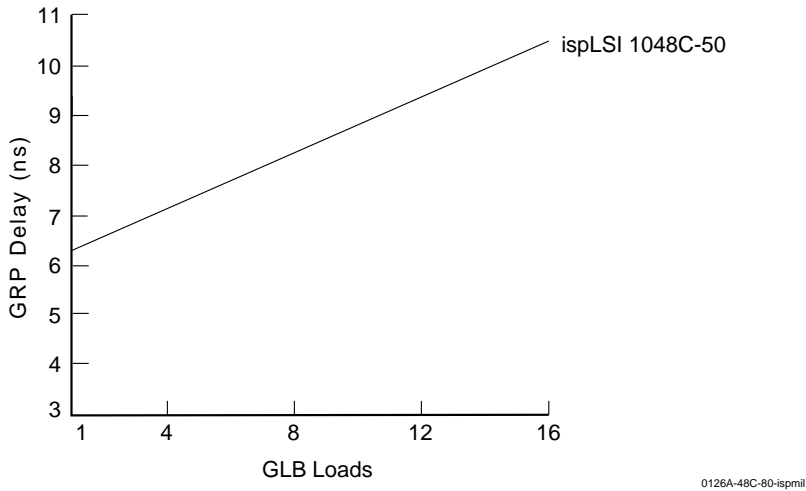
$$\begin{aligned}
 t_{su} &= \text{Logic} + \text{Reg } s_u - \text{Clock (min)} \\
 &= (t_{iobp} + t_{grp4} + t_{20ptxor}) + (t_{gsu}) - (t_{iobp} + t_{grp4} + t_{ptck(min)}) \\
 &= (\#24 + \#32 + \#38) + (\#41) - (\#24 + \#32 + \#47) \\
 8.0 \text{ ns} &= (4.3 + 6.7 + 7.5) + (3.9) - (4.3 + 6.7 + 3.4) \\
 \\
 t_h &= \text{Clock (max)} + \text{Reg } h - \text{Logic} \\
 &= (t_{iobp} + t_{grp4} + t_{ptck(max)}) + (t_{gh}) - (t_{iobp} + t_{grp4} + t_{20ptxor}) \\
 &= (\#24 + \#32 + \#47) + (\#42) - (\#24 + \#32 + \#38) \\
 8.0 \text{ ns} &= (4.3 + 6.7 + 8.2) + (7.3) - (4.3 + 6.7 + 7.5) \\
 \\
 t_{co} &= \text{Clock (max)} + \text{Reg } c_o + \text{Output} \\
 &= (t_{iobp} + t_{grp4} + t_{ptck(max)}) + (t_{gco}) + (t_{orp} + t_{ob}) \\
 &= (\#24 + \#32 + \#47) + (\#43) + (\#48 + \#50) \\
 32.8 \text{ ns} &= (4.3 + 6.7 + 8.2) + (7.3) + (3.4 + 2.9)
 \end{aligned}$$

**Derivations of  $t_{su}$ ,  $t_h$  and  $t_{co}$  from the Clock GLB<sup>1</sup>**

$$\begin{aligned}
 t_{su} &= \text{Logic} + \text{Reg } s_u - \text{Clock (min)} \\
 &= (t_{iobp} + t_{grp4} + t_{20ptxor}) + (t_{gsu}) - (t_{gy0(min)} + t_{gco} + t_{gcp(min)}) \\
 &= (\#24 + \#32 + \#38) + (\#41) - (\#54 + \#43 + \#56) \\
 10.1 \text{ ns} &= (4.3 + 6.7 + 7.5) + (3.9) - (7.4 + 2.3 + 2.6) \\
 \\
 t_h &= \text{Clock (max)} + \text{Reg } h - \text{Logic} \\
 &= (t_{gy0(max)} + t_{gco} + t_{gcp(max)}) + (t_{gh}) - (t_{iobp} + t_{grp4} + t_{20ptxor}) \\
 &= (\#54 + \#43 + \#56) + (\#42) - (\#24 + \#32 + \#38) \\
 6.1 \text{ ns} &= (7.4 + 2.3 + 7.6) + (7.3) - (4.3 + 6.7 + 7.5) \\
 \\
 t_{co} &= \text{Clock (max)} + \text{Reg } c_o + \text{Output} \\
 &= (t_{gy0(max)} + t_{gco} + t_{gcp(max)}) + (t_{gco}) + (t_{orp} + t_{ob}) \\
 &= (\#54 + \#43 + \#56) + (\#43) + (\#48 + \#50) \\
 30.9 \text{ ns} &= (7.4 + 2.3 + 7.6) + (7.3) + (3.4 + 2.9)
 \end{aligned}$$

1. Calculations are based upon timing specifications for the ispLSI 1048C-50

**Maximum GRP Delay vs GLB Loads**

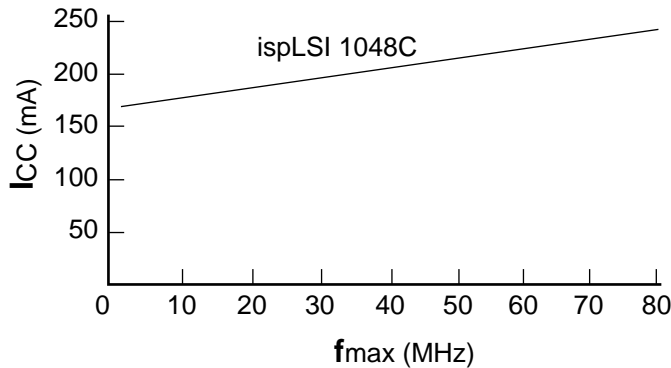


**Power Consumption**

Power consumption in the ispLSI 1048C/883 device depends on two primary factors: the speed at which the device is operating, and the number of Product Terms

used. Figure 3 shows the relationship between power and operating speed.

**Figure 3. Typical Device Power Consumption vs fmax**



Notes: Configuration of Twelve 16-bit Counters  
Typical Current at 5V, 25°C

ICC can be estimated for the ispLSI 1048C using the following equation:

$$I_{CC} = 73 + (\# \text{ of PTs} * 0.23) + (\# \text{ of nets} * \text{Max. freq} * 0.010) \text{ where:}$$

# of PTs = Number of Product Terms used in design

# of nets = Number of Signals used in device

Max. freq = Highest Clock Frequency to the device

The ICC estimate is based on typical conditions (VCC = 5.0V, room temperature) and an assumption of 2 GLB loads on average exists. These values are for estimates only. Since the value of ICC is sensitive to operating conditions and the program in the device, the actual ICC should be verified.

0127A-48C-80-isp

## Pin Description

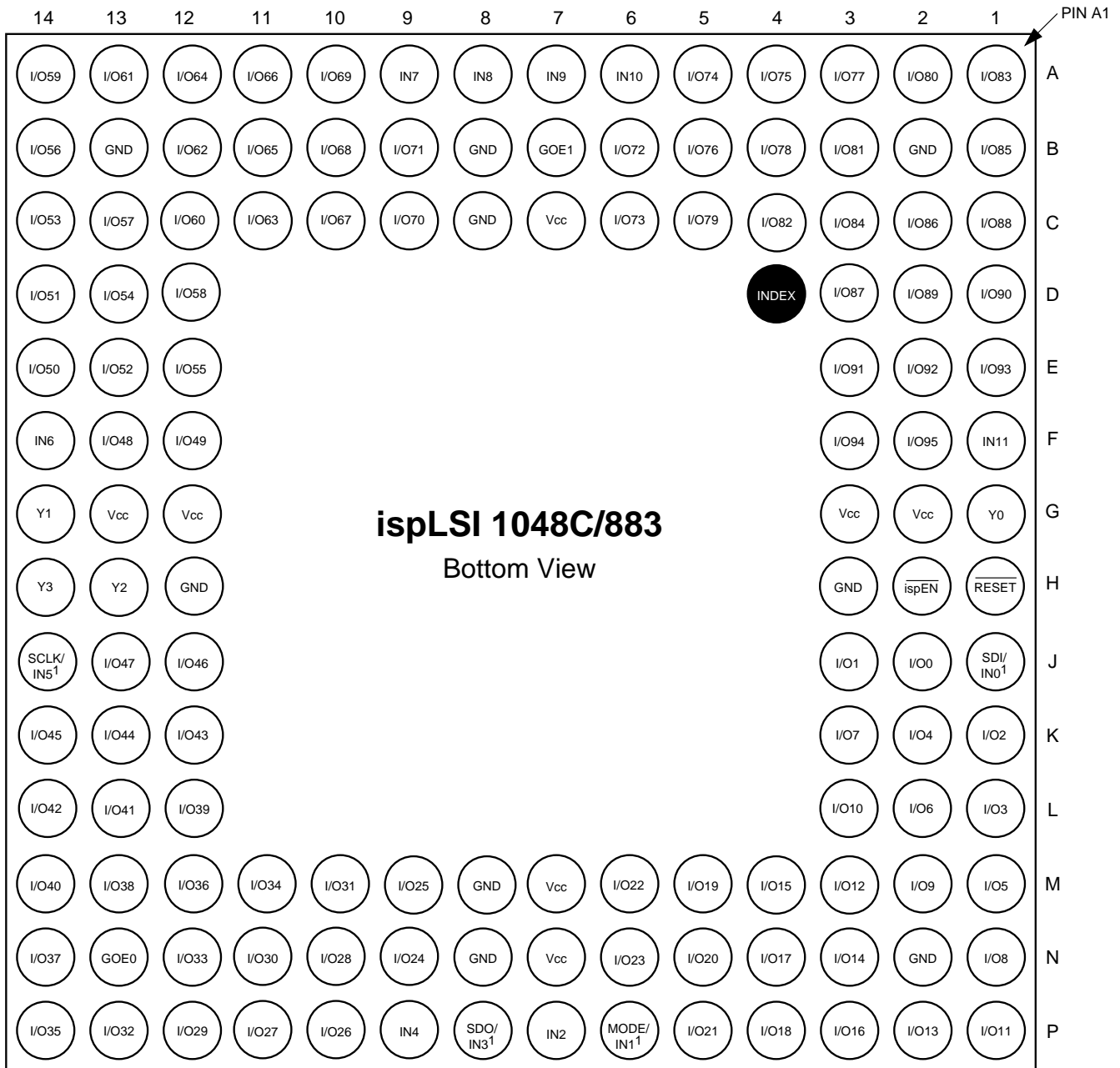
NAME	CPGA PIN NUMBERS	DESCRIPTION
I/O 0 - I/O 5 I/O 6 - I/O 11 I/O 12 - I/O 17 I/O 18 - I/O 23 I/O 24 - I/O 29 I/O 30 - I/O 35 I/O 36 - I/O 41 I/O 42 - I/O 47 I/O 48 - I/O 53 I/O 54 - I/O 59 I/O 60 - I/O 65 I/O 66 - I/O 71 I/O 72 - I/O 77 I/O 78 - I/O 83 I/O 84 - I/O 89 I/O 90 - I/O 95	J2, J3, K1, L1, K2, M1, L2, K3, N1, M2, L3, P1, M3, P2, N3, M4, P3, N4, P4, M5, N5, P5, M6, N6, N9, M9, P10, P11, N10, P12, N11, M10, P13, N12, M11, P14, M12, N14, M13, L12, M14, L13, L14, K12, K13, K14, J12, J13, F13, F12, E14, D14, E13, C14, D13, E12, B14, C13, D12, A14, C12, A13, B12, C11, A12, B11, A11, C10, B10, A10, C9, B9, B6, C6, A5, A4, B5, A3, B4, C5, A2, B3, C4, A1, C3, B1, C2, D3, C1, D2, D1, E3, E2, E1, F3, F2	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
GOE0, GOE1	N13, B7,	Global output enables for all I/Os.
IN 2, IN 4 IN 6 - IN 11	P7, P9 F14, A9, A8, A7, A6, F1	Dedicated input pins to the device.
$\overline{\text{ispEN}}$	H2	Input – Dedicated in-system programming enable input pin. This pin is brought low to enable the programming mode. The MODE, SDI, SDO and SCLK options become active.
SDI/IN 0 <sup>1</sup>	J1	Input – This pin performs two functions. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as an input pin to load programming data into the device. SDI/IN 0 also is used as one of the two control pins for the isp state machine.
MODE/IN 1 <sup>1</sup>	P6	Input – This pin performs two functions. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as a pin to control the operation of the isp state machine.
SDO/IN 3 <sup>1</sup>	P8	Input/Output – This pin performs two functions. It is a dedicated input pin when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as an output pin to read serial shift register data.
SCLK/IN 5 <sup>1</sup>	J14	Input – This pin performs two functions. It is a dedicated input when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as a clock pin for the Serial Shift Register.
$\overline{\text{RESET}}$	H1	Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device.
Y0	G1	Dedicated Clock input. This clock input is connected to one of the clock inputs of all of the GLBs on the device.
Y1	G14	Dedicated clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB on the device.
Y2	H13	Dedicated clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any GLB and/or any I/O cell on the device.
Y3	H14	Dedicated clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any I/O cell on the device.
GND	B2, B8, B13, C8, H3, H12, M8, N2, N8	Ground (GND)
VCC	C7, G2, G3, G12, G13, M7, N7	V <sub>cc</sub>

1. Pins have dual function capability.

Table 2- 0002C-48C/CPGA

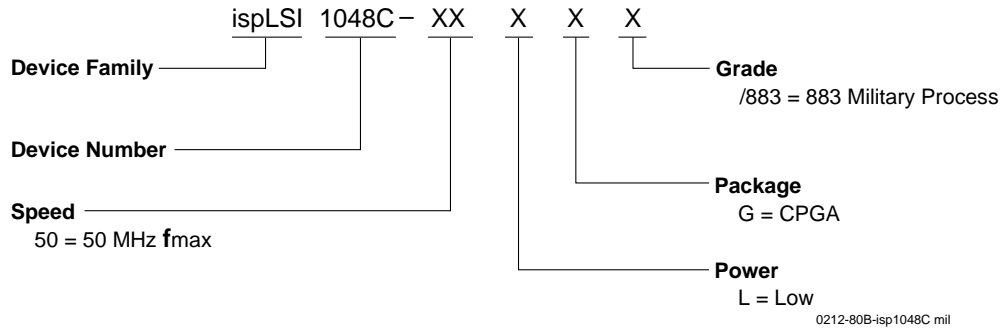
**Pin Configuration**

**ispLSI 1048C/883 133-Pin CPGA Pinout Diagram**



1. Pins have dual function capability.

**Part Number Description**



**Ordering Information**

**MILITARY**

Family	$f_{max}$ (MHz)	$t_{pd}$ (ns)	Ordering Number	SMD Number	Package
ispLSI	50	22	ispLSI 1048C-50LG/883	5962-9558701MXC	133-Pin CPGA

Table 2- 0041A-48C-ispmil



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