

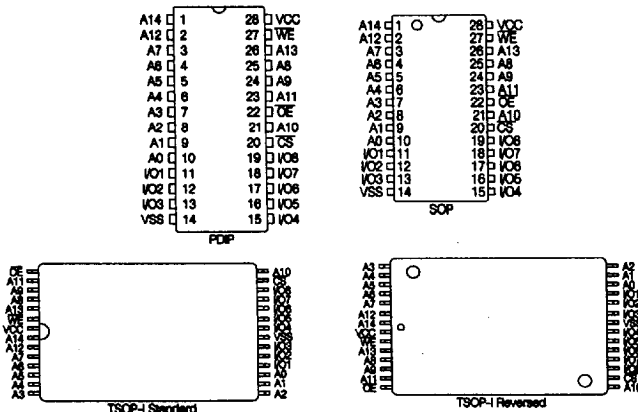
DESCRIPTION

The HY62256A is a high-speed, low power and 32,768 x 8-bits CMOS static RAM fabricated using Hyundai's high performance twin tub CMOS process technology. This high reliability process coupled with innovative circuit design techniques, yields maximum access time of 55ns. The HY62256A has a data retention mode that guarantees data to remain valid at a minimum power supply voltage of 2.0 volt. Using CMOS technology, supply voltages from 2.0 to 5.5 volt have little effect on supply current in data retention mode. Reducing the supply voltage to minimize current drain is unnecessary with the HY62256A Series.

FEATURES

- High speed - 55/70/85/100ns (max.)
- Low power consumption
 - Operating : 150mW (typ.)
 - Standby (CMOS) : 5 μ W (typ.)
- Single 5V $\pm$ 10% power supply
- Battery backup (L/LL-part)
 - 2.0V (min.) data retention
- Fully static operation
 - No clock or refresh required
- TTL compatible inputs and outputs
- Tri-state output
- Standard pin configuration
 - 28 pin 600 mil PDIP
 - 28 pin 330 mil SOP
 - 28 pin 8x13.4 mm TSOP-I

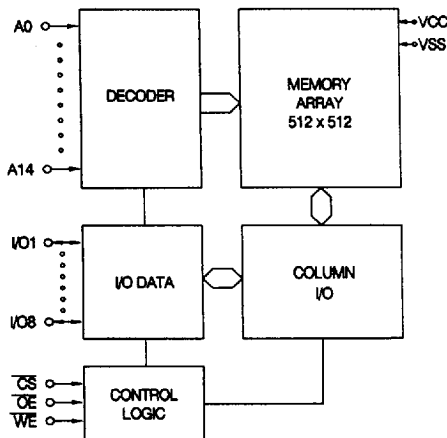
PIN CONNECTION



PIN DESCRIPTION

Pin Name	Pin Function
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
A0-A14	Address Inputs
I/O1-I/O8	Data Input/Output
Vcc	Power(+5V)
Vss	Ground

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS⁽¹⁾

SYMBOL	PARAMETER	RATING	UNIT
VCC, VIN, VOUT	Power Supply, Input/Output Voltage	-0.5 to 7.0	V
TA	Operating Temperature	0 to 70	°C
TBIAS	Temperature Under Bias	-10 to 125	°C
TSTG	Storage Temperature	-65 to 150	°C
PD	Power Dissipation	1.0	W
IOUT	Data Output Current	50	mA
TSOLDER	Lead Soldering Temperature & Time	260 ± 10	°C • sec

Note:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(TA= 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VCC	Power Supply Voltage	4.5	5.0	5.5	V
VIH	Input High Voltage	2.2	-	Vcc+0.5	V
VIL	Input Low Voltage	-0.5 ⁽¹⁾	-	0.8	V

Note:

- VIL = -3.0V for pulse width less than 50ns

TRUTH TABLE

MODE	I/O OPERATION	$\overline{CS}$	WE	$\overline{OE}$
Standby	High-Z	H	X	X
Output Disabled	High-Z	L	H	H
Read	Data Out	L	H	L
Write	Data in	L	L	X

Note:

- H=VIH, L=VIL, X=Don't Care

DC CHARACTERISTICS

(TA = 0°C to 70°C, VCC = 5V± 10%, unless otherwise specified.)

SYMBOL	PARAMETER	TEST CONDITIONS	POWER	MIN.	TYP.	MAX.	UNIT
ILI	Input Leakage Current	$V_{SS} \leq V_{IN} \leq V_{CC}$		-1	-	1	μA
ILO	Output Leakage Current	$V_{SS} \leq V_{OUT} \leq V_{CC}$, $\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$		-1	-	1	μA
ICC	Operating Power Supply Current	$\overline{CS} = V_{IL}$ $V_{IN} = V_{IH}$ or V_{IL} , $I_{IO} = 0mA$		-	30	50	mA
ICC1	Average Operating Current	$\overline{CS} = V_{IL}$ Min. Duty Cycle=100%, $I_{IO} = 0mA$		-	40	70	mA
ISB	TTL Standby Current (TTL Inputs)	$\overline{CS} = V_{IH}$ $V_{IN} = V_{IH}$ or V_{IL}		-	0.4	2	mA
ISB1	CMOS Standby Current (CMOS Inputs)	$\overline{CS} \geq V_{CC} - 0.2V$		-	-	1	mA
		$V_{IN} \geq V_{CC} - 0.2V$ or	L	-	2	100	μA
		$V_{IN} \leq 0.2V$	LL	-	1	25	μA
VOL	Output Low Voltage	$I_{OL} = 2.1mA$		-	-	0.4	V
VOH	Output High Voltage	$I_{OH} = -1.0mA$		2.4	-	-	V

Note:

1. Typical values are at VCC=5.0V, TA=25°C

AC CHARACTERISTICS

(TA=0°C to 70°C, VCC=5V ±10%, unless otherwise noted.)

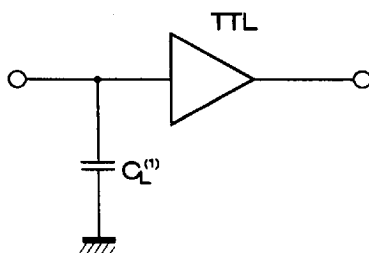
#	SYMBOL	PARAMETER	-55		-70		-85		-10		UNIT
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
READ CYCLE											
1	tRC	Read Cycle Time	55	-	70	-	85	-	100	-	ns
2	tAA	Address Access Time	-	55	-	70	-	85	-	100	ns
3	tACS	Chip Select Access Time	-	55	-	70	-	85	-	100	ns
4	tOE	Output Enable to Output Valid	-	30	-	35	-	45	-	50	ns
5	tCLZ	Chip Select to Low -Z Output	5	-	5	-	5	-	5	-	ns
6	tOLZ	Output Enable to Low-Z Output	5	-	5	-	5	-	5	-	ns
7	tCHZ	Chip Disable to High -Z Output	0	20	0	30	0	30	0	35	ns
8	tOHZ	Output Disable to High -Z Output	0	20	0	30	0	30	0	35	ns
9	tOH	Output Hold from Address Change	5	-	5	-	5	-	5	-	ns
WRITE CYCLE											
10	tWC	Write Cycle Time	55	-	70	-	85	-	100	-	ns
11	tCW	Chip Select to End of Write	50	-	65	-	75	-	80	-	ns
12	tAW	Address Valid to End of Write	50	-	65	-	75	-	80	-	ns
13	tAS	Address Set-up Time	0	-	0	-	0	-	0	-	ns
14	tWP	Write Pluse Width	40	-	50	-	60	-	70	-	ns
15	tWR	Write Recovery Time	0	-	0	-	0	-	0	-	ns
16	tWHZ	Write to High-Z Output	0	20	0	30	0	30	0	35	ns
17	tdW	Data to Write Time Overlap	25	-	35	-	40	-	40	-	ns
18	tdH	Data Hold from Write Time	0	-	0	-	0	-	0	-	ns
19	tOW	Output Active from End of Write	5	-	5	-	5	-	5	-	ns

AC TEST CONDITIONS

(TA=0°C to 70°C, VCC=5V ± 10%, unless otherwise specified.)

PARAMETER	SPEED	VALUE
Input Pulse Level		0.8V to 2.4V
Input Rise and Fall Time		5ns
Input and Output Timing Reference levels		1.5V
Output Load	70/85/100ns	CL=100pF + 1TTL Load
	55ns	CL= 50pF + 1TTL Load

AC TEST LOADS



NOTE:

1. Including jig and scope capacitance.

CAPACITANCE

(TA=25°C, f= 1MHz)

SYMBOL	PARAMETER	CONDITION	MAX.	UNIT
CIN	Input Capacitance	VIN=0V	6	pF
CIO	Input/Output Capacitance	VVO=0V	8	pF

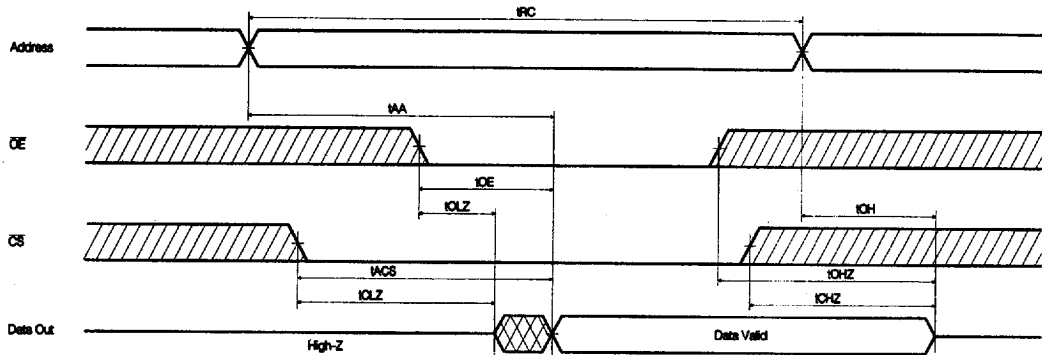
Note:

1. This parameter is sampled and not 100% tested.

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TIMING DIAGRAM

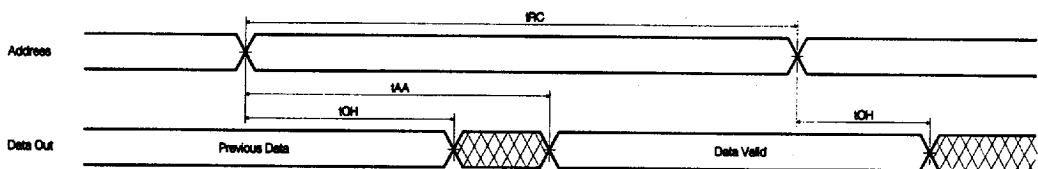
READ CYCLE 1



Note (READ CYCLE):

1. t_{CHZ} and t_{OH} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{CHZ} max. is less than t_{CLZ} min. both for a given device and from device to device.
3. $\overline{WE}$ is high for read cycle.

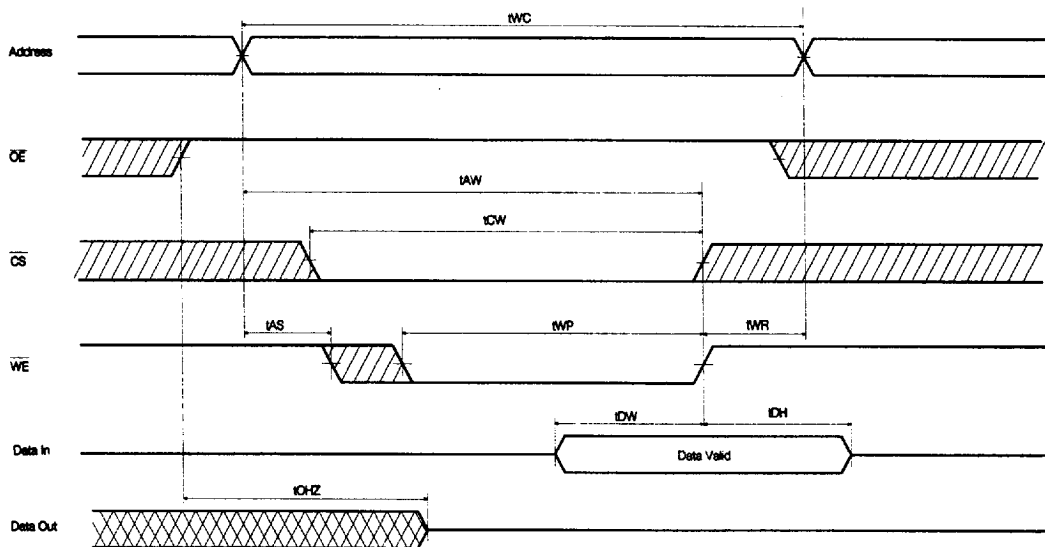
READ CYCLE 2



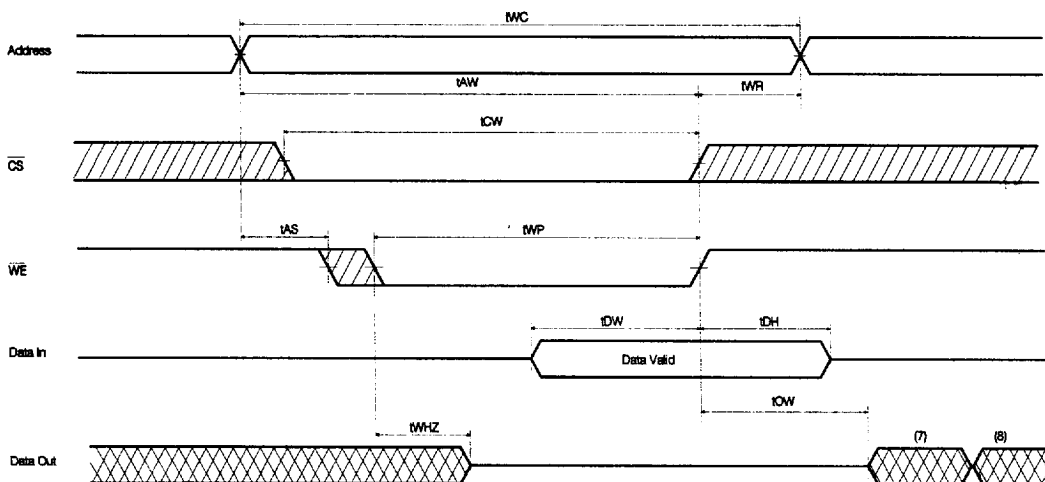
Note(READ CYCLE):

1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected $\overline{CS}=V_{IL}$.
3. $OE=V_{IL}$.

WRITE CYCLE 1 ($\overline{OE}$ Clocked)



WRITE CYCLE 2 ($\overline{OE}$ Low Fixed)



Note (WRITE CYCLE):

1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ going low, and $\overline{WE}$ going low: A write ends at the earliest transition among $\overline{CS}$ going high $\overline{WE}$ going high. t_{wp} is measured from the beginning of write to the end of write.
2. t_{cw} is measured from the later of $\overline{CS}$ going low to end of write.
3. t_{as} is measured from the address valid to the beginning of write.
4. t_{wr} is measured from the end of write to the address change. t_{wr} applied in case a write ends as $\overline{CS}$, or $\overline{WE}$ going high.
5. If $\overline{OE}$ and $\overline{WE}$ are in the read mode during this period, the I/O pins are in the output low-Z state, inputs of opposite phase of the output must not be applied because bus contention can occur.
6. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.
7. D_{OUT} is the same phase of latest written data in this write cycle.
8. D_{OUT} is the read data of the new address.

DATA RETENTION CHARACTERISTICS

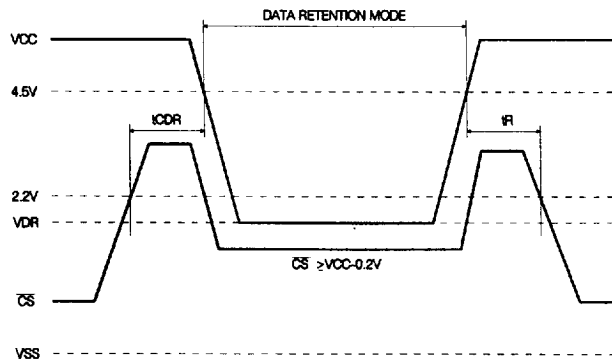
(TA=0°C to 70°C)

SYMBOL	PARAMETER	TEST CONDITION	POWER	MIN.	TYP.	MAX	UNIT
VDR	VCC for Data Retention	$\overline{CS} \geq V_{CC}-0.2V$, $V_{SS} \leq V_{IN} \leq V_{CC}$		2.0	-	-	V
ICCDR	Data Retention Current	$V_{CC}=3.0V$, $\overline{CS} \geq V_{CC}-0.2V$ $V_{SS} \leq V_{IN} \leq V_{CC}$	L	-	1	50	μA
			LL	-	1	15 ⁽²⁾	μA
tCDR	Chip Disable to Data Retention Time	See Data Retention Timing Diagram		0	-	-	ns
tR	Operating Recovery Time			tRC ⁽³⁾	-	-	ns

Notes :

1. Typical values are at the condition of TA=25°C.
2. 3 μA max. at TA=0°C to 40°C
3. tRC is read cycle time.

DATA RETENTION TIMING DIAGRAM



600 mil 28 pin Dual In-line Package(P)

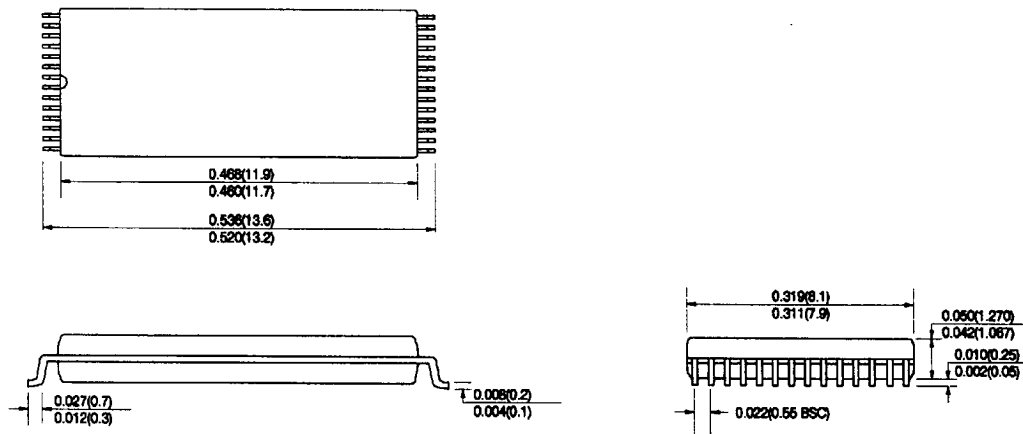


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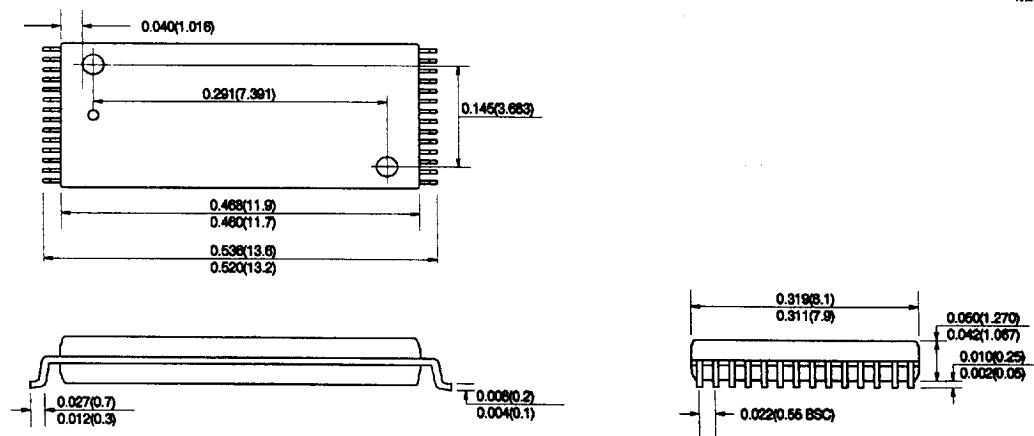
28 pin Plastic Thin Small Out Line Package(T1)

UNIT : INCH(mm) MAX
MIN



28 pin Thin Small Out Line Package(R1)

UNIT : INCH(mm) MAX
MIN



ORDERING INFORMATION

PART NO.	SPEED	POWER	PACKAGE
HY62256AP	55/70/85/100		PDIP
HY62256ALP	55/70/85/100	L-part	PDIP
HY62256ALLP	55/70/85/100	LL-part	PDIP
HY62256AJ	55/70/85/100		SOP
HY62256ALJ	55/70/85/100	L-Part	SOP
HY62256ALLJ	55/70/85/100	LL-Part	SOP
HY62256AT1	55/70/85/100		TSOP-I Standard
HY62256ALT1	55/70/85/100	L-Part	TSOP-I Standard
HY62256ALLT1	55/70/85/100	LL-Part	TSOP-I Standard
HY62256AR1	55/70/85/100		TSOP-I Reversed
HY62256ALR1	55/70/85/100	L-Part	TSOP-I Reversed
HY62256ALLR1	55/70/85/100	LL-Part	TSOP-I Reversed