

6AM13

Silicon N Channel/P Channel Complementary Power MOS FET Array

Application

High speed power switching

Features

- Low on-resistance
 N-channel: $R_{DS(on)} \leq 0.075 \Omega$, $V_{GS} = 10 \text{ V}$
 $I_D = 5 \text{ A}$
 P-channel: $R_{DS(on)} \leq 0.12 \Omega$, $V_{GS} = -10 \text{ V}$
 $I_D = -5 \text{ A}$
- Capable of 4 V gate drive
- Low drive current
- High speed switching
- High density mounting
- Suitable for H-bridged motor driver
- Discrete packaged devices of same die
 N-channel: 2SK971 (TO-220AB),
 2SK1094 (TO-220FM)
 P-channel: 2SJ173 (TO-220AB),
 2SJ176 (TO-220FM)

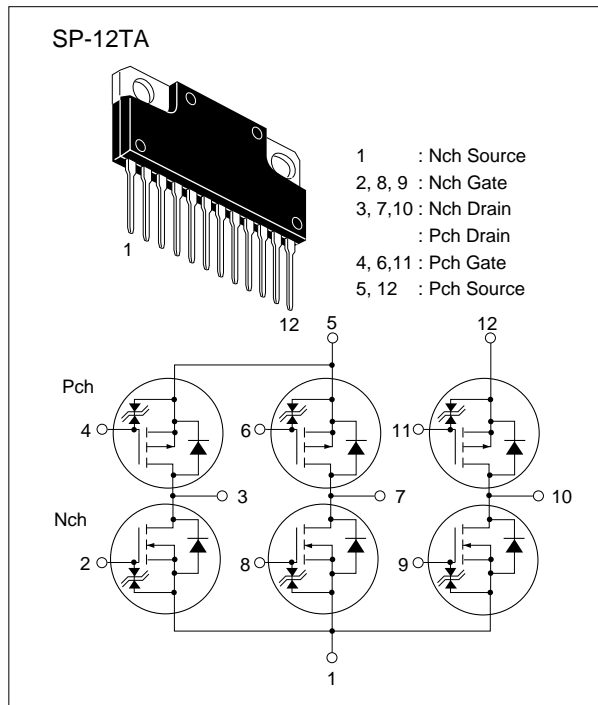


Table 1 Absolute Maximum Ratings ($T_a = 25^\circ\text{C}$)

Item	Symbol	Ratings		
		Nch	Pch	Unit
Drain to source voltage	V_{DSS}	60	-60	V
Gate to source voltage	V_{GSS}	± 20	± 20	V
Drain current	I_D	10	-10	A
Drain peak current	$I_{D(\text{pulse})}^*$	40	-40	A
Body-drain diode reverse drain current	I_{DR}	10	-10	A
Channel dissipation	Pch ($T_c = 25^\circ\text{C}$)**	42		W
Channel dissipation	Pch**	4.8		W
Channel temperature	T_{ch}	150		$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150		$^\circ\text{C}$

* $PW \leq 10 \mu\text{s}$, duty cycle $\leq 1\%$

** 6 devices operation

Table 2 Electrical Characteristics (Ta = 25°C) (1 Unit)

Item	Symbol	N channel			P channel			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max		
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	-60	—	—	V	$I_D = 10 \text{ mA}, V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	± 20	—	—	V	$I_G = \pm 100 \text{ }\mu\text{A}, V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	—	—	± 10	μA	$V_{GS} = \pm 16 \text{ V}, V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	250	—	—	-250	μA	$V_{DS} = 50 \text{ V}, V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	-1.0	—	-2.0	V	$I_D = 1 \text{ mA}, V_{DS} = 10 \text{ V}$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.06	0.075	—	0.09	0.12	Ω	$I_D = 5 \text{ A}, V_{GS} = 10 \text{ V}^*$
		—	0.08	0.11	—	0.12	0.18	Ω	$I_D = 5 \text{ A}, V_{GS} = 4 \text{ V}^*$
Forward transfer admittance	$ y_{fs} $	6	9.5	—	5	8	—	S	$I_D = 5 \text{ A}, V_{DS} = 10 \text{ V}^*$
Input capacitance	C_{iss}	—	860	—	—	1400	—	pF	$V_{DS} = 10 \text{ V}, V_{GS} = 0,$ $f = 1 \text{ MHz}$
Output capacitance	C_{oss}	—	450	—	—	720	—	pF	
Reverse transfer capacitance	C_{rss}	—	140	—	—	220	—	pF	
Turn-on delay time	$t_{d(on)}$	—	10	—	—	15	—	ns	$I_D = 5 \text{ A}, V_{GS} = 10 \text{ V},$ $R_L = 6 \text{ }\Omega$
Rise time	t_r	—	50	—	—	100	—	ns	
Turn-off delay time	$t_{d(off)}$	—	180	—	—	250	—	ns	
Fall time	t_f	—	110	—	—	160	—	ns	
Body-drain diode forward voltage	V_{DF}	—	1.0	—	—	-1.0	—	V	$I_F = 10 \text{ A}, V_{GS} = 0$
Body-drain diode reverse recovery time	t_{rr}	—	120	—	—	200	—	ns	$I_F = 10 \text{ A}, V_{GS} = 0,$ $di_F/dt = 50 \text{ A}/\mu\text{s}$

* Pulse Test

Note: Polarity of test conditions for P channel device is reversed.

■ Nch : See characteristic curves of 2SK971

■ Pch : See characteristic curves of 2SJ173

