

2M x 32 SDRAM

*512K x 32bit x 4 Banks
Synchronous DRAM
LVTTL*

Revision 1.0

January 2002

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Revision History**Revision 1.0 (January 16, 2002)**

- Defined DC spec.

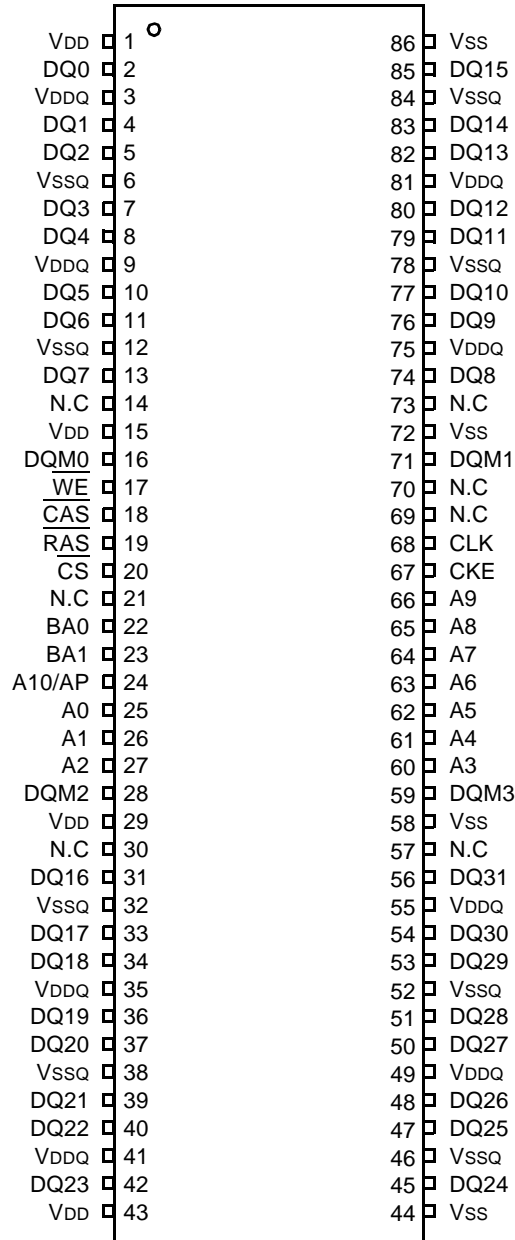
Revision 0.1 (September 03, 2001) - *Preliminary*

- Added K4S643232F-TC/L55

Revision 0.0 (September 03, 2001) - *Target Spec*

- Initial draft

PIN CONFIGURATION (Top view)



86Pin TSOP (II)
(400mil x 875mil)
(0.5 mm Pin pitch)

PIN FUNCTION DESCRIPTION

| Pin | Name | Input Function |
|-------------------------|---------------------------------|--|
| CLK | <i>System clock</i> | Active on the positive going edge to sample all inputs. |
| $\overline{\text{CS}}$ | <i>Chip select</i> | Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM. |
| CKE | <i>Clock enable</i> | Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disables input buffers for power down mode. |
| A0 ~ A10 | <i>Address</i> | Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA10, Column address : CA0 ~ CA7 |
| BA0,1 | <i>Bank select address</i> | Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time. |
| $\overline{\text{RAS}}$ | <i>Row address strobe</i> | Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge. |
| $\overline{\text{CAS}}$ | <i>Column address strobe</i> | Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access. |
| $\overline{\text{WE}}$ | <i>Write enable</i> | Enables write operation and <u>row precharge</u> . Latches data in starting from CAS, WE active. |
| DQM0 ~ 3 | <i>Data input/output mask</i> | Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active. |
| DQ0 ~ 31 | <i>Data input/output</i> | Data inputs/outputs are multiplexed on the same pins. |
| VDD/VSS | <i>Power supply/ground</i> | Power and ground for the input buffers and the core logic. |
| VDDQ/VSSQ | <i>Data output power/ground</i> | Isolated power supply and ground for the output buffers to provide improved noise immunity. |
| NC | <i>No Connection</i> | This pin is recommended to be left No connection on the device. |

ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Value | Unit |
|---------------------------------------|------------------------------------|------------|------|
| Voltage on any pin relative to Vss | V _{IN} , V _{OUT} | -1.0 ~ 4.6 | V |
| Voltage on VDD supply relative to Vss | VDD, VDDQ | -1.0 ~ 4.6 | V |
| Storage temperature | T _{STG} | -55 ~ +150 | °C |
| Power dissipation | P _D | 1 | W |
| Short circuit current | I _{OS} | 50 | mA |

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70°C)

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|---------------------------|-----------------|------|-----|----------|------|------------------------|
| Supply voltage | VDD, VDDQ | 3.0 | 3.3 | 3.6 | V | |
| Input logic high voltage | V _{IH} | 2.0 | 3.0 | VDDQ+0.3 | V | 1 |
| Input logic low voltage | V _{IL} | -0.3 | 0 | 0.8 | V | 2 |
| Output logic high voltage | V _{OH} | 2.4 | - | - | V | I _{OH} = -2mA |
| Output logic low voltage | V _{OL} | - | - | 0.4 | V | I _{OL} = 2mA |
| Input leakage current | I _{LI} | -10 | - | 10 | uA | 3 |

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ VDDQ,
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.
4. The VDD condition of K4S643232F-45/50/55/60 is 3.135V ~ 3.6V

CAPACITANCE (VDD = 3.3V, T_A = 23°C, f = 1MHz, VREF = 1.4V ± 200 mV)

| Pin | Symbol | Min | Max | Unit |
|----------------------------|--------|-----|-----|------|
| Clock | CCLK | - | 4 | pF |
| RAS, CAS, WE, CS, CKE, DQM | CIN | - | 4.5 | pF |
| Address | CADD | - | 4.5 | pF |
| DQ0 ~ DQ31 | COUT | - | 6.5 | pF |

DC CHARACTERISTICS

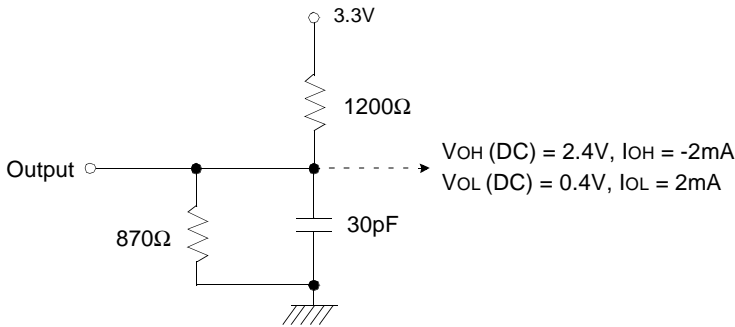
(Recommended operating condition unless otherwise noted, $T_A = 0$ to 70°C , $V_{IH(\min)}/V_{IL(\max)}=2.0\text{V}/0.8\text{V}$)

| Parameter | Symbol | Test Condition | CAS Latency | Speed | | | | | Unit | Note |
|---|--------------------|--|-------------|-------|-----|-----|-----|-----|------|------|
| | | | | -45 | -50 | -55 | -60 | -70 | | |
| Operating Current (One Bank Active) | I _{CC1} | Burst Length =1 $t_{RC} \geq t_{RC(\min)}$, $t_{CC} \geq t_{CC(\min)}$, $I_o = 0\text{mA}$ | 3 | 140 | 140 | 140 | 130 | 130 | mA | 2 |
| | | | 2 | 110 | | | | | | |
| Precharge Standby Current in power-down mode | I _{CC2P} | $\text{CKE} \leq V_{IL(\max)}$, $t_{CC} = 15\text{ns}$ | 2 | | | | | mA | | |
| | I _{CC2PS} | $\text{CKE} \ \& \ \text{CLK} \leq V_{IL(\max)}$, $t_{CC} = \infty$ | 2 | | | | | | | |
| Precharge Standby Current in non power-down mode | I _{CC2N} | $\text{CKE} \geq V_{IH(\min)}$, $\overline{\text{CS}} \geq V_{IH(\min)}$, $t_{CC} = 15\text{ns}$ Input signals are changed one time during 30ns | 12 | | | | | mA | | |
| | I _{CC2NS} | $\text{CKE} \geq V_{IH(\min)}$, $\text{CLK} \leq V_{IL(\max)}$, $t_{CC} = \infty$ Input signals are stable | 7 | | | | | | | |
| Active Standby Current in power-down mode | I _{CC3P} | $\text{CKE} \leq V_{IL(\max)}$, $t_{CC} = 15\text{ns}$ | 4 | | | | | mA | | |
| | I _{CC3PS} | $\text{CKE} \leq V_{IL(\max)}$, $t_{CC} = \infty$ | 4 | | | | | | | |
| Active Standby Current in non power-down mode (One Bank Active) | I _{CC3N} | $\text{CKE} \geq V_{IH(\min)}$, $\overline{\text{CS}} \geq V_{IH(\min)}$, $t_{CC} = 15\text{ns}$ Input signals are changed one time during 30ns | 40 | | | | | mA | | |
| | I _{CC3NS} | $\text{CKE} \geq V_{IH(\min)}$, $\text{CLK} \leq V_{IL(\max)}$, $t_{CC} = \infty$ Input signals are stable | 35 | | | | | | | |
| Operating Current (Burst Mode) | I _{CC4} | $I_o = 0 \text{ mA}$, Page Burst All bank Activated, $t_{CCD} = t_{CCD(\min)}$ | 3 | 180 | 170 | 160 | 150 | 140 | mA | 2 |
| | | | 2 | 120 | | | | | | |
| Refresh Current | I _{CC5} | $t_{RC} \geq t_{RC(\min)}$ | 3 | 150 | 150 | 150 | 140 | 120 | mA | 3 |
| | | | 2 | 120 | | | | | | |
| Self Refresh Current | I _{CC6} | $\text{CKE} \leq 0.2\text{V}$ | 2 | | | | | mA | 4 | |
| | | | 450 | | | | | | | uA |

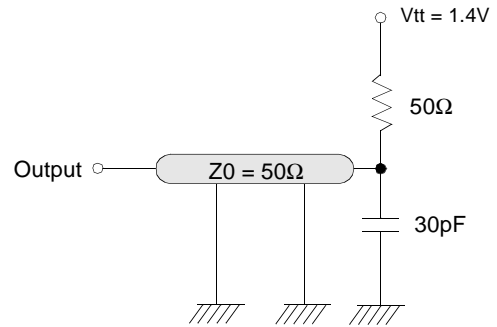
- Notes :**
1. Unless otherwise notes, Input level is CMOS($V_{IH}/V_{IL}=V_{DDQ}/V_{SSQ}$) in LVTTTL.
 2. Measured with outputs open.
 3. Refresh period is 64ms.
 4. K4S643232F-TC**
 5. K4S643232F-TL**

AC OPERATING TEST CONDITIONS ($V_{DD} = 3.3V \pm 0.3V$, $T_A = 0$ to $70^\circ C$)

| Parameter | Value | Unit |
|---|-----------------|------|
| AC input levels (V_{ih}/V_{il}) | 2.4/0.4 | V |
| Input timing measurement reference level | 1.4 | V |
| Input rise and fall time | $t_r/t_f = 1/1$ | ns |
| Output timing measurement reference level | 1.4 | V |
| Output load condition | See Fig. 2 | |



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

Notes : 1. The V_{DD} condition of K4S643232F-45/50/55/60 is 3.135V ~ 3.6V

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

| Parameter | Symbol | Version | | | | | | | | | | Unit | Note |
|---------------------------------------|---------------|---------|----|-----|----|-----|----|-----|----|-----|----|------|------|
| | | -45 | | -50 | | -55 | | -60 | | -70 | | | |
| CAS Latency | CL | 3 | 2 | 3 | 2 | 3 | 2 | 3 | 2 | 3 | 2 | CLK | |
| CLK cycle time | tCC(min) | 4.5 | 10 | 5 | 10 | 5.5 | 10 | 6 | 10 | 7 | 10 | ns | |
| Row active to row active delay | tRRD(min) | 2 | | | | | | | | | | CLK | 1 |
| RAS to CAS delay | tRCD(min) | 4 | 2 | 3 | 2 | 3 | 2 | 3 | 2 | 3 | 2 | CLK | 1 |
| Row precharge time | tRP(min) | 4 | 2 | 3 | 2 | 3 | 2 | 3 | 2 | 3 | 2 | CLK | 1 |
| Row active time | tRAS(min) | 9 | 5 | 8 | 5 | 7 | 5 | 7 | 5 | 7 | 5 | CLK | 1 |
| | tRAS(max) | 100 | | | | | | | | | | us | |
| Row cycle time | tRC(min) | 13 | 7 | 11 | 7 | 10 | 7 | 10 | 7 | 10 | 7 | CLK | 1 |
| Last data in to row precharge | tRDL(min) | 2 | | | | | | | | | | CLK | 2 |
| Last data in to new col.address delay | tCDL(min) | 1 | | | | | | | | | | CLK | 2 |
| Last data in to burst stop | tBDL(min) | 1 | | | | | | | | | | CLK | 2 |
| Col. address to col. address delay | tCCD(min) | 1 | | | | | | | | | | CLK | 3 |
| Mode Register Set cycle time | tMRS(min) | 2 | | | | | | | | | | CLK | |
| Number of valid output data | CAS Latency=3 | 2 | | | | | | | | | | ea | 4 |
| | CAS Latency=2 | 1 | | | | | | | | | | | |

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer. Refer to the following ns-unit based AC table.

| Parameter | Symbol | Version | | | | | Unit |
|--------------------------------|-----------|---------|-----|------|-----|-----|------|
| | | -45 | -50 | -55 | -60 | -70 | |
| Row active to row active delay | tRRD(min) | 9 | 10 | 11 | 12 | 14 | ns |
| RAS to CAS delay | tRCD(min) | 18 | 15 | 16.5 | 18 | 20 | ns |
| Row precharge time | tRP(min) | 18 | 15 | 16.5 | 18 | 20 | ns |
| Row active time | tRAS(min) | 40.5 | 40 | 38.5 | 42 | 49 | ns |
| | tRAS(max) | 100 | | | | | us |
| Row cycle time | tRC(min) | 58.5 | 55 | 55 | 60 | 70 | ns |

2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

| Parameter | | Symbol | -45 | | -50 | | -55 | | -60 | | -70 | | Unit | Note |
|---------------------------|---------------|--------|------|------|-----|------|-----|------|-----|------|------|------|------|------|
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | | |
| CLK cycle time | CAS Latency=3 | tCC | 4.5 | 1000 | 5 | 1000 | 5.5 | 1000 | 6 | 1000 | 7 | 1000 | ns | 1 |
| | CAS Latency=2 | | 10 | | 10 | | 10 | | 10 | | 10 | | | |
| CLK to valid output delay | CAS Latency=3 | tSAC | - | 4.0 | - | 4.5 | - | 5.0 | - | 5.5 | - | 5.5 | ns | 1, 2 |
| | CAS Latency=2 | | - | 6 | - | 6 | - | 6 | - | 6 | - | 6 | | |
| Output data hold time | | tOH | 2 | - | 2 | - | 2 | - | 2 | - | 2 | - | ns | 2 |
| CLK high pulse width | CAS Latency=3 | tCH | 1.75 | - | 2 | - | 2 | - | 2.5 | - | 3 | - | ns | 3 |
| | CAS Latency=2 | | 3 | - | 3 | - | 3 | - | 3 | - | 3 | - | | |
| CLK low pulse width | CAS Latency=3 | tCL | 1.75 | - | 2 | - | 2 | - | 2.5 | - | 3 | - | ns | 3 |
| | CAS Latency=2 | | 3 | - | 3 | - | 3 | - | 3 | - | 3 | - | | |
| Input setup time | CAS Latency=3 | tSS | 1.2 | - | 1.5 | - | 1.5 | - | 1.5 | - | 1.75 | - | ns | 3 |
| | CAS Latency=2 | | 2.5 | - | 2.5 | - | 2.5 | - | 2.5 | - | 2.5 | - | | |
| Input hold time | | tSH | 1 | - | 1 | - | 1 | - | 1 | - | 1 | - | ns | 3 |
| CLK to output in Low-Z | | tSLZ | 1 | - | 1 | - | 1 | - | 1 | - | 1 | - | ns | 2 |
| CLK to output in Hi-Z | CAS latency=3 | tSHZ | - | 4.0 | - | 4.5 | - | 5.0 | - | 5.5 | - | 5.5 | ns | - |
| | CAS latency=2 | | - | 6 | - | 6 | - | 6 | - | 6 | - | 6 | | |

- Note :**
1. Parameters depend on programmed CAS latency.
 2. If clock rising time is longer than 1ns, $(tr/2-0.5)ns$ should be added to the parameter.
 3. Assumed input rise and fall time $(tr \ \& \ tf)=1ns$.
If $tr \ \& \ tf$ is longer than 1ns, transient time compensation should be considered, i.e., $[(tr + tf)/2-1]ns$ should be added to the parameter.

SIMPLIFIED TRUTH TABLE

| Command | | CKEn-1 | CKEn | \overline{CS} | \overline{RAS} | \overline{CAS} | \overline{WE} | DQM | BA _{0,1} | A _{10/AP} | A _{9 ~ A₀} | Note | |
|------------------------------------|------------------------|--------|------|-----------------|------------------|------------------|-----------------|-----|-------------------|--------------------|---|------|---|
| Register | Mode register set | H | X | L | L | L | L | X | OP code | | | 1,2 | |
| Refresh | Auto refresh | H | H | L | L | L | H | X | X | | | 3 | |
| | Entry | | L | | | | | | | | | 3 | |
| | Self refresh | Exit | L | H | L | H | H | H | X | X | | | 3 |
| | | | | | H | X | X | X | | | | | 3 |
| Bank active & row addr. | | H | X | L | L | H | H | X | V | Row address | | | |
| Read & column address | Auto precharge disable | H | X | L | H | L | H | X | V | L | Column address (A ₀ ~ A ₇) | 4 | |
| | Auto precharge enable | | | | | | | | | H | | 4,5 | |
| Write & column address | Auto precharge disable | H | X | L | H | L | L | X | V | L | Column address (A ₀ ~ A ₇) | 4 | |
| | Auto precharge enable | | | | | | | | | H | | 4,5 | |
| Burst Stop | | H | X | L | H | H | L | X | X | | | 6 | |
| Precharge | Bank selection | H | X | L | L | H | L | X | V | L | X | | |
| | All banks | | | | | | | | X | H | | | |
| Clock suspend or active power down | Entry | H | L | H | X | X | X | X | X | | | | |
| | | | | L | V | V | V | | | | | | |
| Precharge power down mode | Entry | H | L | H | X | X | X | X | X | | | | |
| | | | | L | H | H | H | | | | | | |
| | Exit | L | H | H | X | X | X | X | | | | | |
| | | | | L | V | V | V | | | | | | |
| DQM | | H | X | | | | | V | X | | 7 | | |
| No operation command | | H | X | H | X | X | X | X | X | | | | |
| | | | | L | H | H | H | | | | | | |

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Notes :1. OP Code : Operand codeA₀ ~ A₁₀ & BA₀ ~ BA₁ : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 CLK cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA₀ ~ BA₁ : Bank select addresses.If both BA₀ and BA₁ are "Low" at read, write, row active and precharge, bank A is selected.If both BA₀ is "Low" and BA₁ is "High" at read, write, row active and precharge, bank B is selected.If both BA₀ is "High" and BA₁ is "Low" at read, write, row active and precharge, bank C is selected.If both BA₀ and BA₁ are "High" at read, write, row active and precharge, bank D is selected.If A_{10/AP} is "High" at row precharge, BA₀ and BA₁ is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

New row active of the associated bank can be issued at t_{RP} after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

MODE REGISTER FIELD TABLE TO PROGRAM MODES

Register Programmed with MRS

| Address | BA0 ~ BA1 | A10/AP | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
|----------|-----------|--------|-------|----|----|-------------|----|----|----|--------------|----|----|
| Function | RFU | RFU | W.B.L | TM | | CAS Latency | | | BT | Burst Length | | |

| Test Mode | | | CAS Latency | | | | Burst Type | | Burst Length | | | | |
|---------------------------|------------|-------------------|-------------|----|----|----------|------------|------------|--------------|----|----|-----------|----------|
| A8 | A7 | Type | A6 | A5 | A4 | Latency | A3 | Type | A2 | A1 | A0 | BT = 0 | BT = 1 |
| 0 | 0 | Mode Register Set | 0 | 0 | 0 | Reserved | 0 | Sequential | 0 | 0 | 0 | 1 | 1 |
| 0 | 1 | Reserved | 0 | 0 | 1 | Reserved | 1 | Interleave | 0 | 0 | 1 | 2 | 2 |
| 1 | 0 | Reserved | 0 | 1 | 0 | 2 | 0 | | 1 | 0 | 4 | 4 | |
| 1 | 1 | Reserved | 0 | 1 | 1 | 3 | | | 0 | 1 | 1 | 8 | 8 |
| Write Burst Length | | | 1 | 0 | 0 | Reserved | | | 1 | 0 | 0 | Reserved | Reserved |
| A9 | Length | | 1 | 0 | 1 | Reserved | | | 1 | 0 | 1 | Reserved | Reserved |
| 0 | Burst | | 1 | 1 | 0 | Reserved | | | 1 | 1 | 0 | Reserved | Reserved |
| 1 | Single Bit | | 1 | 1 | 1 | Reserved | | | 1 | 1 | 1 | Full Page | Reserved |

Full Page Length : x32 (256)

POWER UP SEQUENCE

SDRAMs must be powered up and initialized in a predefined manner to prevent undefined operations.

1. Apply power and start clock. Must maintain CKE= "H", DQM= "H" and the other pins are NOP condition at the inputs.
 2. Maintain stable power, stable clock and NOP input condition for a minimum of 200us.
 3. Issue precharge commands for all banks of the devices.
 4. Issue 2 or more auto-refresh commands.
 5. Issue a mode register set command to initialize the mode register.
- cf.) Sequence of 4 & 5 is regardless of the order.

The device is now ready for normal operation.

- Note :**
1. If A9 is high during MRS cycle, "Burst Read Single Bit Write" function will be enabled.
 2. RFU (Reserved for future use) should stay "0" during MRS cycle.

BURST SEQUENCE (BURST LENGTH = 4)

| Initial Address | | Sequential | | | | Interleave | | | |
|-----------------|----|------------|---|---|---|------------|---|---|---|
| A1 | A0 | | | | | | | | |
| 0 | 0 | 0 | 1 | 2 | 3 | 0 | 1 | 2 | 3 |
| 0 | 1 | 1 | 2 | 3 | 0 | 1 | 0 | 3 | 2 |
| 1 | 0 | 2 | 3 | 0 | 1 | 2 | 3 | 0 | 1 |
| 1 | 1 | 3 | 0 | 1 | 2 | 3 | 2 | 1 | 0 |

BURST SEQUENCE (BURST LENGTH = 8)

| Initial Address | | | Sequential | | | | | | | | Interleave | | | | | | | |
|-----------------|----|----|------------|---|---|---|---|---|---|---|------------|---|---|---|---|---|---|---|
| A2 | A1 | A0 | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| 0 | 0 | 1 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 0 | 1 | 0 | 3 | 2 | 5 | 4 | 7 | 6 |
| 0 | 1 | 0 | 2 | 3 | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 | 0 | 1 | 6 | 7 | 4 | 5 |
| 0 | 1 | 1 | 3 | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 | 2 | 1 | 0 | 7 | 6 | 5 | 4 |
| 1 | 0 | 0 | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 |
| 1 | 0 | 1 | 5 | 6 | 7 | 0 | 1 | 2 | 3 | 4 | 5 | 4 | 7 | 6 | 1 | 0 | 3 | 2 |
| 1 | 1 | 0 | 6 | 7 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 4 | 5 | 2 | 3 | 0 | 1 |
| 1 | 1 | 1 | 7 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

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