



LB1876

Three-Phase Brushless Motor Driver for Polygon Mirror Motors

Preliminary

Overview

The LB1876 is a driver for polygon mirror motors such as used in laser printers and similar equipment. It incorporates all necessary circuitry (speed control + driver) on a single chip. Direct PWM drive enables drive with low power loss.

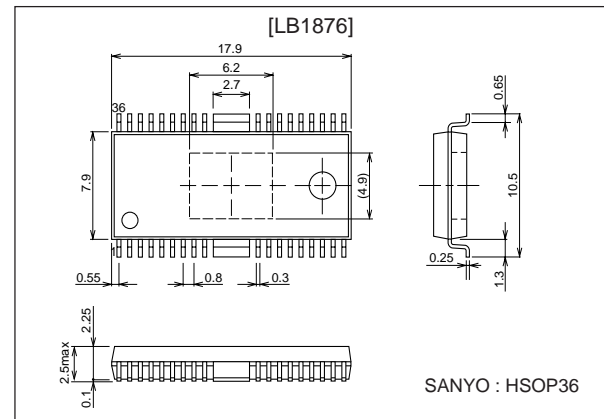
Functions and Features

- Three-phase bipolar drive
- Direct PWM drive technique
- Built-in lower side output diode
- Output current limiter
- Reference clock input circuit (FG frequency equivalent)
- PLL speed control circuit
- Phase lock detector output (with masking function)
- Built-in protection circuitry includes current limiter, restraint protection, overheat protection, low-voltage protection, etc.
- Brake method switching circuit (free-run or reverse torque)
- 5V regulator output
- Power save function

Package Dimensions

unit: mm

3235-HSOP36



Specifications

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage 1	$V_{CC\max}$		30	V
Maximum output current	$I_{O\max}$	$T \leq 500\text{ ms}$	2.5	A
Allowable power dissipation 1	$P_d\max1$	IC only	0.9	W
Allowable power dissipation 2	$P_d\max2$	*With substrate	2.1	W
Operating temperature	T_{opr}		-20 to +80	$^\circ\text{C}$
Storage temperature	T_{stg}		-55 to +150	$^\circ\text{C}$

*Substrate: $114.3 \times 76.1 \times 1.6\text{ mm}^3$, glass epoxy

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Allowable Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage range	Vcc		9.5 to 28	V
5V regulated output current	I _{REG}		0 to -20	mA
LD pin voltage	VLD		0 to 28	V
LD pin output current	ILD		0 to 15	mA
FGS pin voltage	VFGS		0 to 28	V
FGS pin output current	IFGS		0 to 10	mA

Electrical Characteristics at Ta = 25°C, Vcc = VM = 24V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Power supply current 1	I _{cc 1}			17		mA
Power supply current 2	I _{cc 2}	in STOP mode		4		mA
[5V regulated output]						
Output voltage	V _{REG}		4.65	5.0	5.35	V
Voltage fluctuation	ΔV _{REG1}	V _{cc} = 9.5 to 28V		40	100	mV
Load fluctuation	ΔV _{REG2}	I _o = -5 to -20 mA		30	100	mV
Temperature coefficient	ΔV _{REG3}	Design target value		0		mV/°C
[Output block]						
Output saturation voltage 1	V _{osat1}	I _o = 1.0A, V _o (SINK)+V _o (SOURCE)		2.2		V
Output saturation voltage 2	V _{osat2}	I _o = 2.0A, V _o (SINK)+V _o (SOURCE)		2.8		V
Output leak current	I _{oleak}				100	μA
Lower side diode forward voltage 1	V _{D1}	I _D = -1.0A		1.2		V
Lower side diode forward voltage 2	V _{D2}	I _D = -2.0A		1.5		V
[Hall amplifier block]						
Input bias current	I _{HB}		-4	-1		μA
Common mode input voltage range	V _{ICM}		0		V _{REG} -2.0	V
Hall input sensitivity			80			mVp-p
Hysteresis width	ΔV _{IN}		15	24	42	mV
Input voltage L->H	V _{SLH}			12		mV
Input voltage H->L	V _{SHL}			-12		mV
[FG/Schmitt block]						
Input bias current	I _B (FGS)		-4	-1		μA
Common mode input voltage range	V _{ICM} (FGS)		0		V _{REG} -2.0	V
Input sensitivity	V _{IN} (FGS)		80			mVp-p
Hysteresis width	ΔV _{IN} (FGS)	Design target value	15	24	42	mV
Input voltage L->H	V _{SLH} (FGS)	Design target value		12		mV
Input voltage H->L	V _{SHL} (FGS)	Design target value		-12		mV
[PWM oscillator]						
Output High level voltage	V _{OH} (PWM)		2.5	2.8	3.1	V
Output Low level voltage	V _{OL} (PWM)		1.2	1.5	1.8	V
Oscillator frequency	f(PWM)	C = 3900 pF		18		kHz
Amplitude	V(PWM)		1.05	1.30	1.55	Vp-p

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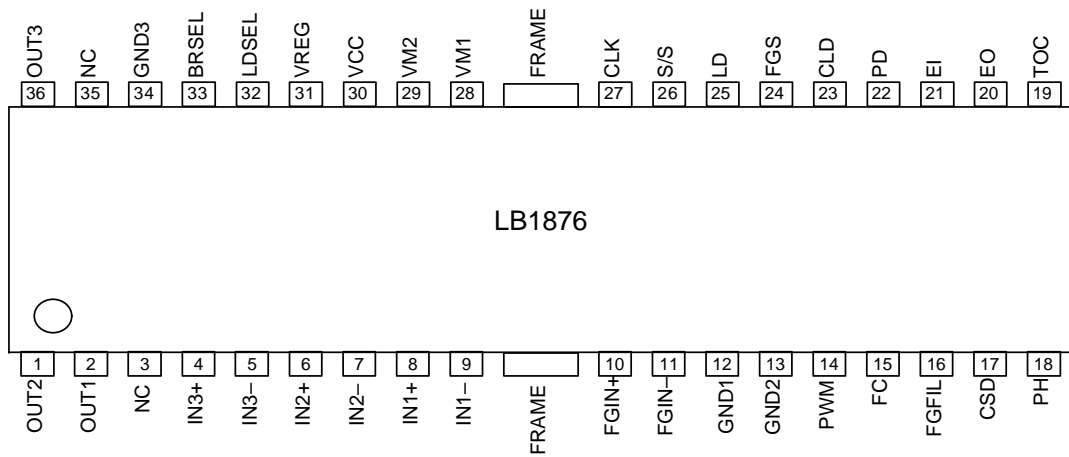
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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[FGS output]						
Output saturation voltage	VOL(FGS)	IFGS = 7 mA		0.15	0.5	V
Output leak current	IL(FGS)	VO = V _{CC}			10	μA
[CSD oscillator]						
Output High level voltage	VOH(CSD)			3.0		V
Output Low level voltage	VOL(CSD)			0.9		V
Amplitude	V(CSD)			2.1		V _{p-p}
External capacitor charge current	ICHG1			-9		μA
External capacitor discharge current	ICHG2			9		μA
Oscillator frequency	f(CSD)	C = 0.068 μF		30		Hz
[Phase comparator output]						
Output High level voltage	VPDH	IOH = -100 μA	VREG-0.2	VREG-0.1		V
Output Low level voltage	VPDL	IOH = 100 μA		0.2	0.3	V
Output source current	IPD+	VPD = VREG/2			-0.5	mA
Output sink current	IPD-	VPD = VREG/2	1.5			mA
[Phase lock detector output]						
Output saturation voltage	VOL(LD)	ILD = 10 mA		0.15	0.5	V
Output leak current	IL(LD)	VO = V _{CC}			10	μA
[ERR amplifier]						
Input offset voltage	VIO(ER)	Design target value	-10		10	mV
Input bias current	IB(ER)		-1		1	μA
Output High level voltage	VOH(ER)	IOH = -500 μA	VREG-1.2	VREG-0.9		V
Output Low level voltage	VOL(ER)	IOL = 500 μA		0.9	1.2	V
DC bias level	VB(ER)		-5%	VREG/2	5%	V
[Current limiter]						
Drive gain 1	GDF1	in phase lock mode	0.4	0.5	0.6	times
Drive gain 2	GDF2	in unlock mode	0.8	1.0	1.2	times
Limiter voltage	VRF	V _{CC} -VM	0.45	0.5	0.55	V
[Thermal shutdown operation]						
Thermal shutdown operating temperature	TSD	Design target value (junction temperature)	150	180		°C
Hysteresis width	ΔTSD	Design target value (junction temperature)		40		°C
[CLK pin]						
External input frequency	fI(CKIN)		0.1		10	kHz
High level input voltage	VIH(CKIN)		3.5		VREG	V
Low level input voltage	VIL(CKIN)		0		1.5	V
Input open voltage	VIO(CKIN)		VREG-0.5		VREG	V
Hysteresis width	VIS(CKIN)		0.35	0.5	0.65	V
High level input current	IIH(CKIN)	VCKIN = VREG	-10	0	10	μA
Low level input current	IIL(CKIN)	VCKIN = 0V	-280	-210		μA
[S/S pin]						
High level input voltage	VIH(SS)		3.5		VREG	V
Low level input voltage	VIL(SS)		0		1.5	V
Input open voltage	VIO(SS)		VREG-0.5		VREG	V
Hysteresis width	VIS(SS)		0.35	0.5	0.65	V
High level input current	IIH(SS)	VS/S = VREG	-10	0	10	μA
Low level input current	IIL(SS)	VS/S = 0V	-280	-210		μA

Three-phase logic truth table (IN = "H" indicates the IN+ > IN- condition)

IN1	IN2	IN3	OUT1	OUT2	OUT3
H	L	H	L	H	M
H	L	L	L	M	H
H	H	L	M	L	H
L	H	L	H	L	M
L	H	H	H	M	L
L	L	H	M	H	L

Pin Assignment



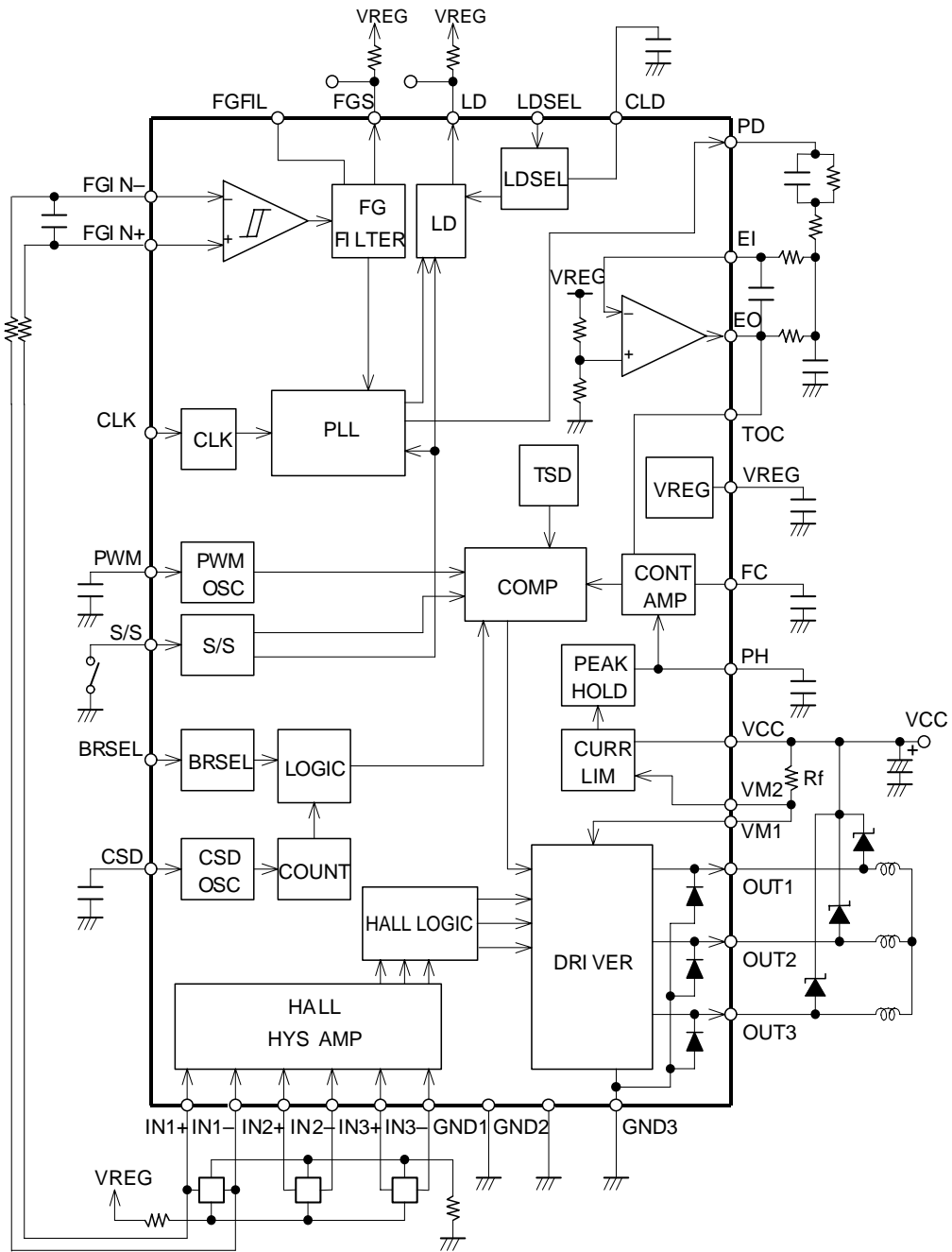
Top view



Pin Description

Pin name	Pin number	
OUT1	2	Output pins for external lower side transistor drive.
OUT2	1	PWM controls duty cycle ratio by lower transistors.
OUT3	36	Connect Schottky diode between these pins and VCC.
IN1+, IN1-	8,9	Hall input pins for each phase.
IN2+, IN2-	6,7	Logic High indicates VIN+ > VIN-.
IN3+, IN3-	4,5	
FG IN+	10	FG comparator non-inverting input.
FG IN-	11	FG comparator inverting input.
GND1	12	Control circuit ground.
GND2	13	Sub-ground.
PWM	14	PWM oscillation frequency setting pin. Connect to ground via capacitor.
FC	15	Current control circuit frequency characteristics compensation pin. Connect to ground via capacitor.
FGFIL	16	FG filter pin. Connect to ground via capacitor if noise in FG signal is a problem.
CSD	17	Restraint protection circuit operating time setting pin/reset pulse setting pin. Connect to ground via capacitor. If the protection circuit is not to be used, connect a resistor in parallel with capacitor.
PH	18	RF waveform smoothing pin. Connect to ground via capacitor.
TOC	19	Torque specifying input pin. Normally connected to EO pin. When TOC potential falls, ON duty cycle ratio of lower side output transistors changes and torque increases.
EO	20	Error amplifier output.
EI	21	Error amplifier input.
PD	22	Phase comparator output pin. Phase deviation is output as a duty cycle change of the pulse.
CLD	23	Phase lock signal masking time setting pin. Connect to ground via capacitor. Leave open if masking is not required.
FGS	24	FG Schmitt output (open collector output).
LD	25	Phase lock detector output (open collector output). Goes ON when PLL is locked.
S/S	26	Start/stop input. Low: Start; High or Open: Stop.
CLK	27	Clock input. 10 kHz max.
VM1	28	Output block power supply. Short to VM2 for use.
VM2	29	Output current detector pin. Connect to VCC via low resistor. Set to maximum output current $I_{OUT} = 0.5/R_f$.
VCC	30	Power supply pin. Connect to ground via capacitor to prevent noise.
VREG	31	5V regulator output pin (control circuit power supply). Connect to ground via capacitor to stabilize operation.
LDSEL	32	Phase lock signal masking switching pin. When "Low", the unlock signal (short "High" signal of LD output) is masked. When "High" or Open, the lock signal (short "Low" signal of LD output) is masked.
BRSEL	33	Braking method select pin. "Low" selects reverse torque control and "High" or Open selects free-run. When reverse torque is controlled, lower side output transistors require external SBD.
GND3	34	Output circuit ground.
FRAME	—	Leave open.
NC	3,35	Not connected internally. Can be used for wiring.

Equivalent Circuit Block Diagram and Sample Application Circuit



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