



LB1955

Three-Phase Brushless Motor Driver

Functions

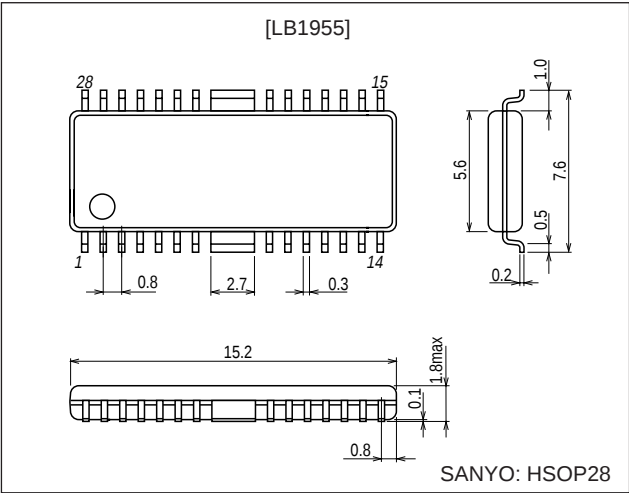
- The LB1955 is a 3-phase brushless motor driver IC that is optimal for applications such as driving the drum motor in VCRs.

Features

- Current linear drive
- FG and PG free
- Single-voltage power supply
- Built-in AGC circuit
- Built-in thermal shutdown circuit

Package Dimensions

unit: mm
3222-HSOP28



Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V _{CCmax}		14.5	V
Maximum output current	I _{OUT}		1.0	A
Allowable power dissipation	P _{dmax}	Independent device	0.60	W
Operating temperature	T _{opr}		-20 to +75	°C
Storage temperature	T _{stg}		-55 to +150	°C

Allowable Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V _{CC}		10.2 to 13.8	V
Hall input amplitude	V _{hall}	At the input	70 to 500	mVp-p
VC input voltage	V _C		0 to 5	V

■ Any and all SANYO products described or contained herein do not have specifications that can handle applications that require extremely high levels of reliability, such as life-support systems, aircraft's control systems, or other applications whose failure can be reasonably expected to result in serious physical and/or material damage. Consult with your SANYO representative nearest you before using any SANYO products described or contained herein in such applications.

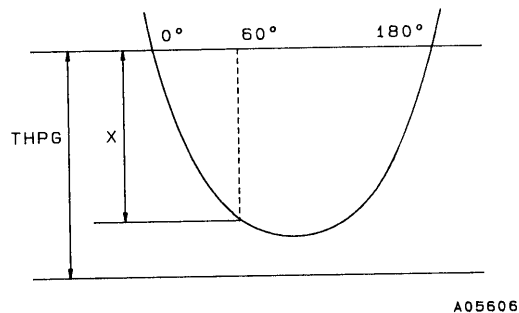
■ SANYO assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all SANYO products described or contained herein.

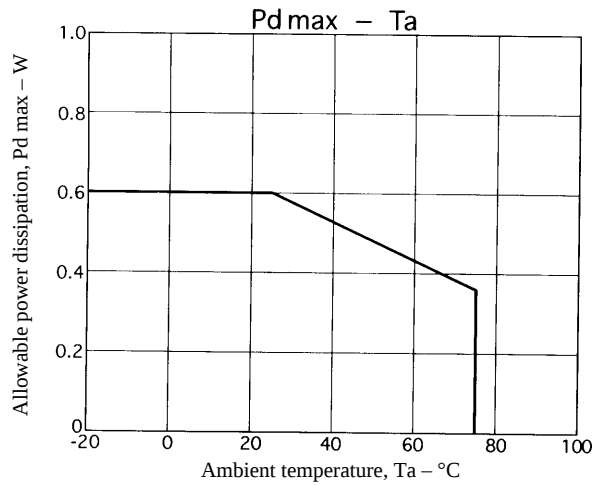
Electrical Characteristics at Ta = 25°C, V_{CC} = 12 V

Parameter	Symbol	Conditions		Ratings			Unit
				min	typ	max	
[Power Supply]							
Current drain	I _{CC}	V _C = 0 V, LCTR = 6 V		7.0	10.0	13.0	mA
IC internal power supply	V _{REF}			4.75	5.0	5.25	V
[Output]							
Output saturation voltage	V _{O(sat)1}	I _O = 400 mA	Sink side			0.4	V
		V _C = 5 V, R _f = 0 Ω	Source side			1.5	V
Output saturation voltage 2	V _{O(sat)2}	I _O = 800 mA	Sink side			0.7	V
		V _C = 5 V, R _f = 0 Ω	Source side			2.0	V
3-phase output current ripple	I _{or}	I _O = 100 mA, R _f = 0.47 Ω		−5		+5	%
[Hall Amplifier]							
Input offset voltage	V _{Hoff}			−20		+20	mV
Input bias current	I _{Hb}	V _{AGC} = 1.4 V	U _{IN}			10	μA
			V _{IN} , W _{IN}			5	μA
Common-mode input voltage range	V _{HCM}			2.2		5.0	V
[Control]							
VC pin input bias current	I _{VCb}	V _C = 0 V		−10	−1.3		μA
Control start voltage	V _{THVC}	R _f = 0.47 Ω, I _O ≥ 10 mA With the Hall input logic fixed		2.25	2.5	2.75	V
Open-loop control gain	G _{MVC}	R _f = 0.47 Ω, ΔI _O = 200 mA With the Hall input logic fixed and VG shorted to RF		0.72	0.9	1.08	A/V
[PG]							
PG Hall amplifier input offset voltage	V _{PGoff}	Design target		−10		+10	mV
Peak hold charge current	I _{SHCHG}	(U, V, W) = (L, L, H)			30		μA
PG comparator threshold	THPG	SH = 1000pF, Design target*		113	117	121	%
PG output high-level voltage	V _{PGH}			4.5		5.2	V
PG leakage current	I _{LEAKPG}			−10	0	+10	μA
[FG]							
Back emf Schmitt input hysteresis width	V _{SCHG}	In the back emf Schmitt input increasing direction, Design target			100		mV
		In the back emf Schmitt input decreasing direction, Design target			0		mV
Ringing canceller Schmitt input hysteresis width	V _{SCHR}	In the Schmitt input increasing direction, Design target			180		mV
		In the Schmitt input decreasing direction, Design target		−20	0	+20	mV
FG output high-level voltage	V _{FGH}	FGR = 0 V		4.5		5.2	V
FG leakage current	I _{LEAKFG}			−10	0	+10	μA
[TSD]							
Thermal shutdown operating temperature	TTSD	Design target			180		°C
Thermal shutdown temperature hysteresis width	ΔTSD	Design target			15		°C

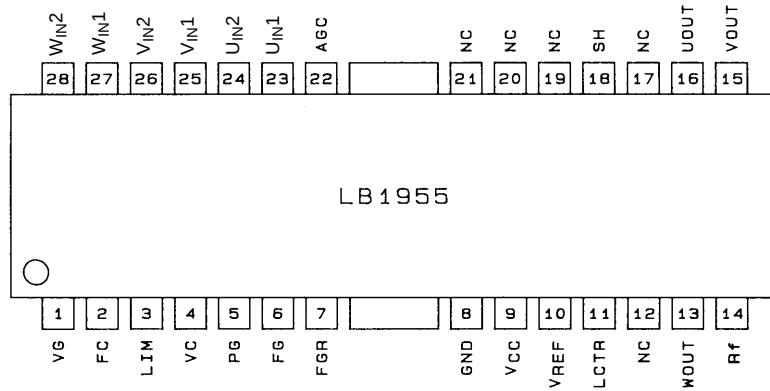
Note: * is provided for when X is the peak value at the 60° position of the lower side of the U_{IN1} Hall amplifier input: THPG = 1.17X.

However, note that the THPG level may be reduced if the value of the capacitor (SH) used for the sample-and-hold circuit is too small since a discharge current of a few nA will result.





Pin Assignment



A05605

Pin Functions

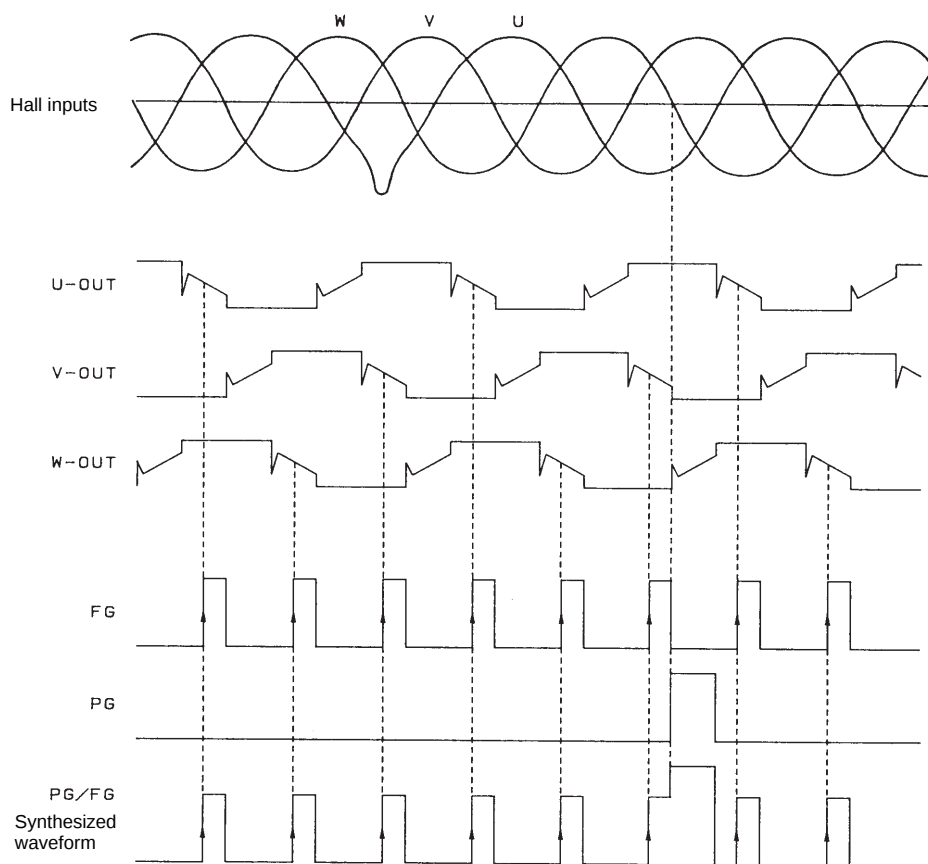
Pin No.	Pin	Function
23, 24	U_{IN1} , U_{IN2}	U phase Hall element input
25, 26	V_{IN1} , V_{IN2}	V phase Hall element input
27, 28	W_{IN1} , W_{IN2}	W phase Hall element input
16	UOUT	U phase output
15	VOUT	V phase output
13	WOUT	W phase output
11	LCTR	Pin connected to the center points of the coils that are Y-connected to the U, V, and W outputs.
9	V_{CC}	Power supply
10	V_{REF}	Reference voltage output
8	GND	GND
14	Rf	Output current detection
1	VG	Closed loop control gain switching
2	FC	Speed control loop frequency characteristics correction
3	LIM	Output current limit setting
4	VC	Speed control
5	PG	PG waveform output
6	FG	FG waveform output (FGR shorted to GND)
7	FGR	PG/FG synthesized output (FGR shorted to PG)
18	SH	PG waveform sample-and-hold circuit capacitor connection
22	AGC	Connection for the capacitor used by the AGC circuit, which holds the input gain at a fixed level.
12, 17, 19 20, 21	NC	No connection

Truth Table

	Source → sink	Hall input logic		
		U	V	W
1	W phase → V phase	H	H	L
2	W phase → U phase	H	L	L
3	V phase → U phase	H	L	H
4	V phase → W phase	L	L	H
5	U phase → W phase	L	H	H
6	U phase → V phase	L	H	L

Note: The Hall input "H" and "L" values are defined as follows: "H" means that for that phase the (+) input is higher than the (-) input, and "L" means that for that phase the (+) input is lower than the (-) input. However, note that an input potential difference corresponding to the Hall to output gain is required.

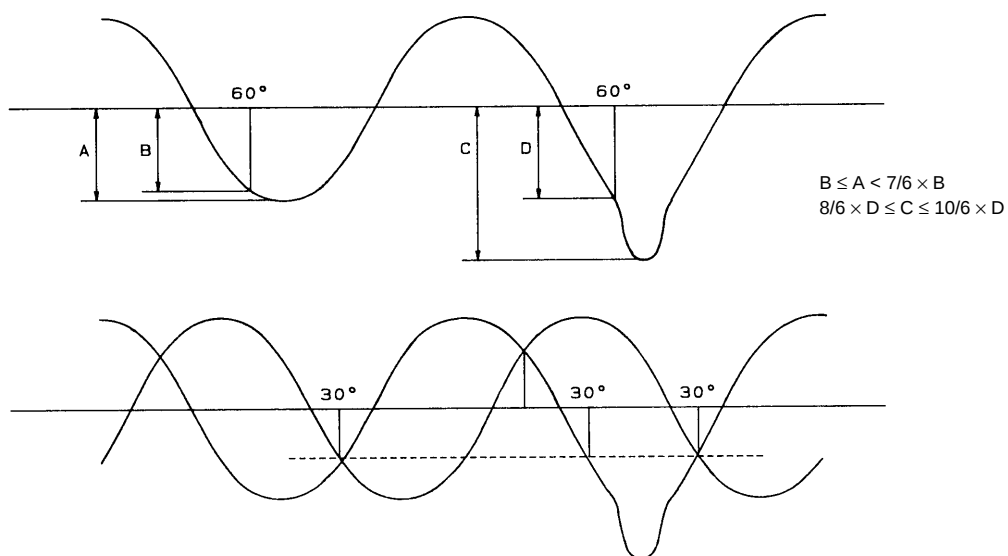
Timing Charts



A05607

Note: The Hall inputs are defined as follows: $U = U_{IN1} - U_{IN2}$, $V = V_{IN1} - V_{IN2}$, and $W = W_{IN1} - W_{IN2}$. Inputs to the Hall input pins must be applied in the phase order shown in the timing chart.

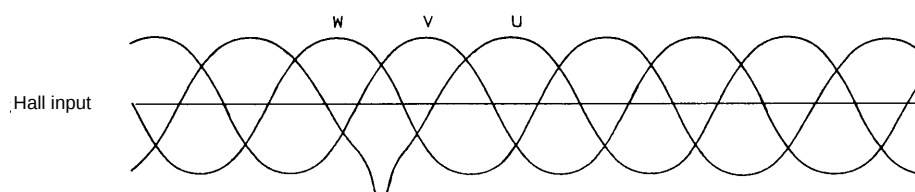
Recommended Special Magnetization Waveforms



A05608

Note: Note that the intersections between the special magnetization and general waveforms and the intersections between pairs of general waveforms must be set up to be 30° apart.

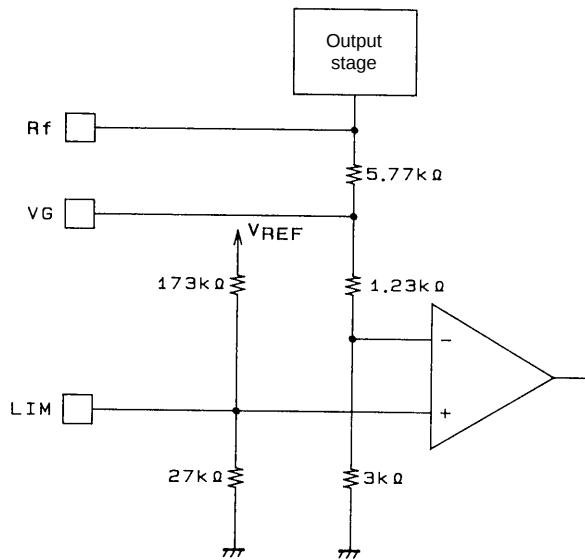
Hall Input Order



A05609

Note: The Hall input order must be set up to be $W \rightarrow V \rightarrow U$.

VG and LIM Pin Usage



LIM pin: Open
 VG – Rf: Shorted
 $G_m = 0.423/R_f$ (A/V)
 (Closed loop control gain)
 $I_{lim} = (V_{REF} \times 27/200 - 0.2) \times 4.23/3/R_f$
 (Current limit)

VG pin: Open
 $G_m = 1/R_f$ (A/V)
 (Closed loop control gain)
 $I_{lim} = (V_{REF} \times 27/200 - 0.2) \times 10/3/R_f$
 (Current limit)

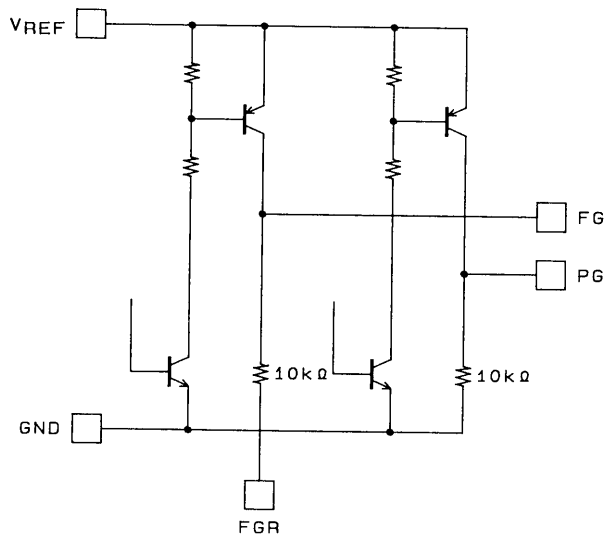
LIM – VREF: Shorted
 No current limit.

A05610

Note: This current limiting function is for protection against unusual and abnormal currents. If a current limit level below the rated current is set, this will, inversely, result in heat generation within the IC.

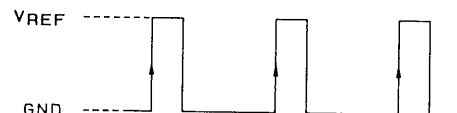
When the LIM pin is open, VG is shorted to Rf, and Rf = 0.47 Ω, this will result in a current limit level of about 1.3 to 1.4 A. If this limit falls under the rated value due to mode changes or changes in the value of the Rf resistor, set the current limit to an appropriate value by applying to the LIM pin a voltage that is divided from the VREF to ground potential by resistors of a few kΩ. Alternatively, short the LIM pin to VREF to defeat the current limit function.

PG and FG Pin Output Circuits

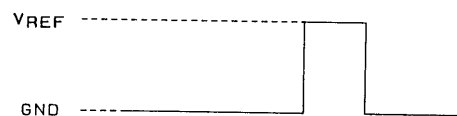


A05611

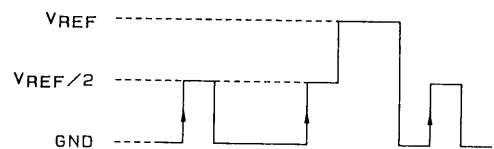
FG (FGR shorted to ground)



PG

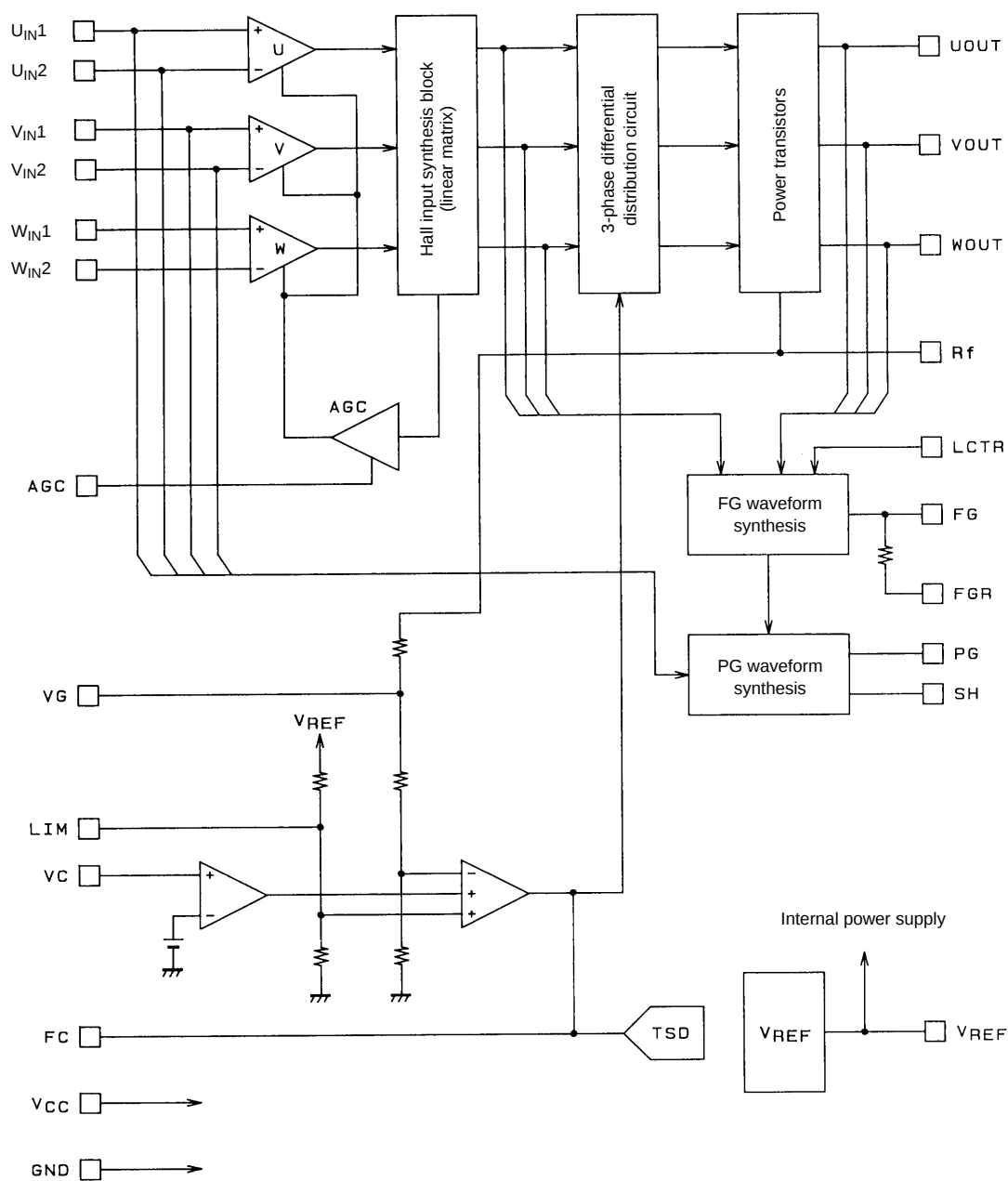


PG (FGR shorted to PG)



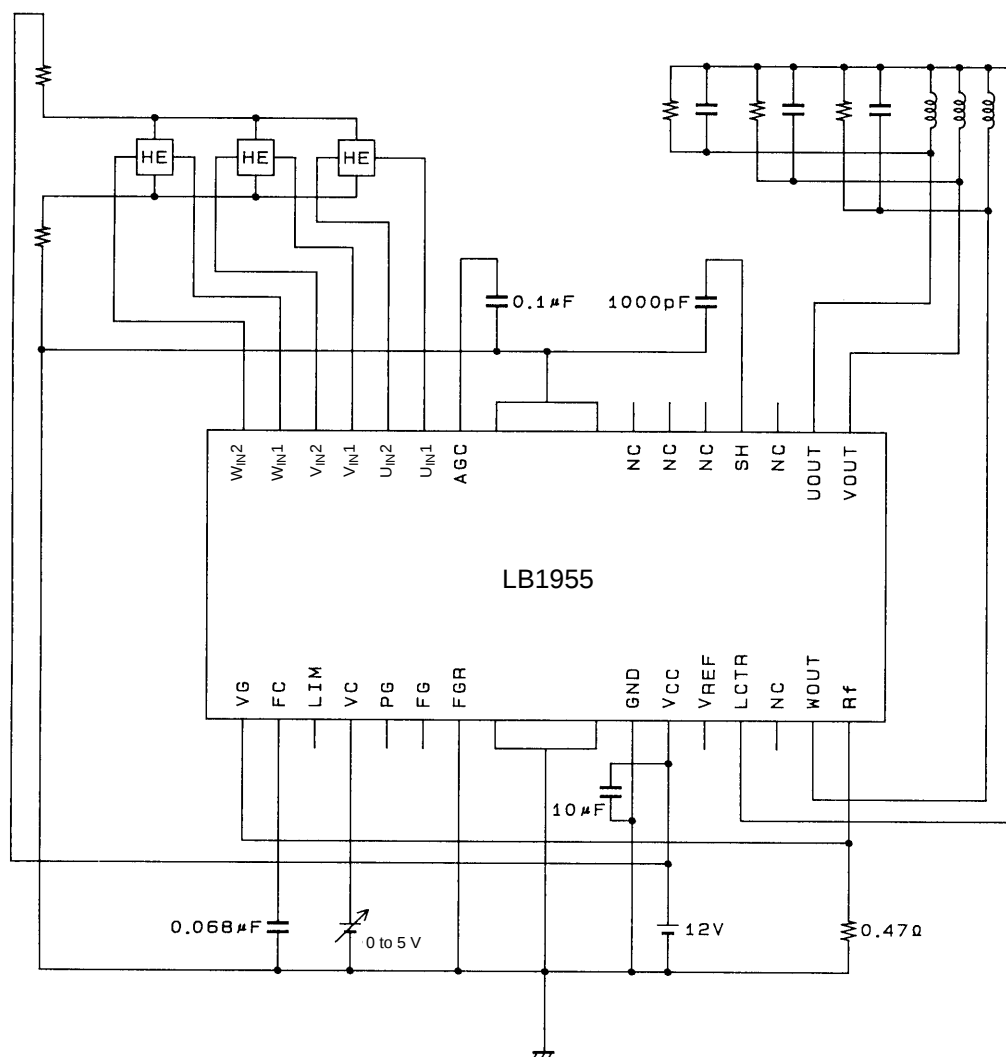
A05612

Block Diagram



A05613

Sample Application Circuit



A05614

- Specifications of any and all SANYO products described or contained herein stipulate the performance, characteristics, and functions of the described products in the independent state, and are not guarantees of the performance, characteristics, and functions of the described products as mounted in the customer's products or equipment. To verify symptoms and states that cannot be evaluated in an independent device, the customer should always evaluate and test devices mounted in the customer's products or equipment.
- SANYO Electric Co., Ltd. strives to supply high-quality high-reliability products. However, any and all semiconductor products fail with some probability. It is possible that these probabilistic failures could give rise to accidents or events that could endanger human lives, that could give rise to smoke or fire, or that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.
- In the event that any or all SANYO products (including technical data, services) described or contained herein are controlled under any of applicable local export control laws and regulations, such products must not be exported without obtaining the export license from the authorities concerned in accordance with the above law.
- No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written permission of SANYO Electric Co., Ltd.
- Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the SANYO product that you intend to use.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. SANYO believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.

This catalog provides information as of April, 1999. Specifications and information herein are subject to change without notice.