Ordering number: EN 3889C

CMOS IC

LC7152, 7152M, 7152NM, 7152KM

Universal Dual-PLL Frequency Synthesizers

Overview

The LC7152, 7152M, 7152NM, 7152KM are universal dual-PLL frequency synthesizers for use in weak signal type cordless telephone applications in the USA, South Korea, and Japan, and broadcast satellite (BS) tuners in the USA and Europe.

Features

- Dual charge pump built in for fast channel switching
- Digital lock detector enables PLL lock status check with crystal oscillator precision
- Programmable reference frequency divider supports various applications
- The LC7152NM is a built-in power-on reset circuit version of the LC7152M
- The LC7152KM is an enhanced frequency characteristics version of the LC7152M

Functions

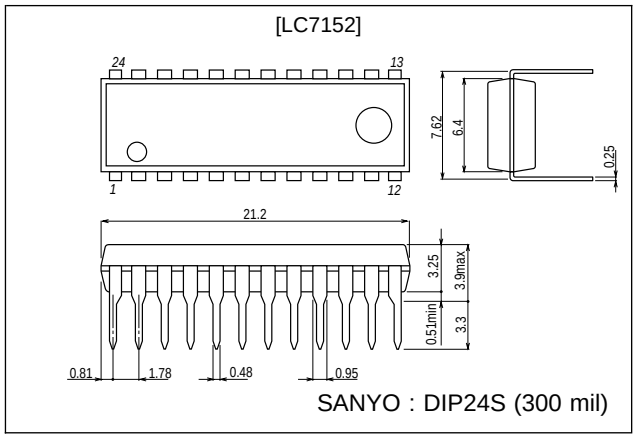
- 2-system PLL built-in (dual PLL)
- 16-bit programmable local-oscillator divider 1.5 to 55 MHz (V_{DD} = 2.0 to 3.3 V), LC7152KM: 55 to 80 MHz (V_{DD} = 2.7 to 3.3 V)
- 14-bit programmable reference-frequency divider 320 Hz to 640 kHz reference frequency using a 10.24 MHz crystal oscillator
- Digital lock detector
- Dual charge pump
- Amplifier built-in for an active LPF
- Serial transmission data input (CCB format)
- LC7152NM with power-on reset circuit (pins $\overline{\text{OUTA}}$ and $\overline{\text{OUTB}}$ become open at power-on)
- 2.0 to 3.3 V supply voltage
- DIP24S and MFP24S packages

- **CCB is a trademark of SANYO ELECTRIC CO., LTD.**
- **CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.**

Package Dimensions

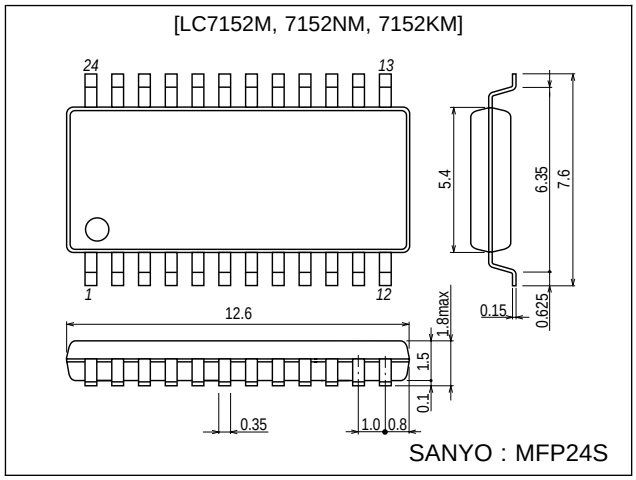
unit : mm

3067-DIP24S



unit : mm

3112-MFP24S



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Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD}max	V_{DD}	–0.3 to +7.0	V
Maximum input voltage	V_{IN}max(1)	CE, CL, DI, AIA, AIB	–0.3 to +7.0	V
	V_{IN}max(2)	XIN, PIA, PIB, TEST	–0.3 to V_{DD}+0.3	V
Maximum output voltage	$V_O$max(1)	$\overline{LDI}$, $\overline{LDB}$	–0.3 to +7.0	V
	$V_O$max(2)	AOA, AOB, $\overline{OUTA}$, $\overline{OUTB}$	–0.3 to +15	V
	$V_O$max(3)	PDA1, PDA2, PDB1, PDB2, XOUT	–0.3 to V_{DD}+0.3	V
Maximum output current	$I_O$max(1)	$\overline{LDA}$, $\overline{LDB}$, $\overline{OUTA}$, $\overline{OUTB}$	0 to 3	mA
	$I_O$max(2)	AOA, AOB	0 to 6	mA
Allowable power dissipation	Pd max	Ta≦85°C, LC7152	350	mW
		Ta≦85°C, LC7152M, 7152NM, 7152KM	160	mW
Operating temperature	Topr		–40 to +85	°C
Storage temperature	Tstg		–55 to +125	°C

Allowable Operating Ranges at Ta = –40 to +85°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}(1)	V_{DD}	2.0		3.3	V
	V_{DD}(2)	V_{DD}:Serial data retention voltage, see Figure1, *1	1.5			V
	V_{DD}(3)	V_{DD}:Power-on reset voltage, t_R≧ 20 ms, see Figure1, *1			0.05	V
Input high-level voltage	V_{IH}(1)	CE, CL, DI:V_{DD} = 2.0 V	1.5		5.5	V
	V_{IH}(2)	CE, CL, DI:V_{DD} = 3.3 V	1.7		5.5	V
Input low-level voltage	V_{IL}(1)	CE, CL, DI:V_{DD} = 2.0 V	0		0.4	V
	V_{IL}(2)	CE,CL,DI:V_{DD}= 3.3 V	0		0.6	V
Output voltage	V_O(1)	$\overline{LDA}$, $\overline{LDB}$	0		5.5	V
	V_O(2)	AOA, AOB, $\overline{OUTA}$, $\overline{OUTB}$	0		13	V
Input frequency	f_{IN}(1)	XIN:Sine wave, capacitively coupled	1.0		13	MHz
	f_{IN}(2)	PIA, PIB: Sine wave, capacitively coupled *2	1.5		55	MHz
	f_{IN}(3)	PIA, PIB: Sine wave, capacitively coupled *3	55		80	MHz
Input amplitude	V_{IN}(1)	XIN: Sine wave, capacitively coupled	200		600	mVrms
	V_{IN}(2)	PIA, PIB: Sine wave, capacitively coupled *2,3	100		600	mVrms
Crystal oscillator frequency	$f_{X'tal}$	XIN, XOUT: CI ≦ 50 Ω CL ≦ 16 pF *4	4	10.24	11	MHz

Note *1 LC7152NM

		FA/FB (serial data input frequency select bits)		V_{DD}	Device
		[0]	[1]		
*2	f_{IN}(2)	1.5 to 23 MHz	20 to 55 MHz	2.0 to 3.3 V	LC7152, 7152M, LC7152NM, 7152KM
*3	f_{IN}(3)	————	55 to 80 MHz	2.7 to 3.3 V	LC7152KM

*4 Cl is the crystal impedance and CL is the load capacitance.

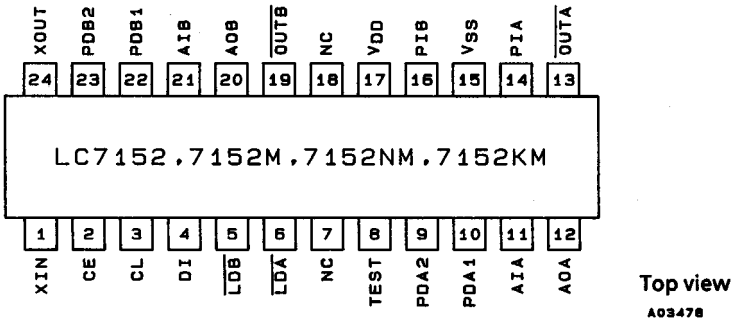
Electrical Characteristics in the allowable operating ranges

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Output high-level voltage	$V_{OH}(1)$	PDA1, PDB1: I_O = 1 mA	V_{DD} – 1.0			V
	$V_{OH}(2)$	PDA2, PDB2: I_O = 2 mA	V_{DD} – 1.0			V
Output low-level voltage	$V_{OL}(1)$	PDA1, PDB1: I_O 1 mA			1.0	V
	$V_{OL}(2)$	PDA2, PDB2: I_O = 2 mA			1.0	V
	$V_{OL}(3)$	$\overline{OUTA}$, $\overline{OUTB}$: I_O= 1 mA			1.0	V
	$V_{OL}(4)$	$\overline{LDA}$, $\overline{LDB}$: I_O = 2 mA			1.0	V
	$V_{OL}(5)$	AOA, AOB: I_O = 0.5 mA, AIA = AIB = 1.2 V			0.5	V
	$V_{OL}(6)$	AOA, AOB: I_O = 1 mA, AIA = AIB = 1.3 V			0.5	V
Output off-leakage current	$I_{OFF}(1)$	$\overline{LDA}$. $\overline{LDB}$: V_O = 5.5 V			5.0	µA
	$I_{OFF}(2)$	PDA1, PDB1, PDA2, PDB2: V_O = 0/3.3 V		0.01	10.0	nA
	$I_{OFF}(3)$	AOA, AOB, $\overline{OUTA}$, $\overline{OUTB}$: V_O = 13 V			5.0	µA
Input high-level current	$I_{IH}(1)$	CE, CL, DI: V_I = 5.5 V			5.0	µA
	$I_{IH}(2)$	XIN: V_I = 3.3 V, V_{DD} = 3.3 V	2.0		6.5	µA
	$I_{IH}(3)$	PIA, PIB: V_I = 3.3 V, V_{DD} = 3.3 V	3.5		10.0	µA
	$I_{IH}(4)$	AIA, AIB: V_I = 3.3 V		0.01	10.0	nA
	$I_{IH}(5)$	TEST: V_I = 3.3 V, V_{DD} = 3.3 V		120		µA
Input low-level current	$I_{IL}(1)$	CE, CL, DI: V_I = 0 V			5.0	µA
	$I_{IL}(2)$	XIN: V_I = 0 V, V_{DD} = 3.3 V	2.0		6.5	µA
	$I_{IL}(3)$	PIA, PIB: V_I = 0 V, V_{DD} = 3.3 V	3.5		10.0	µA
	$I_{IL}(4)$	AIA, AIB: V_I = 0 V		0.01	10.0	nA
	$I_{IL}(5)$	TEST: V_I = 0 V, V_{DD} = 3.3 V			5.0	µA
Internal feedback resistance	$R_f(1)$	XIN: V_{DD} = 3.3 V		1.0		MΩ
	$R_f(2)$	PIA, PIB:V_{DD} = 3.3 V		600		kΩ
Internal pull-down resistance	Rd	TEST: V_{DD} = 3.3 V		30		kΩ
Input capacitance	C_{IN}	XIN, PIA, PIB		2.5		pF
Supply current*1	$I_{DD}(1)$	V_{DD}(= 2.0 V):f_{IN} = 55 MHz		3.0	8.0	mA
	$I_{DD}(2)$	V_{DD}(= 3.3 V):f_{IN} = 55 MHz		7.0	14.0	mA
Supply current*2	$I_{DD}(4)$	V_{DD}(= 2.0 V):f_{IN} = 55 MHz		1.5	4.5	mA
	$I_{DD}(5)$	V_{DD}(= 3.3 V):f_{IN} = 55 MHz		3.9	8.0	mA

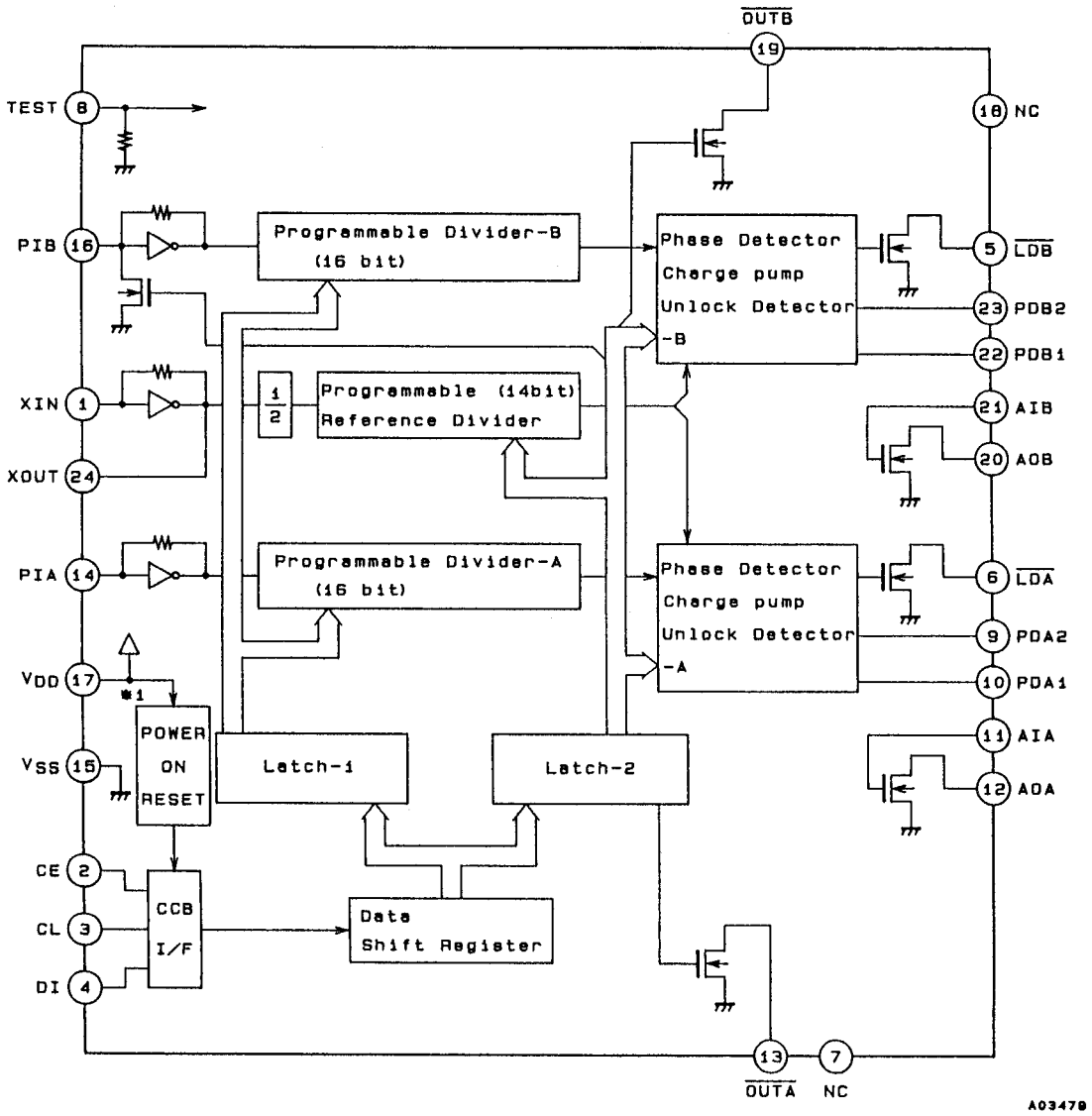
Note *1. Dual PLL operation (both PLL-A and PLL-B), SB= 0, XIN= 10.24 MHz (crystal), PIA and PIB input = 100mVrms at f_{IN}, all other inputs at V_{SS}, all other outputs open.

*2. Standby mode: Single PLL operation (PLL-A operating and PLL-B stopped), SB = 1, XIN = 10.24 MHz (crystal), PIA input = 100mVrms at f_{IN}, all other inputs at V_{SS}, all other outputs open.

Pin Assignment



Equivalent Block Diagram



Pin Functions

Symbol	Pin No.	Function		Symbol	Pin No.	Function
PIB	16	Side-B oscillator signal input		PDB2	23	Sub charge pump
XIN	1	Crystal oscillator		PDB1	22	Main charge pump
XOUT	24			AIB	21	Low-pass filter transistors
PIA	14	Side-A oscillator signal output		AOB	20	
V_{DD}	17	Power supply		$\overline{OUTB}$	19	General-purpose output port
V_{SS}	15	Ground		$\overline{LDA}$	6	Side-A unlock detection
CE	2	Serial data input	Chip enable	PDA2	9	Sub charge pump
CL	3		Clock	PDA1	10	Main charge pump
DI	4		Data	AIA	11	Low-pass filter transistors
TEST	8	IC Test		AOA	12	
NC	7, 18	No connections		$\overline{OUTA}$	13	General-purpose output port
$\overline{LDB}$	5	Side-B unlock detection				

Pin Description

<table>
<tr><th>Symbol</th><th>Pin No.</th><th>Function</th><th>Description of function</th></tr>
<tr><td>PIA</td><td>14</td><td>Side-A local oscillator signal input</td><td>• Side-A programmable divider. The input frequency ranges are as follows.
<table>
<tr><th>FA = [0]</th><th>FA = [1]</th><th>V_{DD}</th><th>Device</th></tr>
<tr><td>1.5 to 23 MHz</td><td>20 to 55 MHz</td><td>2.0 to 3.3 V</td><td>LC7152, 7152M
LC7152NM, 7152KM</td></tr>
<tr><td>————</td><td>55 to 80 MHz</td><td>2.7 to 3.3 V</td><td>LC7152KM</td></tr>
</table>
FA: Serial data
• Bits DA0 to DA15 determine the divider ratios
Divider ratio N = 272 to 65535</td></tr>
<tr><td>PIB</td><td>16</td><td>Side-B local-oscillator signal input</td><td>• Side-B programmable divider
The input frequency ranges are the same as for PIA.
FB(→ FA): Determined by the serial data
• Bits DB0 to DB15 determine the divider ratios
Divider ratio N= 272 to 65535
• Serial data: Bit SB is the standby mode control bit
When SB = 1, standby mode is selected. In standby mode, side-B is stopped, PIB is pulled down to V_{SS}.
When SB = 0, normal operation is selected.</td></tr>
<tr><td>XIN
XOUT</td><td>1
24</td><td>Crystal oscillator</td><td>• Crystal oscillator connections (CI ≦ 50 Ω, CL ≦ 16pF).
Note) When using a crystal other than as indicated above, its compatibility with the crystal oscillator must be thoroughly studied.</td></tr>
<tr><td>PDA1

PDB1</td><td>10

22</td><td>Side-A main charge pump

Side-B main charge pump</td><td>• These are PLL charge pump outputs that output the PLL phase error signals. When the frequency generated by dividing the local oscillator signal frequency by N is higher than the reference frequency, the charge pump outputs a high-level signal for the phase error; when lower, the charge pump outputs a low-level signal for the phase error.
If the two values match, these pins go to high-impedance.
• fosc/N > fref or leading
→ Positive Pulse
• fosc/N < fref or lagging
→ Negative Pulse
• fosc/N = fref and coincidence
→ High-Impedance
(*SB = [1] : PDB1 → High-Impedance)</td></tr>
<tr><td>PDA2

PDB2</td><td>9

23</td><td>Side-A sub charge pump

Side-B sub charge pump</td><td>• PLL charge pump output; outputs PLL phase error signal only when the unlock condition is detected.
• The unlock detection threshold is set by serial data bits UL0 and UL1.
• When a phase error that is shorter than the detection threshold occurs, this signal goes to high impedance and the phase error signal for the main charge pump is output.
• The output pulse of the phase error signal has the same polarity as the main charge pump.</td></tr>
<tr><td>$\overline{\text{LDA}}$

$\overline{\text{LDB}}$</td><td>6

5</td><td>Side-A unlock detector output

Side-B unlock detector output</td><td>• Outputs the PLL lock/unlock status.
Locked: Open
Unlocked: Low
• The unlock detection threshold for lock/unlock discrimination is set by serial data bits UL0 and UL1.
• The output phase error extension is set by serial data bits UE0 and UE1.
• For details, refer to the description of the serial data.
• SB = 1: $\overline{\text{LDB}}$ → Open</td></tr>
<tr><td>AIA
AOA
AIB
OAB</td><td>11
12
21
20</td><td>Side-A low-pass filter transistor

Side-B low-pass filter transistor</td><td>• MOS N-channel transistor for the PLL filter

• The AOA and AOB output withstand voltage is 13V.</td></tr>
<tr><td>$\overline{\text{OUTA}}$

$\overline{\text{OUTB}}$</td><td>13

19</td><td>Side-A general purpose output port
Side-B general purpose output port</td><td>• These latch the serial data bits OA and OB that are sent from the controller, and then invert and output the data.
($\overline{\text{OUTA}}$ can also output XIN divided by two.
• In the LC7152NM, $\overline{\text{OUTA}}$ and $\overline{\text{OUTB}}$ are open at the power-on reset.</td></tr>
</table>

For more information on crystal oscillator : Nihon Dempa Kogyo Co., Ltd.

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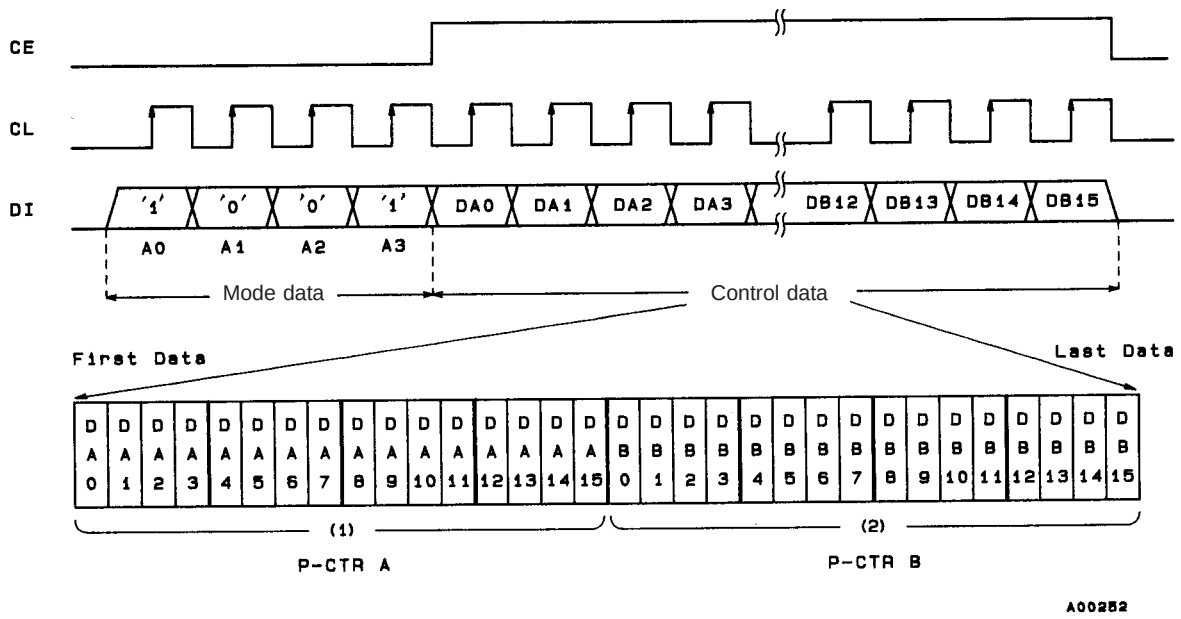
Symbol	Pin No.	Function	Description of function
CE *1	2	Chip enable input	• Set this pin high when inputting serial data to the LC7152.
CL *1	3	Clock input	• Clock for data synchronization when inputting serial data to the LC7152.
DI *1	4	Data input	• Input for serial data being sent from the controller to the LC7152.
V_{DD} V_{SS}	17 15	Power supply Ground	• LC7152 power supply pin.
TEST	8	IC Test input	• LC7152 test pin. (Normally V_{SS} or open.) • However, divide-by-two XIN frequency is output from the pin $\overline{OUTA}$ by applying the V_{DD} level voltage after serial data transfer (T0 = T1 = T2 = 0). Crystal oscillation frequency can be checked normally when the pin is left open.

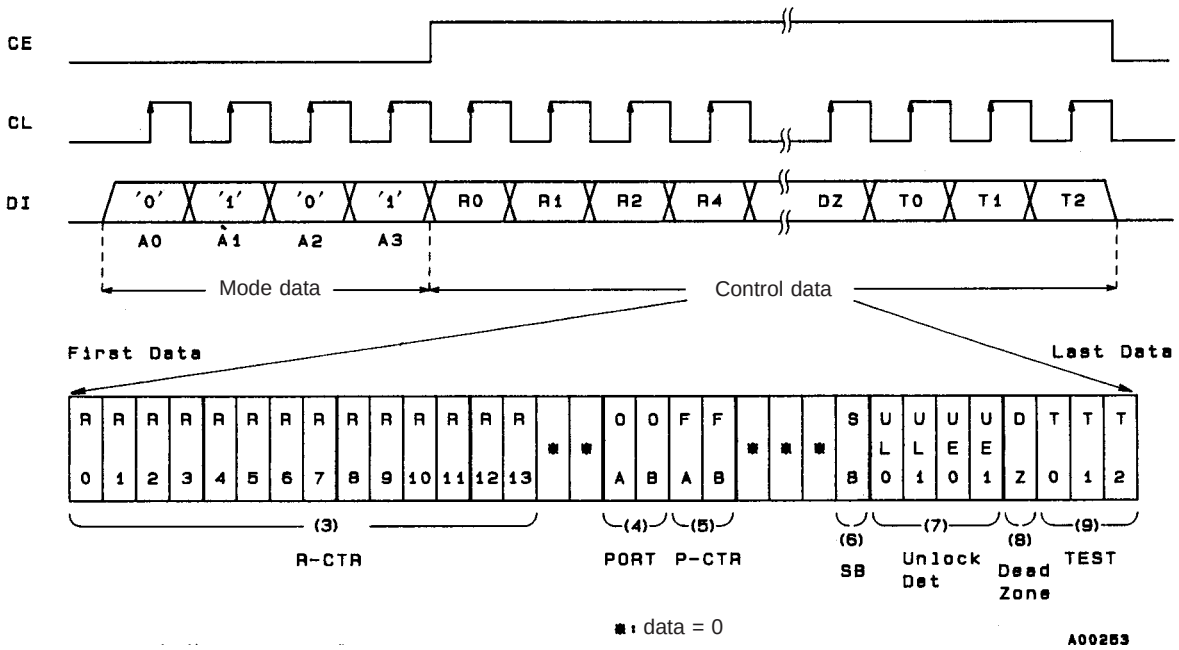
*1 The input "H" voltage and the input "L" voltage on the CE, CL, and DI pins are V_{IH} = 1.5 to 5.5V and V_{IL} = 0 to 0.4V when V_{DD} = 2.0V. When V_{DD} = 3.3V, then V_{IH} = 1.7 to 5.5V and V_{IL} = 0 to 0.6V. (Voltage greater than V_{DD} may be applied to V_{IH}.)

Serial Input Data (PLL Control data) format

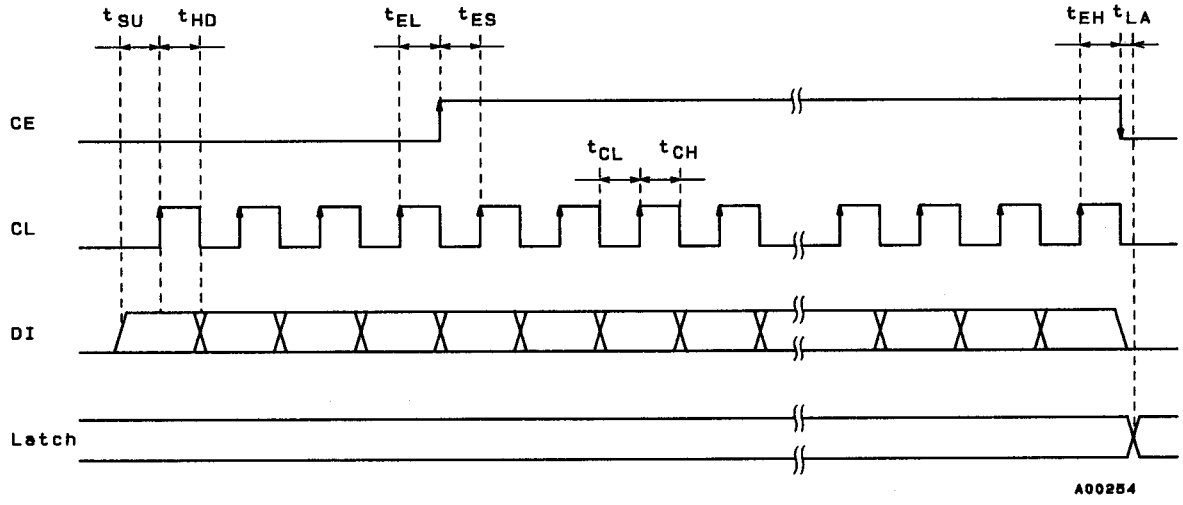
Mode1: Latch-1 data (programmable divider data)



Mode 2: Latch-2 data (reference divider and control data)



Serial Data Transfer Timing



Symbol	Parameter	10.24 MHz crystal	Other crystal frequencies
t_{SU}	Data setup time	At least 0.40 µs	At least $4/f_{X'tal}$
t_{HD}	Data hold time	At least 0.40 µs	At least $4/f_{X'tal}$
t_{EL}	Enable low-level pulse width	At least 0.40µs	At least $4/f_{X'tal}$
t_{ES}	Enable setup time	At least 0.40 µs	At least $4/f_{X'tal}$
t_{EH}	Enable hold time	At least 0.40 µs	At least $4/f_{X'tal}$
t_{CL}	Clock low-level pulse width	At least 0.40 µs	At least $4/f_{X'tal}$
t_{CH}	Clock high-level pulse width	At least 0.40 µs	At least $4/f_{X'tal}$
t_{LA}	Latch propagation delay	Up to 0.40 µs	Up to $4/f_{X'tal}$

Note Perform data transfer after the crystal oscillations normalize. Data transferred before normal oscillations will not be recognized.

Description of Serial Data

<table>
<tr><th>No.</th><th>Controller/Data</th><th>Description</th><th>Related Data</th></tr>
<tr><td>(1)</td><td>Side-A programmable divider data: DA0 to DA15</td><td>• This data sets the side-A programmable divider number. This data is a binary value in which DA0 is the LSB.
The range of divider values that can be set is 272 to 65,535.
NA = fVCO-A/fref</td><td>R0 to R13</td></tr>
<tr><td>(2)</td><td>Side-B programmable divider data: DB0 to DB15</td><td>• This data sets the side-B programmable divider number. This data is a binary value in which DB0 is the LSB.
The range of divider values that can be set is 272 to 65,535.
NB = fVCO-B/fref</td><td>R0 to R13</td></tr>
<tr><td>(3)</td><td>Reference frequency data: R0 to R13</td><td>• This data sets the reference divider number. This data is a binary value in which R0 is the LSB.
The range of divider values that can be set is 8 to 16,383.
(Actual divider number) = (setting) x 2
(reference frequency: fref) = ($f_{X'tal}$: XIN)/(actual divider number)</td><td>UL0 Ul1 UE0 UE1</td></tr>
<tr><td>(4)</td><td>Output port data: OA, OB</td><td>• This data determines the output on the general-purpose output port.
OA → OUTA
OB → OUTB
• Data 0: open; Data 1: low
• During the power-on reset in the LC7152NM, OA and OB are both “0”.</td><td></td></tr>
<tr><td>(5)</td><td>Input frequency range switching data: FA, FB</td><td>• This data switches the input frequency range for the PIA and PIB pins. (FA → PIA, FB → PIB)
<table><tr><th rowspan="2">Data</th><th>Supply voltage (V_{DD})</th></tr><tr><th>2.0 to 3.3 V</th></tr><tr><td>[0]</td><td>1.5 to 23 MHz</td></tr><tr><td>[1]</td><td>20 to 55 MHz</td></tr></table>• In the case of the LC7152KM: Data 1: 55 to 80 MHz (V_{DD} = 2.7 V to 3.3 V)</td><td>DA0 to DA15
DB0 to DB15</td></tr>
<tr><td>(6)</td><td>Standby mode data : SB</td><td>• This data puts the PLL in standby mode.
• SB = 1: standby mode ($\overline{LDB}$ pin: open)
→ Single PLL operation: Side-A operating, side-B stopped
• SB = 0: standby mode off
→ Dual PLL operation: Side-A operating, side-B operating
• During the power-on reset in the LC7152NM, SB is “1”.</td><td></td></tr>
<tr><td>(7)</td><td>Unlock detection data

: UL0, UL1

: UE0, UE1</td><td>• This is the phase error detection threshold data that is used for PLL lock/unlock discrimination. If the threshold shown in the table is exceeded, the unlocked state is detected.
unit : µs
<table><tr><th rowspan="2">UL0</th><th rowspan="2">UL1</th><th rowspan="2">Phase error detector threshold</th><th colspan="5">XIN : fXIN [MHz] example</th></tr><tr><th>4.0</th><th>7.2</th><th>8.0</th><th>10.24</th><th>12.8</th></tr><tr><td>0</td><td>0</td><td>0</td><td>←</td><td>←</td><td>←</td><td>←</td><td>←</td></tr><tr><td>1</td><td>0</td><td>±4/$f_{X'tal}$</td><td>±1.00</td><td>±0.55</td><td>±0.50</td><td>±0.39</td><td>±0.31</td></tr><tr><td>0</td><td>1</td><td>±16/$f_{X'tal}$</td><td>±4.00</td><td>±2.22</td><td>±2.00</td><td>±1.56</td><td>±1.20</td></tr><tr><td>1</td><td>1</td><td>±64/$f_{X'tal}$</td><td>±16.00</td><td>±8.88</td><td>±8.00</td><td>±6.25</td><td>±5.00</td></tr></table>(Note) Note that if the data changes in lock state, the PLL will be unlocked temporarily.
• The detected phase error (øE) signal can be extended by a certain amount of time and output on the $\overline{LDA}$ and $\overline{LDB}$ pins. This data determines the length of this extension. However, when UL0 = UL1 = 0, the phase error is not extended, and is output directly.
unit : ms
<table><tr><th rowspan="2">UE0</th><th rowspan="2">UE1</th><th rowspan="2">Reference frequency fref</th><th colspan="3">Reference frequency : fref [kHz] example</th></tr><tr><th>1 kHz</th><th>5 kHz</th><th>12.5 kHz</th></tr><tr><td>0</td><td>0</td><td>4 × (1/fref)</td><td>4.0*</td><td>0.8</td><td>0.32</td></tr><tr><td>1</td><td>0</td><td>8 × (1/fref)</td><td>8.0</td><td>1.6</td><td>0.64</td></tr><tr><td>0</td><td>1</td><td>32 × (1/fref)</td><td>32.0</td><td>6.4*</td><td>2.56</td></tr><tr><td>1</td><td>1</td><td>64 × (1/fref)</td><td>64.0</td><td>12.8</td><td>5.12*</td></tr></table>(*standard value)</td><td></td></tr>
</table>

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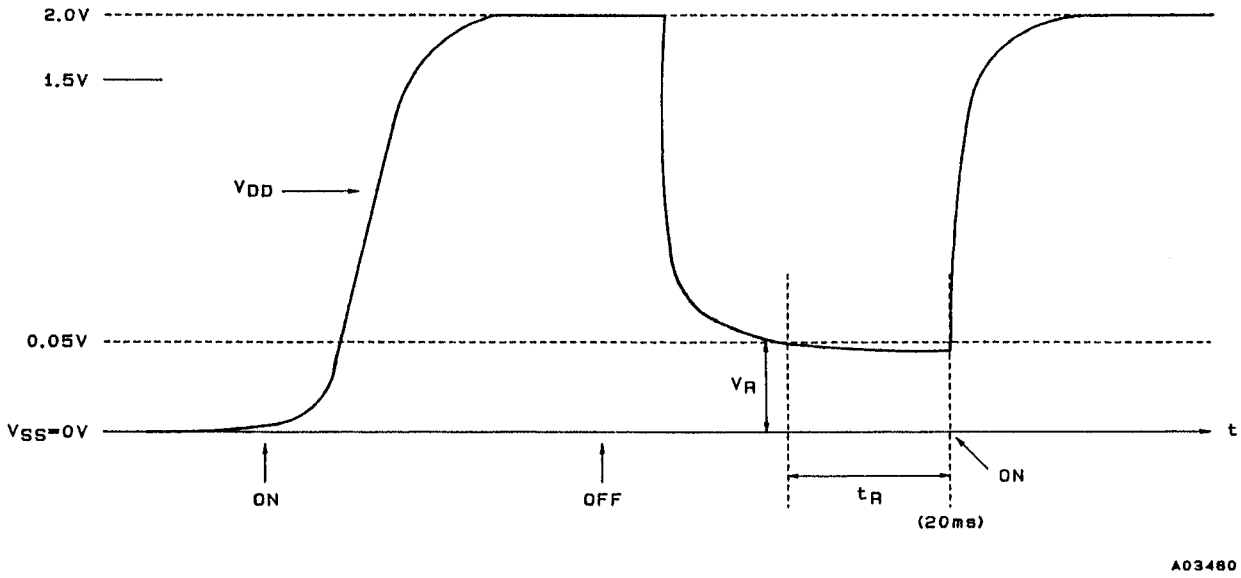
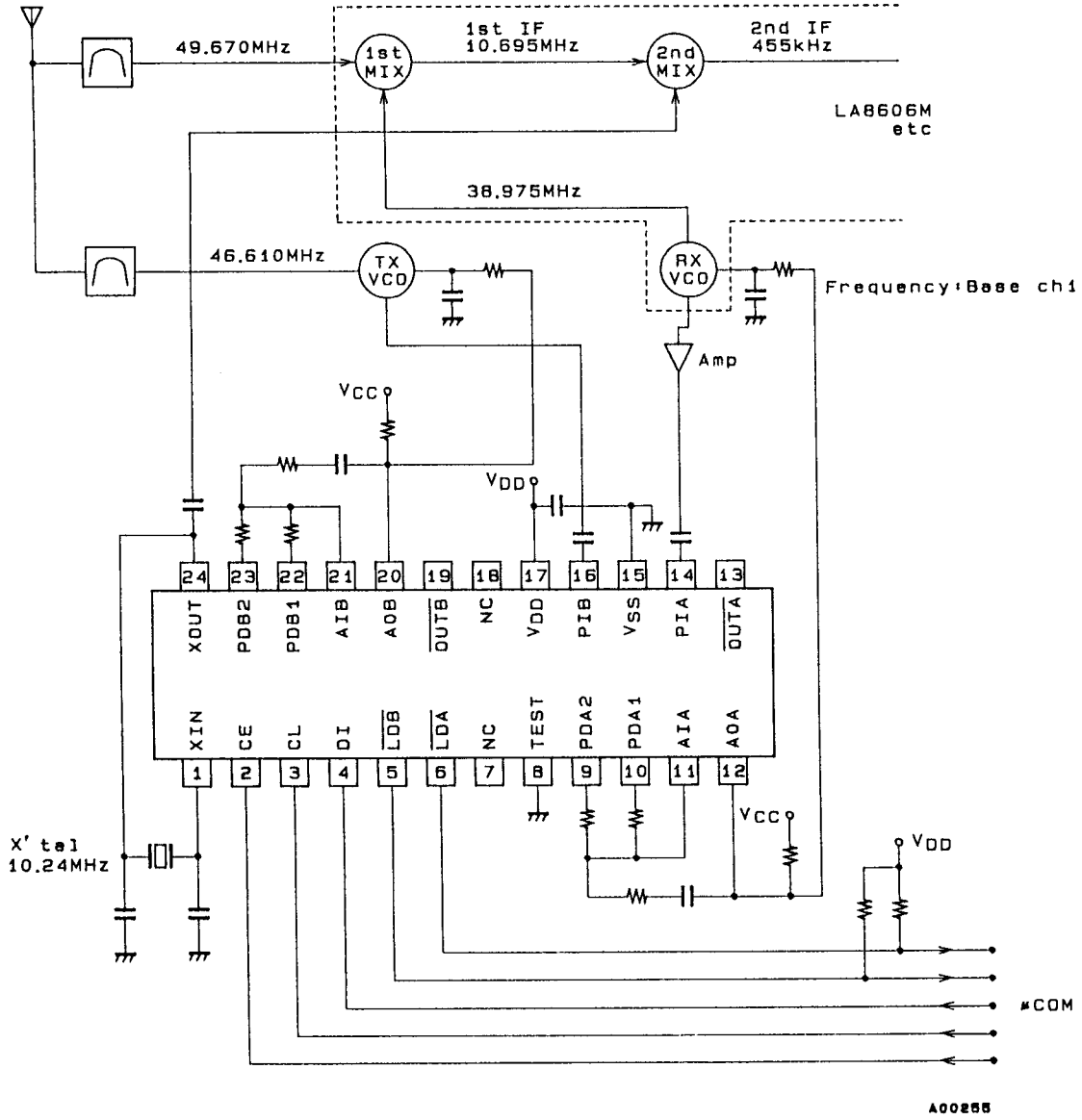
<table>
<tr><th>No.</th><th>Controller/Data</th><th>Description</th><th>Related Data</th></tr>
<tr><td>(8)</td><td>Dead zone control data: DZ</td><td>• This data controls the phase comparator dead zone.
(DZA < DZB)
<table><tr><th>DZ</th><th>Mode</th></tr><tr><td>0</td><td>DZA</td></tr><tr><td>1</td><td>DZB</td></tr></table></td><td></td></tr>
<tr><td>(9)</td><td>IC test data: T0, T1, T2</td><td>• This is the IC test mode switching data. The user does not need to be concerned about this data.
Assume that T0 = T1 = T2 = 0.
Normally, the test pins must be either at V_{SS} or left open.</td><td></td></tr>
</table>

Power-on Reset supply voltage



- Power-on reset is performed when the supply voltage V_{DD} exceeds 2.0 V by power application after the V_{DD} has once fallen under 0.05 V and kept the level for at least 20ms.
- Latch data is retained when the V_{DD} is 1.5 V, where power-on reset is not performed.

Sample Application Circuit (FCC: 10 ch 46/49 MHz cordless telephone)



Example: FCC 1-channel 46/49 MHz cordless telephone base station (See diagram in the preceding page.)
for fref: 5 kHz, RX VCO: 38.975 MHz, TX VCO: 46.610 MHz

Programmable Divider Data

(1) $NA = \frac{fVCO-A}{fref} = \frac{RX\ VCO}{fref} = \frac{38.975MHz}{5kHz} = 7795\ (DA0\ to\ DA15)$
$(1E73)Hex$

(2) $NB = \frac{fVCO-B}{fref} = \frac{TX\ VCO}{fref} = \frac{46.610MHz}{5kHz} = 9322\ (DB0\ to\ DB15)$
$(246A)Hex$

(3) Reference frequency data

$$NR = \left(\frac{fX'tal}{fref} \right) \div 2 = \frac{10.24MHz}{5kHz} \div 2 = 1024\ (R0\ to\ R13)$$
$(400)Hex$

(4) Output port data
General-purpose output port: Open (OA = 0, OB = 0)

(5) Input frequency range select bits
FA = FB = 1

(6) Standby mode
During standby (SB = 1)

(7) Unlock detector output
Extends the phase error signal by 6.4ms if a phase error of ±6.25 µs or more is generated.
: UL0 = UL1 = 1
: UE0 = 0, UE1 = 1

(8) Dead-zone control data
DZA mode : DZ = 0

(9) LSI test data: T0 = T1= T2 = 0

(1) Mode 1: Latch-1 data

DA0	DA1	DA2	DA3	DA4	DA5	DA6	DA7	DA8	DA9	DA10	DA11	DA12	DA13	DA14	DA15	DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	DB8	DB9	DB10	DB11	DB12	DB13	DB14	DB15
1	1	0	0	1	1	1	0	0	1	1	1	1	0	0	0	0	1	0	1	0	1	1	0	0	0	1	0	0	1	0	0

A00256

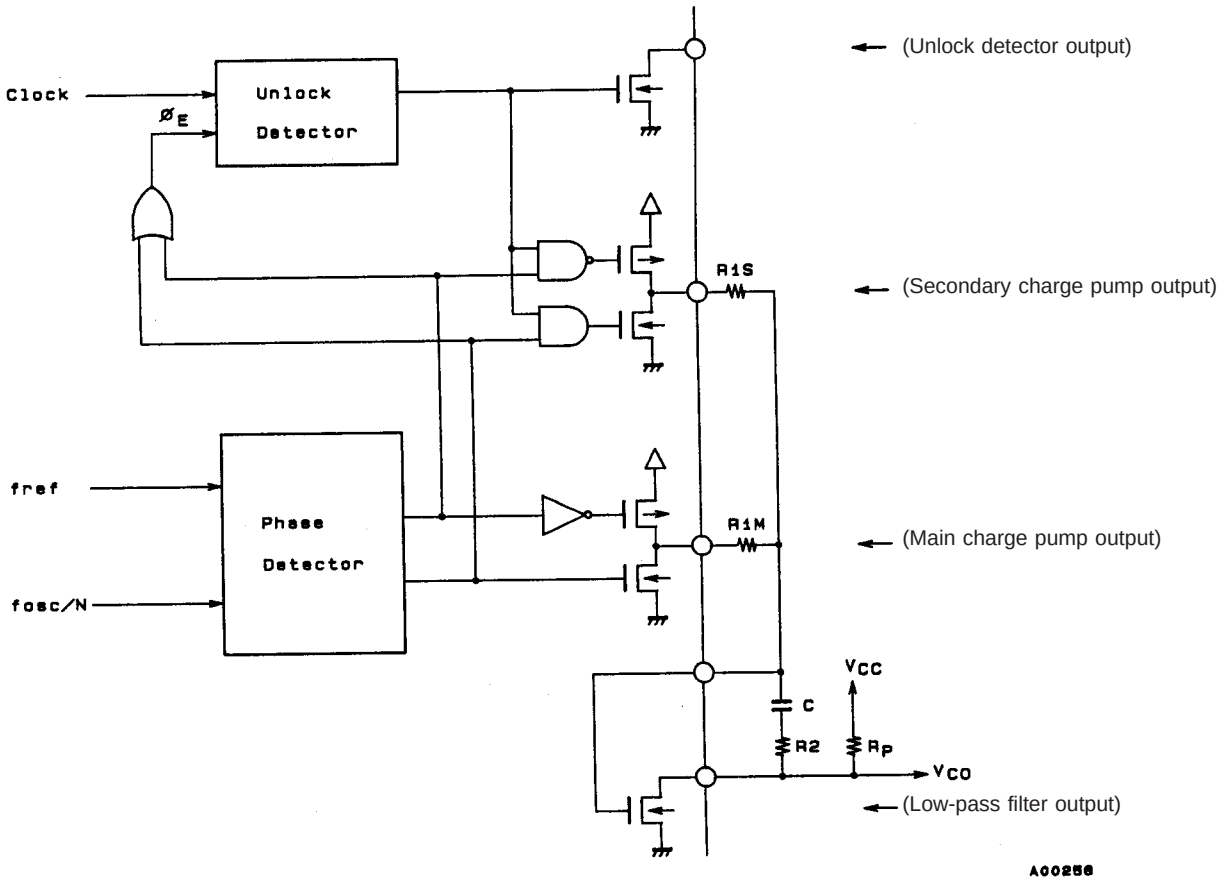
(2) Mode 2: Latch-2 data

RA0	RA1	RA2	RA3	RA4	RA5	RA6	RA7	RA8	RA9	RA10	RA11	RA12	RA13	*	*	DA	DB	FA	FB	*	*	*	SB	UL0	UL1	UE0	UE1	DZ	T0	T1	T2
0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	1	0	0	0	0/1	1	1	0	1	0	0	0	0

* : data = 0

A00257

Dual Charge Pump Descriptions



If an unlock state is detected at channel switch, the sub-charge pump operates, R1M/R1S becomes R1, low-pass filter's time constant is reduced, and the lockup accelerates.
When the circuit is locked, side-band characteristics and modulation characteristics are improved by making the sub-charge pump off, i.e., floating, R1M to be R1, and increasing low-pass filter's time constant.

Device Comparison

Device	Operating frequency			Power-on reset circuit	Package
	FA/FB = 0	FA/FB = 1			
	1.5 to 23 MHz	20 to 55 MHz	55 to 80 MHz		
LC7152	Yes	Yes	No	No	DIP24S
LC7152M	Yes	Yes	No	No	MFP24S
LC7152NM	Yes	Yes	No	Yes	MFP24S
LC7152KM	Yes	Yes	Yes (V_{DD} = 2.7 to 3.3 V)	No	MFP24S