Ordering number : ENN*7202

CMOS IC

LC89057W-VF4-E

Digital Audio Interface Transceiver

Preliminary

Overview

The LC89057W-VF4-E is an IC that demodulates and modulates signals during data transfer between digital audio devices via the IEC60958/61937 and EIAJ CP-1201. Sampling input of data up to 192 KHz can be received. It features a built-in VCO and oscillation amplifier, two bit clock circuits that enable independent setting of the divide ratios that can be used for the DSP data input/output clocks, and LR clock output pins. A multi-channel PCM interface using multiple LC89057W-VF4-E is also possible through a master/slave function. Target applications include high-performance AV amplifiers and DVD audio equipment that use a multi-channel PCM interface.

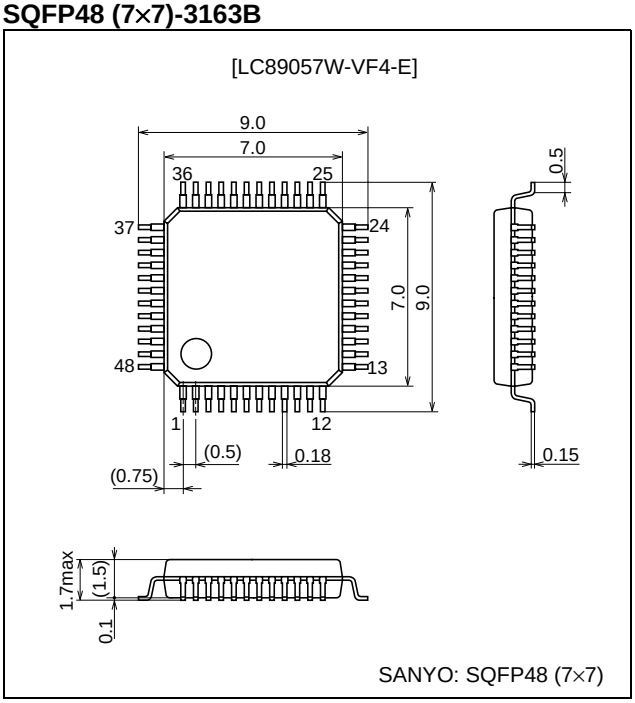
1 Features

- Realization of the full demodulation function as the target of high performance AV equipment.
  - Input sampling frequency of 32kHz to 192kHz and maximum 24 bit data can be received.
  - I^2S data output also supported for easy interface with DSP.
  - Outputs 512fs, 256fs, 128fs, 64fs, 32fs, 2fs, fs, and fs/2 clocks.
  - Oscillation amplifier and external input clocks can be output regardless of the PLL status.
  - Output clock continuity is maintained during clock switching.
  - Multi-channel transfer and reception are supported through use of master/slave function.
  - Demodulation functions can be processed using common low jitter clock when PLL not used.
  - Built-in PLL error lock prevention circuit for accurate locking.

2 Package Dimensions

unit: mm

SQFP48 (7×7)-3163B



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• Outputs various information for easy system configuration.
  – Outputs DTS-CD/LD detection flag for DTS sync signal detection.
  – Outputs burst preamble Pc from microcontroller interface.
  – Calculates sampling frequency of input signal and outputs it from microcontroller interface.
  – Outputs interrupt signal for microcontroller (interrupt source can be selected).
  – Outputs transition period signal at VCO clock and oscillation amplifier clock switch.
  – Outputs of channel status bit 1 (non-PCM data detection bit).
  – Outputs channel status emphasis information.
  – Outputs first 48 channel status bits update flag.
  – Validity flag and user data output can also be selected.
  – Various settings and outputs can also possible through microcontroller interface.

• Large number of built-in functions to reduce number of peripheral circuit.
  – Built-in modulation function that can attach channel status, validity flag, and user data.
  – Total of 7 digital data input pins: 1 input pin with amplifier and 6 input pins with 5V input level tolerable can be acceptable TTL level signal.
  – Bi-phase input data detection function that enables monitoring with input pin status microcontroller.
  – Input data can be selected via PLL lock error.
  – Input data can be selected independently from the selection of demodulation data from the 8 types of input data.
  – 2 types of bit clock and LR clock outputs are provided. Various divide ratios can be set for one of these types.
  – A serial digital audio data input pin is provided. It can be switched to demodulation output.
  – Data input to the serial digital audio data input pin can be modulated.
  – Built-in oscillation amplifier and frequency divider for crystal resonator can also be used as clock generator.
  – Built-in 4 bit general-purpose parallel I/O port can also be used for interface with peripheral IC.
  – Single 3.3V power supply operation. TTL input port supports 5V interface.
  – Small SQFP48 package for efficient substrate mounting surface use.

3 Pin Assignment

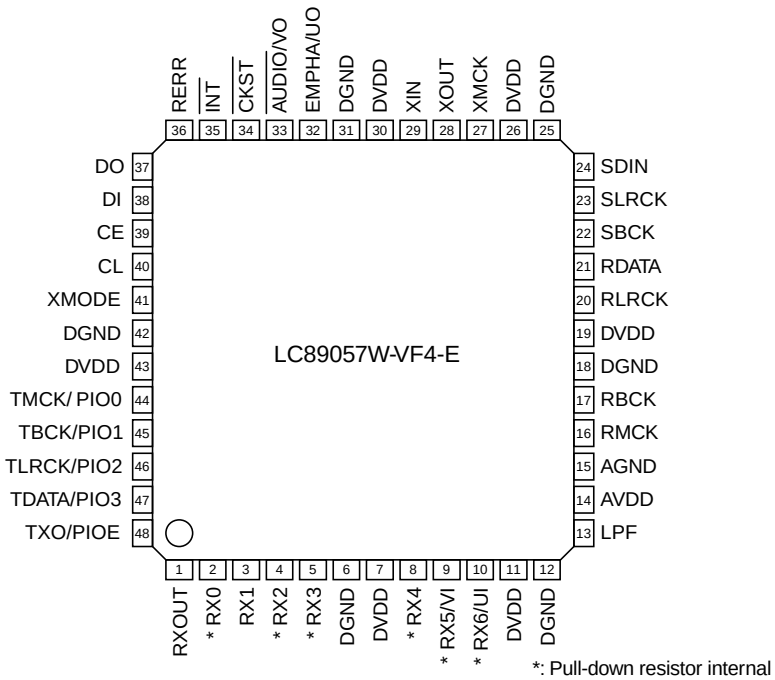


Figure 3.1. LC89057W-VF4-E Pin Assignment

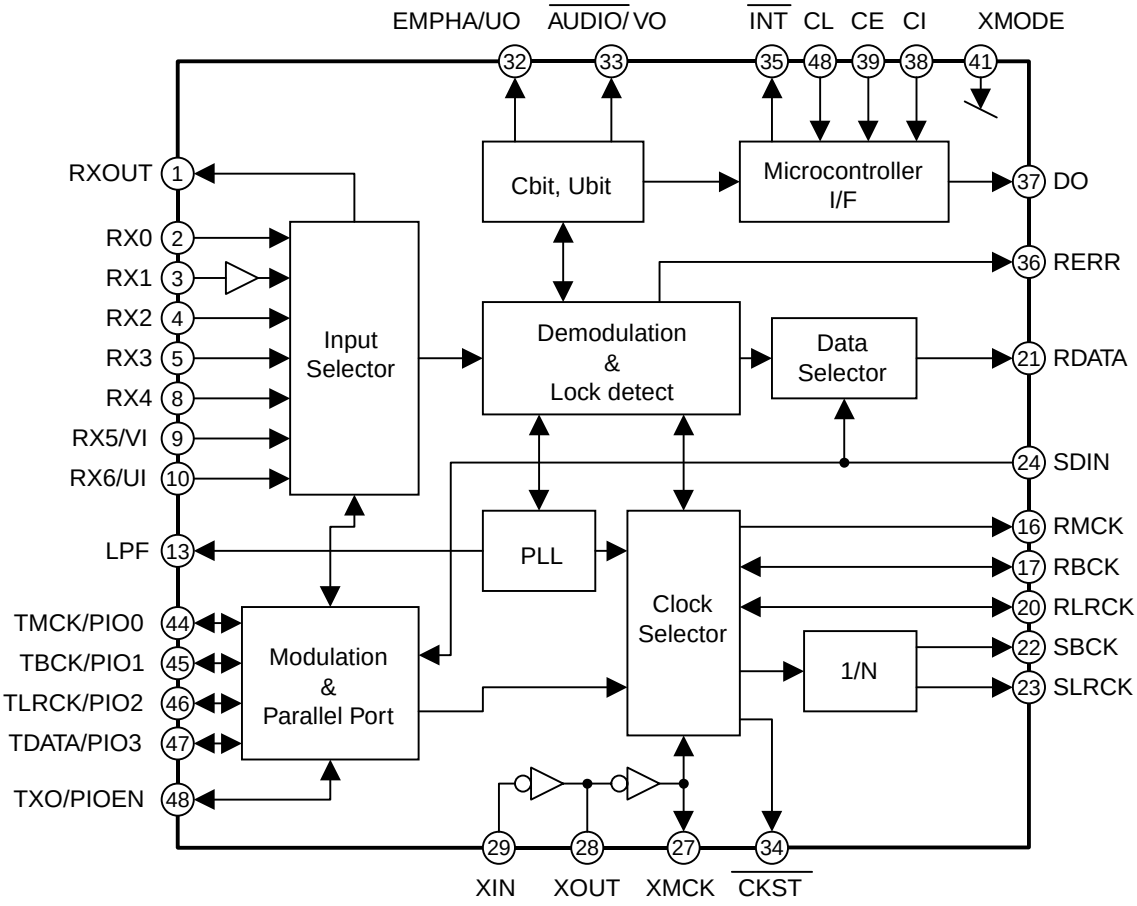
4 Pin Functions

Table 4.1. Pin Functions

Pin No.	Pin	I/O	Function
1	RXOUT	O	Input bi-phase selection data output pin
2	RX0	I_5	TTL-compatible digital data input pin
3	RX1	I	Coaxial-compatible digital data input pin with built-in amplifier
4	RX2	I_5	TTL-compatible digital data input pin
5	RX3	I_5	TTL-compatible digital data input pin
6	DGND		Digital GND
7	DVDD		Digital power supply
8	RX4	I_5	TTL-compatible digital data input pin
9	RX5/VI	I_5	TTL-compatible digital data || Validity flag input pin for modulation
10	RX6/UI	I_5	TTL-compatible digital data || User data input pin for modulation
11	DVDD		PLL digital power supply
12	DGND		PLL digital GND
13	LPF	O	PLL loop filter connection pin
14	ACDD		PLL analog power supply
15	AGND		PLL analog GND
16	RMCK	O	R system clock output pin (256fs, 512fs, XIN, VCO)
17	RBCK	O/I	R bit clock input/output pin (64fs)
18	DGND		Digital GND
19	DVDD		Digital power supply
20	RLRCK	O/I	R LR clock input/output pin (fs)
21	RDATA	O	Serial audio data input pin
22	SBCK	O	S bit clock output pin (32fs, 64fs, 128fs)
23	SLRCK	O	S LR clock output pin (fs/2, fs, 2fs)
24	SDIN	I_5	Serial audio data input pin
25	DGND		Digital GND
26	DVDD		Digital power supply
27	XMCK	O	Oscillation amplifier output pin
28	XOUT	O	Crystal resonator connection output pin
29	XIN	I	Crystal resonator connection, external supply clock input pin (24.576 MHz or 12.288 MHz)
30	DVDD		Digital power supply
31	DGND		Digital GND
32	EMPHA/UO	I/O	Emphasis information || U data output || Chip address setting pin
33	$\overline{\text{AUDIO}}$/VO	I/O	Non-PCM output || V flag output || Chip address setting pin
34	$\overline{\text{CKST}}$	I/O	Clock switch transition period signal || Demodulation master or slave function switch pin
35	$\overline{\text{INT}}$	I/O	Microcontroller interrupt output || Modulation or general-purpose I/O switch pin
36	RERR	O	PLL clock error, data error flag output
37	DO	O	Microcontroller I/F read data output pin (3-state)
38	DI	I_5	Microcontroller I/F write data input pin
39	CE	I_5	Microcontroller I/F chip enable input pin
40	CL	I_5	Microcontroller I/F clock input pin
41	XMODE	I_5	System reset input pin
42	DGND		Digital GND
43	DVDD		Digital power supply
44	TMCK/PIO0	I/O	Modulation 256fs system clock input || General-purpose I/O input/output pin
45	TMCK/PIO1	I/O	Modulation 64fs bit clock input || General-purpose I/O input/output pin
46	TLRCK/PIO2	I/O	Modulation fs clock input || General-purpose I/O input/output pin
47	TLRCK/PIO3	I/O	Modulation serial audio data input || General-purpose I/O input/output pin
48	TXO/PIOEN	O/I	Modulation data output || General-purpose I/O enable input pin

1) Input/output I or O = –0.3 to 3.6V, I_5 = –0.3 to 5.5V
2) Pins 32 and 33 are latch address setting input pins when pin 41 = "L".
3) Pin 34 is a demodulation function master or slave setting input pin when pin 41 = "L".
4) Pin 35 is a modulation function or general-purpose I/O function switch setting input pin when pin 41 = "L".
5) Perform ON/OFF for all power supplies with the same timing as a latch-up countermeasure.

5 Block Diagram



6 Electrical Characteristics

6.1 Absolute Maximum Ratings

Table 6.1. Absolute Maximum Ratings at T_a = 25°C, AGND = DGND = 0V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$AVDD_{max}$	6-1-1	–0.3 to 4.6	V
Maximum supply voltage	$DVDD_{max}$	6-1-2	–0.3 to 4.6	V
Input voltage 1	V_{i1}	6-1-3	–0.3 to DVDD +0.3	V
Input voltage 2	V_{i2}	6-1-4	–0.3 to 5.8	V
Output voltage	V_o	6-1-5	–0.3 to DVDD +0.3	V
Storage ambient temperature	T_{stg}		–55 to 125	°C
Operating ambient temperature	T_{opg}		–30 to 70	°C
Maximum input/output current	$T_{i,}$ T_o	6-1-6	±20	mA

∗ 6-1-1: AVDD pin

∗ 6-1-2: DVDD pin

∗ 6-1-3: RX1, RBCK, RLRCK, XIN pins
TMCK/PIO0, TBCK/PIO1, TLRCK/PIO2 pins
TDATA/PIO3, TXO/PIOEN pins

∗ 6-1-4: RX0, RX2, RX3, RX4, RX5/VI, RX6/UI pins
SDIN, DI, CE, CL, XMODE pins

∗ 6-1-5: RXOUT, RMCK, RBCK, RLRCK, SBCK, SLRCK pins
RDATA, XMCK, XOUT, EMPHA/UO, $\overline{\text{AUDIO}}$/VO pins
$\overline{\text{CKST}}$, $\overline{\text{INT}}$, RERR, DO, pins
TMCK/PIO0, TBCK/PIO1, TLRCK/PIO2 pins
TDATA/PIO3, TXO/PIOEN pins

∗ 6-1-6: Per input/output pin

6.2 Recommended Operating Conditions

Table 6.2. Recommended Operating Conditions

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	AVDD, DVDD		3.0	3.3	3.6	V
Input voltage range 1	V_{IN1}	6-2-1	0	3.3	3.6	V
Input voltage range 2	V_{IN2}	6-2-2	0	3.3	5.5	V
Operating temperature	V_{opg}		–30	–	70	°C

∗ 6-2-1: RX1, RBCK, RLRCK, XIN pins
TMCK/PIO0, TBCK/PIO1, TLRCK/PIO2 pins
TDATA/PIO3, TXO/PIOEN pins

∗ 6-2-2: RX0, RX2, RX3, RX4, RX5/VI, RX6/UI pins
SDIN, DI, CE, CL, XMODE pins

6.3 DC Characteristics

Table 6.3. DC Characteristics at T_a = 25°C, AVDD = DVDD = 3.3V, AGND = DGND = 0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input, High	V_{IH}	6-3-1	0.7VDD	–	–	V
Input, Low	V_{IL}		–	–	0.2VDD	V
Input, High	V_{IH}	6-3-2	2.0	–	5.8	V
Input, Low	V_{IL}		–0.3	–	0.8	V
Output, High	V_{OH}	6-3-3	VDD–0.8	–	–	V
Output, Low	V_{OL}		–	–	0.4	V
Output, High	V_{OH}	6-3-4	VDD–0.8	–	–	V
Output, Low	V_{OL}		–	–	0.4	V
Output, High	V_{OH}	6-3-5	VDD–0.8	–	–	V
Output, Low	V_{OL}		–	–	0.4	V
Output, High	V_{OH}	6-3-6	VDD–0.8	–	–	V
Output, Low	V_{OL}		–	–	0.4	V
Input amplitude	V_{PP}	6-3-7	200	–	–	mV
Consumption current	V_{DD1}	6-3-8	–	1.7	3.4	mA
Consumption current	V_{DD1}	6-3-9	–	17	34	mA
Consumption current	V_{DD1}	6-3-10	–	19	38	mA

∗ 6-3-1: CMOS levels: RX1, RBCK, RLRCK, XIN pins

∗ 6-3-2: TTL levels: Pins other than those listed above

∗ 6-3-3: I_{OH} = −12mA, I_{OL} = 8mA: RMCK pin

∗ 6-3-4: I_{OH} = −8mA, I_{OL} = 8mA: XMCK, XOUT pins

∗ 6-3-5: I_{OH} = −4mA, I_{OL} = 4mA: RXOUT, RBCK, RLRCK, RDATA, SBCK pins
SLRCK, TMCK/PIO0, TBCK/PIO1, TLRCK/PIO2 pins
TDATA/PIO3, TXO/PIOEN pins

∗ 6-3-6: I_{OH} = −2mA, I_{OL} = 2mA: Pins other than those listed above

∗ 6-3-7: Before capacitance of RX1 input pin

∗ 6-3-8: Demodulation function and oscillation amplifier stopped, modulation only, output sampling frequency = 96kHz

∗ 6-3-9: XIN continuous 24.576MHz oscillation, demodulation only, input sampling frequency = 96kHz

∗ 6-3-10: XIN continuous 24.576MHz oscillation, modulation, input/output sampling frequency = 96kHz

6.4 AC Characteristics

Table 6.4. AC Characteristics at T_a = 25°C, AVDD = DVDD = 3.3V, AGND = DGND = 0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
RX0 TO RX6 sampling frequency	f_{RFS}		28	–	195	kHz
XIN clock frequency	f_{XF1}	6-4-1	8	12.288	19	MHz
XIN clock frequency	f_{XF2}	6-4-2	20	24.576	30	MHz
RMCK clock frequency	f_{RCK}		4	–	100	MHz
RMCK clock jitter	t_j		–	200	–	ps
RMCK, RBCK delay	t_{MBO}		–	–	10	ns
RBCK, RDATA delay	t_{BDO}		–	–	10	ns
RMCK, SBC delay	t_{MBO}	6-4-3	–	–	10	ns
SMCK, RDATA delay	t_{BDO}	6-4-4	–	–	10	ns
TMCK input pulse width	t_{WMI}		10	–	–	ns
TBCK input pulse width	t_{WBI}		40	–	–	ns
TLRCK sampling frequency	t_{TFS}		28	–	195	kHz
TBCK, TDATA setup	t_{DSI}		–	20	–	ns
TBCK, TDATA hold	t_{DHI}		–	20	–	ns
TMCK, TBCK delay	t_{MBI}		–	–	10	ns
TBCK, TDATA delay	t_{BDI}		–	–	10	ns

∗ 6-4-1: XINSEL = "0" setting, 12.288MHz must be set when calculating input sampling frequency

∗ 6-4-2: XINSEL = "1" setting, 24.576MHz must be set when calculating input sampling frequency

∗ 6-4-3: When RMCK and SBCK source clocks are the same

∗ 6-4-4: When SBCK is the PLL source clock

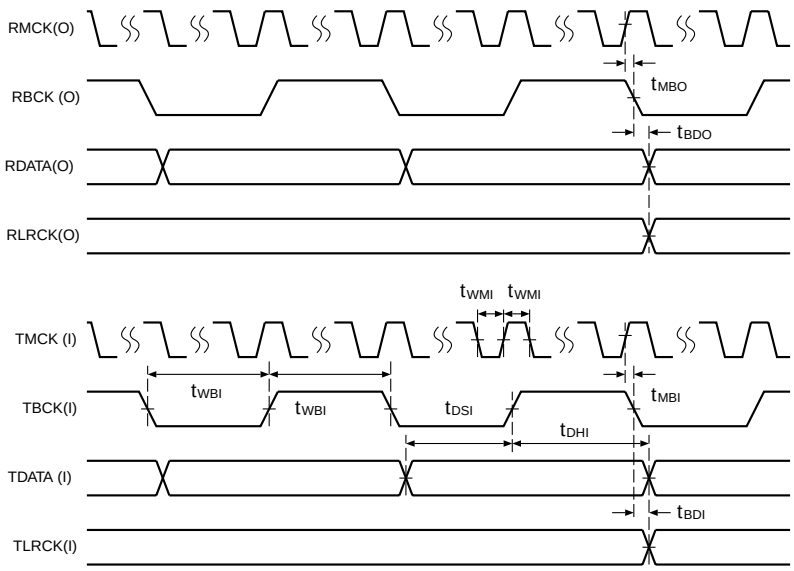


Figure 6.1. AC Characteristics

6.5 Microcontroller Interface AC Characteristics

Table 6.5. I/F AC Characteristics at T_a = 25°C, AVDD = DVDD = 3.3V, AGND = DGND = 0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
XMODE pulse width, Low	$t_{RST\ dw}$		200	–	–	µs
$\overline{INT}$ pulse width, Low	$t_{INT\ wd}$	6-5-1	5	1/fs	36	µs
CL pulse width, Low	$t_{CL\ dw}$		100	–	–	ns
CL pulse width, High	$t_{CL\ uw}$		100	–	–	ns
CL, CE setup time	$t_{CL\ setup}$		50	–	–	ns
CL, CE hold time	$t_{CE\ hold}$		50	–	–	ns
CL, DI setup time	$t_{DI\ setup}$		50	–	–	ns
CL, DE hold time	$t_{DI\ hold}$		50	–	–	ns
CL, CE hold time	$t_{CL\ hold}$		50	–	–	ns
CL, DO delay time	$t_{CL\ to\ DO}$		–	–	20	ns
CE, DO delay time	$t_{CE\ to\ DO}$		–	–	20	ns

* 6-5-1: When INTOPF is set to "1", fs = input sampling frequency

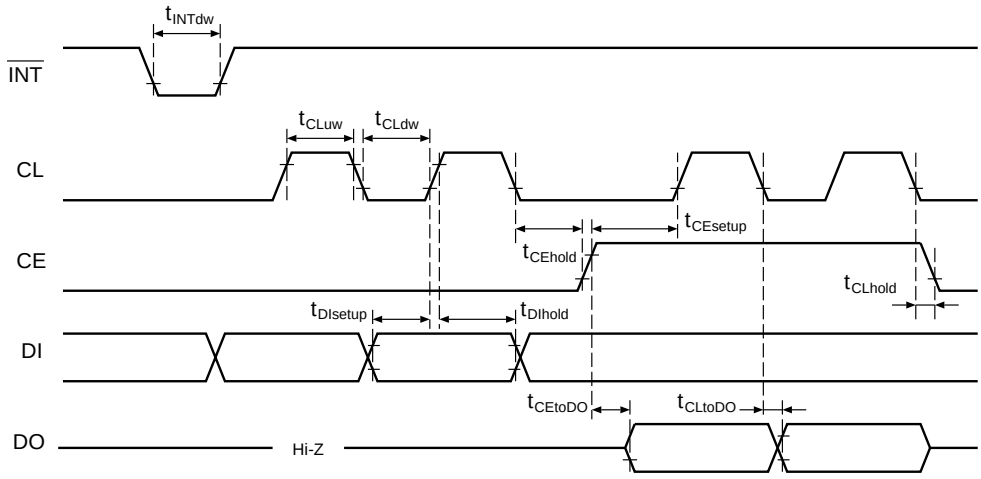


Figure 6.2. Microcontroller Interface AC Characteristics

7 Initial System Settings

7.1 System Reset (XMODE)

- The system operates normally when XMODE is set to "H" after applying a supply voltage of 3.0V or higher. Following power ON, the system is reset by setting XMODE to "L" again.
- Connect a 10kΩ pull-down or pull-up resistor to EMPHA/UO, $\overline{\text{AUDIO}}$/VO, $\overline{\text{CKST}}$, and $\overline{\text{INT}}$ for the chip address, demodulation function master or slave, and modulation function or general-purpose I/O function settings
- If EMPHA/UO, $\overline{\text{AUDIO}}$/VO, $\overline{\text{CKST}}$, and $\overline{\text{INT}}$ are not pulled up or down, their state at setting input is undefined and they cannot be set properly. Always connect a pull-up or pull-down resistor to these pins.

Table 7.1. Pin Names and Settings

Setting	Pins
Chip address	EMPHA/UO, $\overline{\text{AUDIO}}$/VO
Demodulation function master or slave	$\overline{\text{CKST}}$
Modulation function or general-purpose I/O function	$\overline{\text{INT}}$

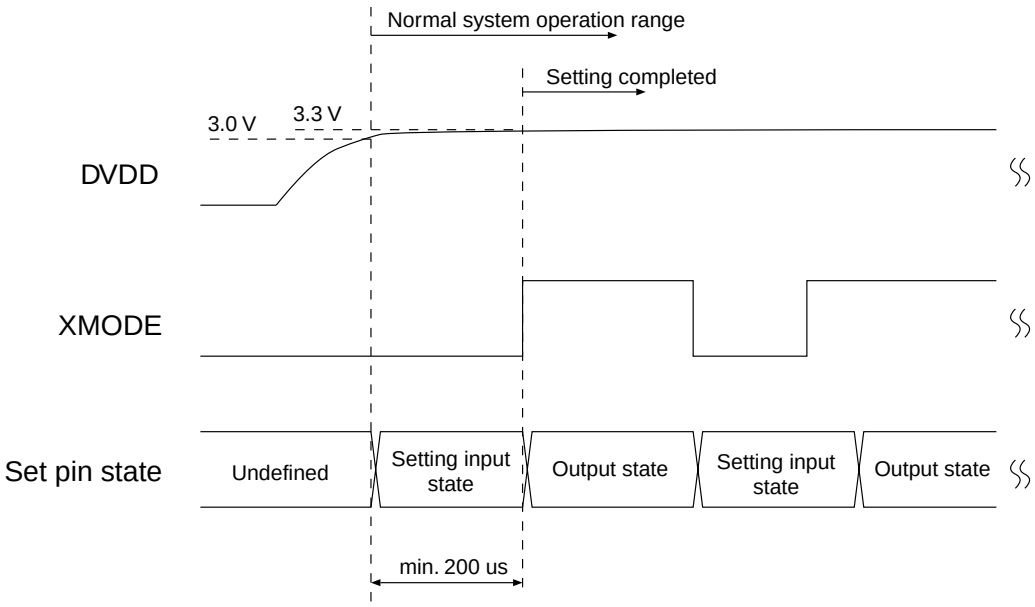


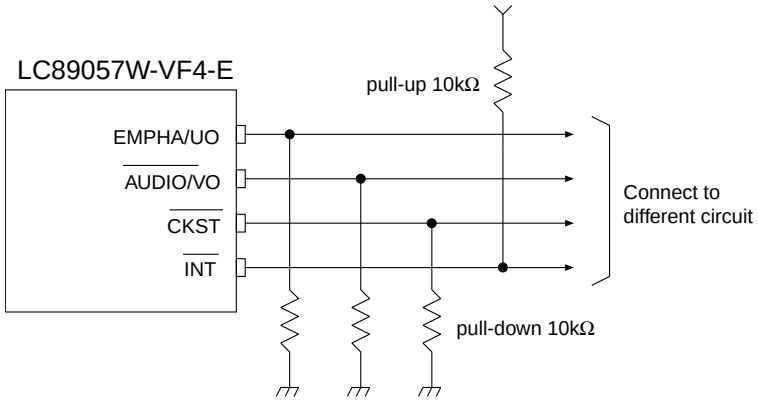
Figure 7.1. Setting Timing Chart of Function Setting Input Pins

7.2 Chip Address Settings (EMPHA/UO, $\overline{\text{AUDIO}}$/VO)

- The LC89057W-VF4-E comes with a function to set a unique chip address to allow the use of several LC89057W-VF4-E on the same microcontroller bus.
- Connect a 10kΩ pull-down or pull-up resistor to EMPHA/UO and $\overline{\text{AUDIO}}$/VO as the chip address settings. This allows up to set 4 chip addresses.
- Chip addresses in the microcontroller interface are set with CAL and CAU provided as the first two bits on the LSB side. CAL corresponds to the lower and CAU to the higher chip address.
- Command writing is enabled by making the chip address settings using EMPHA/UO and $\overline{\text{AUDIO}}$/VO the same as the chip addresses sent from the microcontroller.
- The chip address setting must be performed even when using only one LC89057W-VF4-E in the system. If the chip address setting is not performed, the chip address is undefined and control from the microcontroller cannot be performed. When the microcontroller is not used, the state of the chip address setting pin is input open while XMODE is "L". Be sure to connect either a pull-down resistor or a pull-up resistor to EMPHA/UO and $\overline{\text{AUDIO}}$/VO.

Table 7.2. Chipset Address Settings

$\overline{\text{AUDIO}}$/VO	EMPHA/UO	CAU	CAL
Pull-down	Pull-down	0	0
Pull-down	Pull-up	0	1
Pull-up	Pull-down	1	0
Pull-up	Pull-up	1	1



Setting Contents of Above Figure

Chip address setting	=>	CAL = CAU = 0
Demodulation function master or slave setting	=>	Master
Modulation function or general-purpose I/O port switch	=>	General-purpose I/O port function

Figure 7.2. Function Setting Input Pin Setting Example

7.3. Demodulation Function Master/Slave Settings ($\overline{CKST}$)

- A master/slave function that allows multi-channel synchronized transfer using multiple LC89057W-VF4-E LSIs is built in. This setting connects either a 10kΩ pull-down or a pull-up resistor to $\overline{CKST}$.
- Set the master mode when using only one LC89057W-VF4-E LSI. When using multiple LC89057W-VF4-E LSIs, set one to the master mode and the others to the slave mode.
- To perform multi-channel transfer using multiple LC89057W-VF4-E LSIs, connect RBCK and RLRCK (output) on the master side to RBCK and RLRCK (input) on the slave side. Also connect XMCK on the master side to XIN on the slave side. At this time, set the same polarity for RBCK and RLRCK and the same frequency for XIN and XMCK.
- If the input data sampling frequency or the phase between the master and slave differ or if the clock sources differ even though the sampling frequencies are the same, some of the output data may get dropped or read twice on the slave side. Whether this phenomenon is occurring can be checked with $\overline{INT}$ and the microcontroller interface.

Table 7.3. Master/Slave Switching

$\overline{CKST}$	Mode
Pull-down	Master mode
Pull-up	Slave mode

Table 7.4. Clock Pin State

Pin	Master mode	Slave mode
RMCK	Output	Low
RBCK	Output	Input
RLRCK	Output	Input

7.4 Modulation Function and General-Purpose I/O Port Switching ($\overline{INT}$)

- The modulation function and the general-purpose I/O function share the same pin and therefore cannot be used simultaneously.
- To switch functions, connect either a 10kΩ pull-down or pull-up resistor to $\overline{INT}$.

Table 7.5. Modulation Function and General-Purpose I/O Switching

$\overline{INT}$ State	Function
pull-down	Modulation f unction
Pull-up	General-purpose I/O

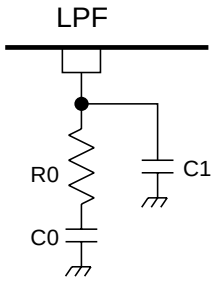
8 Description of Demodulation Function

- The demodulation function operation settings are performed with RXOPR. The operating status is set as the initial value.

8.1 Clocks

8.1.1 PLL (LPF)

- A VCO (Voltage Controlled Oscillator) that can be stopped with PLLOPR is provided on chip and synchronization to frequencies from 32kHz to 192kHz and transfer rate of 4MHz to 25MHz can be selected.
- The PLL clock frequency is selected with PLLSEL. For systems with an input data sampling frequency of 105kHz or lower, the initial setting of 512fs is recommended. Since the system clock RMCK output initial value is set to 1/2 of PLLSEL, the RMCK output is 256fs when a PLL clock frequency of 512fs is used.
- For receptions systems with an input data sampling frequency higher than 105kHz, switch the PLL clock frequency to 256fs. Since, if the same initial output setting as above is used, RMCK is 128fs, set PRESEL0,1 as needed.
- LPF is a PLL loop filter pin. Connect the following resistance and capacitances by selecting the PLLSEL system clock. Since PLLSEL switching involves a change in LPF loop filter constant, perform the PLLSEL setting prior to bi-phase data input.



Clock	R0	C0	C1
512fs	220Ω	0.1μF	0.022μF
256fs	330Ω	0.068μF	0.001μF

Figure 8.1. Loop Filter Configuration

8.1.2 Demodulation Function without Using PLL (TMCK)

- The LC89057W-VF4-E has a function to process input bi-phase data using an external clock (external synchronization function). In normal demodulation processing, the clock is generated in synchronization with data by the built-in PLL and data processing is performed using this clock. In contrast, in the LC89057W-VF4-E, data processing is also possible to perform data processing by supplying a data synchronized clock instead of the clock generated by the PLL via an independent transmission path.
- To use the external synchronization function, set the demodulation function without using PLL with EXSYNC, and after setting the 256fs clock with PLLSEL, and PLLSEL setting frequency 1/1 with PRSEL0,1, input the 256fs clock synchronized with the input data to TMCK. As a result of these settings, the same operation as PLL demodulation processing when the 256fs clock is set is performed. Also, do not connect anything to LPF. No loop filter is required either.
- Complete the above external synchronization function settings prior to bi-phase data input. Also pay attention to the bandwidth of clock transmission path.
- A high-precision clock system using an external PLL can also be configured by using the external synchronization function.

8.1.3 Oscillation amplifiers (XIN, XOUT, MCK)

- The LC89057W-VF4-E features a built-in oscillation amplifier. An oscillation circuit can be configured by connecting a crystal resonator, feedback resistor, and load capacitance to XIN and XOUT. When connecting a crystal resonator, use a fundamental crystal resonator. Also, note that the load capacitance depends on the crystal resonator characteristics.
- If not using the built-in oscillation amplifier and using instead an oscillation module, etc., as the clock source, connect the output of an external clock supply source to XIN. At this time, it is not necessary to connect a feedback resistor between XIN and XOUT.
- Supply the 12.288MHz or 24.576MHz clock set with XINSEL to XIN. If inputting another frequency to XIN, it is necessary to perform a setting with FSERR so that even if the input data sampling frequency changes, the result is not reflected to the error flag. Operation is made possible by performing this setting. However, since time definition gap occurs in relation to the recommended frequency operation, the encoding result cannot be used for input fs calculations. In this case, the input fs can be calculated by performing decimal division of the count value with 1/2000th of the XIN input frequency. For details, see Chapter 10 Microcontroller Interface.
- Since the XIN clock serves as the reference for internal processing, complete the XINSEL setting prior to bi-phase data input.
- Always perform clock supply to XIN for the following applications.

  (1) Detection of bi-phase data input
  (2) Clock source during PLL is unlocked
  (3) Input data sampling frequency calculation
  (4) Time definition during input data switching
  (5) External supply clock source (AD converter clock, etc.) for XIN source

- The oscillation amplifier automatically stops while PLL is locked. However, it can also be set for continuous operation with AMPOPR0,1. Although setting the continuous operation mode enables input data detection and input sampling frequency calculation even when the PLL is locked, this has an effect on the sound quality because the oscillation amplifier and PLL clock coexist.
- If the oscillation amplifier is set to continuous operation with AMPOPR0,1 while PLL is locked, RERR outputs an error ("H") once. This is because, at the same time that the oscillation amplifier goes into the operating state, the fs calculation value held when its operation stopped is reset. This error has no influence on clock output, but RDATA is muted while this error occurs. Therefore, the AMPOPR0,1 setting must be completed either prior to bi-phase data input or during PLL unlock.
- The oscillation amplifier can be stopped if it is unnecessary. However, when the operation is resumed after being stopped, return to the normal operation after an interval of 10ms or longer to allow the resonator oscillation to stabilize.
- XMCK outputs the XIN clock. The XMCK output settings are performed with XMSEL0,1. The XIN clock can be set to 1/1, 1/2, and muted output.
- When using the modulation function only, no clock needs to be supplied to XIN. In this case, use the built-in oscillation amplifier and frequency divider for MCK, BCK, and LRCK clock generation. If using only the oscillation amplifier, input the crystal resonator frequency to XIN and XOUT or an external clock to XIN, and fix the potential of digital data input pins RX0 to RX6. At this time, do not perform the DIR function stop setting with RXOPR and PLLOPR. The output clock may be muted.

8.1.4 Master clock and clock source switching

- The RMCK, RBCK, and RLRCK (hereunder, R system), and the SBCK and SLRCK (hereunder, S system) clock sources can be selected from the following three master clocks.

  (1) PLL source (256fs or 512fs)
  (2) XIN source (12.288MHz or 24.576MHz)
  (3) TMCK source (256fs)

- Clock source switching can either be done in one of two ways, by either setting the R system and the S system on an interconnected basis, or fixing the S system to the XIN source and setting only the R system. This setting is performed with SELMTD, OCKSEL, and RCKSEL.
- The clock source is automatically switched between PLL clock and XIN clock by locking/unlocking the PLL. The continuity of the clock is maintained at this time. However, if switching the clock source with SELMTD, the continuity of the S system is not maintained.
- The clock source can be switched to XIN with OCKSEL and RCKSEL, regardless of the PLL status. The clock source switch command and clock output of the R and S systems are shown below.

Table 8.1. Correspondence between Clock Source Switch Commands and Clock Output Pins

SELMTD	R System Output Clock	S System Output Clock
0	According to OCKSEL	According to OCKSEL
1	According to RCKSEL	Fixed to XIN source

Table 8.2. Relationship between Clock Source Switch Commands and Clock Sources when PLL Locked/Unlocked

SELMTD	OCKSEL	RCKSEL	R System Clock Source		S System Clock Source	
			Locked	Unlocked	Locked	Unlocked
0	0	X	PLL	XIN	PLL	XIN
	1	X	XIN	XIN	XIN	XIN
1	X	0	PLL	XIN	XIN	XIN
	X	1	XIN	XIN	XIN	XIN

- The TMCK source is selected with EXSYNC. This setting results in the same operation as when 256fs is set with the PLL source. Set PLLSEL to 256fs.
- The various clocks are output with the TMCK source as the master clock, similarly to the PLL clock status when data synchronized with the TMCK source is input. In this case too, the XIN source is switched with OCKSEL and RCKSEL. When the TMCK source is not supplied or the input data is not synchronized, the source is switched to the XIN source similarly to the PLL source unlocked status.
- The PLL status can always be monitored with RERR even after the XIN source is switched. Moreover, the processed information can be read with the microcontroller interface regardless of the PLL status.
- When the PLL changes from the locked to the unlocked status, the timing for switching the clock from the PLL source to the XIN source can be changed with XTWT0,1. Use these commands if noise occurs during clock switching.

8.1.5 Cautions on switching clock source while PLL is locked

- Clock continuity is maintained when switching the clock to the XIN source with SELMTD, OCKSEL, and RCKSEL when the oscillation amplifier is stopped while the PLL is locked (initial setting), but RERR outputs an error ("H") once. This is because, although the oscillation amplifier goes into the operating state at the same time that the clock is switched to the XIN source, and calculation of the input fs (sampling frequency) resumes, the previous fs calculation value is reset and processing is performed as if the fs value had changed compared to the newly calculated fs value.
- The following settings must be performed in order to switch the clock source with SELMTD, OCKSEL, and RCKSEL while PLL is locked while maintaining the RERR status.

  (1) Set the oscillation amplifier to the continuous operation mode with AMPOPR0,1.
  (2) Set with FSERR the mode for not reflecting fs changes to the error flag.

- By performing one of the above settings, it is possible to control the RERR change status when switching the clock source with SELMTD, OCKSEL, and RCKSEL.
- When switching the clock source to XIN from the status where the oscillation amplifier is stopped while the PLL is locked, the output clock using XIN as the source is output after the oscillation amplifier starts operating. Switching of the clock source from XIN to PLL when the PLL is locked is performed instantaneously, and clock continuity is maintained in either case.

8.1.6 Master clock block diagram (TMCK, XIN, XOUT, RMCK, XMCK)

- The relationships between the three master clocks, switching, and the frequency division function, are shown.
- The contents in the square brackets [***] by the switch function blocks correspond to the write command names.
- Lock/Unlock switching is automatically performed through PLL locking/unlocking.

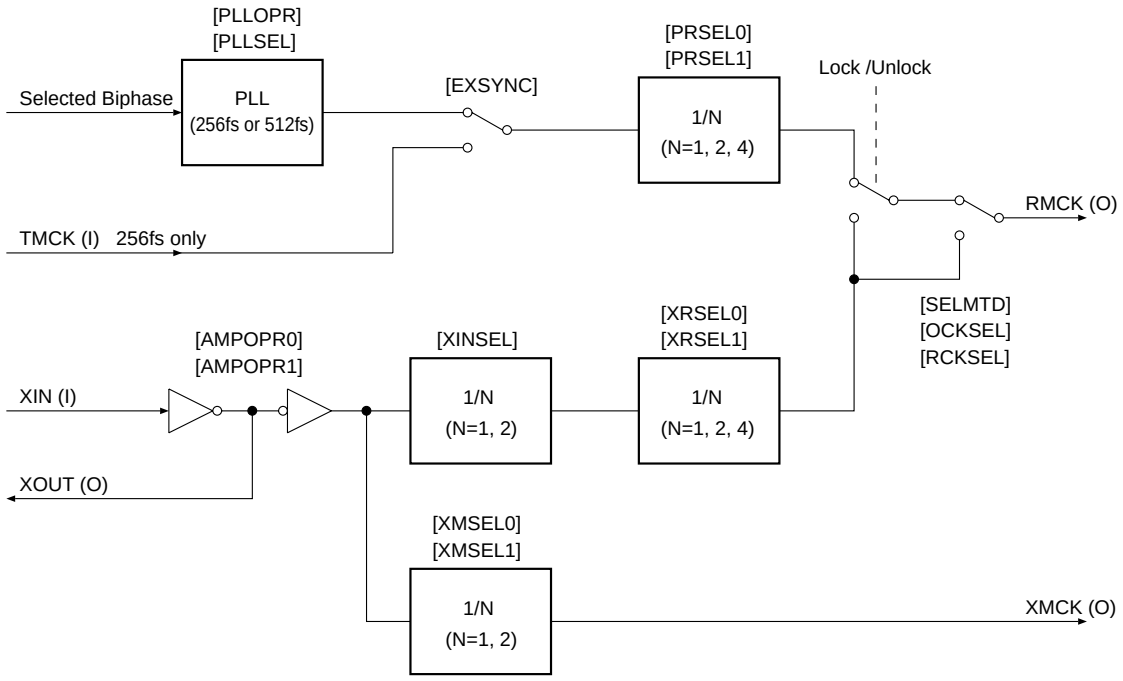


Figure 8.2. Master Clock Block Diagram

8.1.7 Output clocks (RMCK, RBCK, RLRCK, SBCK, SLRCK)

- The LC89057W-VF4-E features two clock systems in order to supply the various needed clocks to the A/D converter, DSP, and other peripheral devices.
- The clock output settings for the R and S systems are done with PRSEL0,1, XRSEL0,1, XRBCK0,1, XRLRCK0,1, PSBCK0,1, PSLRCK0,1, XSBCK0,1, and XSLRCK0,1.

(a) Setting range for clock output pins when using PLL source
  (1) RMCK: Select from 1/1, 1/2, and 1/4 of 512fs or 256fs
  (2) RBCK: 64fs output
  (3) RLRCK: fs output
  (4) SBCK: Select from 128fs, 64fs, and 32fs
  (5) SLRCK: Select from 2fs, fs, and fs/2

(b) Setting range for clock output pins when using XIN source
  (1) RMCK: Select from 1/1, 1/2, and 1/4 of 12.288MHz or 24.576MHz
  (2) RBCK: Select from 12.288MHz, 6.144MHz, and 3.072MHz
  (3) SBCK: Select from 12.288MHz, 6.144MHz, and 3.072MHz
  (4) RLRCK: Select from 192kHz, 96kHz, and 48kHz
  (5) SLRCK: Select from 192kHz, 96kHz, and 48kHz

- The polarity of RBCK, RLRCK, SBCK, and SLRCK can be reversed with RBCKP, RLRCKP, SBCKP, and SLRCKP.
- Clock switching is processed from the rising edge of RLRCK output after the falling edge of microcontroller interface CE.

Table 8.3. Output Clock Frequencies (Bold Items = Initial Settings)

Output Pin Name	PLL Source		TMCK Source	XIN Source	
	512fs	256fs	256fs	12.288MHz	24.576MHz
RMCK	512fs **256fs** 128fs	256fs **128fs** 64fs	256fs **128fs** 64fs	**12.288MHz** 6.144MHz 3.072MHz	**24.576MHz** 12.288MHz 6.144MHz
RBCK	**64fs**			12.288MHz 6.144MHz **3.072MHz**	
RLRCK	**fs**			192kHz 96kHz **48kHz**	
SBCK	128fs **64fs** 32fs			12.288MHz 6.144MHz **3.072MHz**	
SLRCK	2fs **fs** fs/2			192kHz 96kHz **48kHz**	

8.1.8 Output clocks block diagram (RMCK, RBCK, RLRCK, SBCK, SLRCK, XMCK)

- The relationships between the output clock and switch function are shown below.
- PLL in the figure indicates the PLL source (or TMCK source), and XIN the XIN source.
- The contents in the square brackets [***] by the switch function blocks correspond to the write command names.
- The broken lines connecting the switches indicate coordinated switching.
- Lock/Unlock switching is automatically performed through PLL locking/unlocking.
- Master/slave switching is done through demodulation function master/slave function switching.

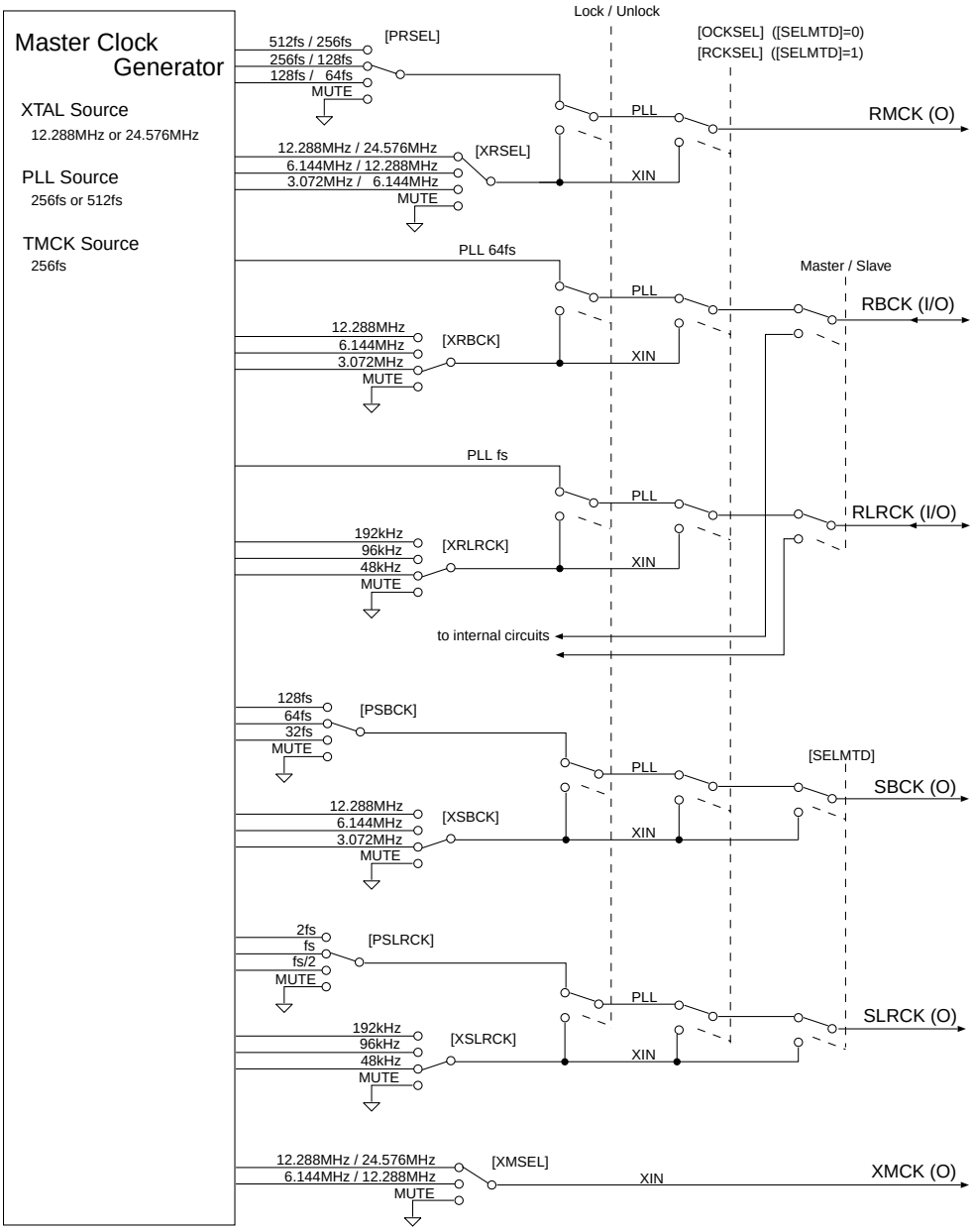
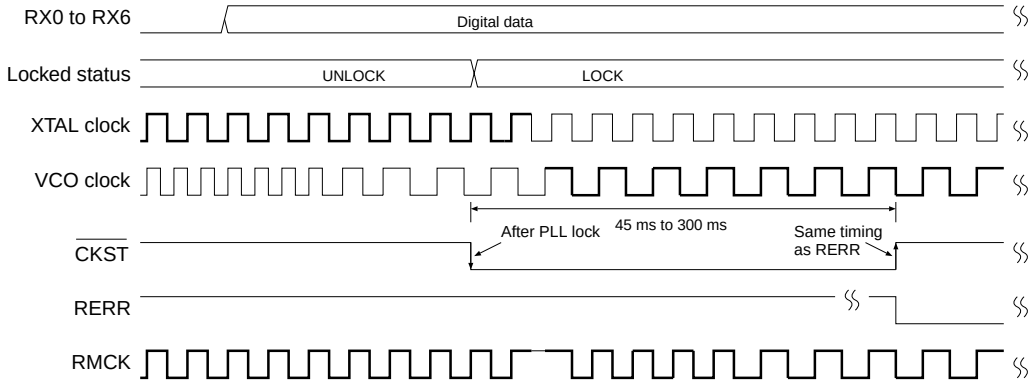


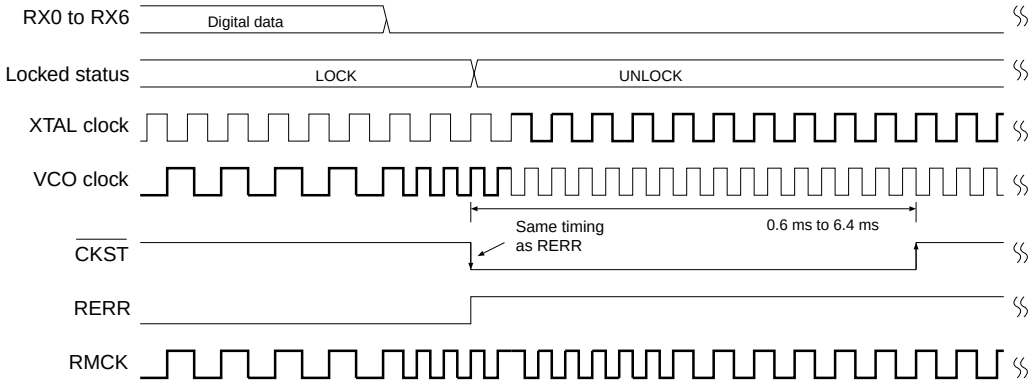
Figure 8.3. Clock Output Block Diagram

8.1.9 Clock switch transition signal output ($\overline{CKST}$)

- $\overline{CKST}$ outputs "L" when the output clock changes through PLL lock/unlock.
- In the lock-in stage, the $\overline{CKST}$ "L" pulse falls at the word clock generated from the XIN clock after PLL is locked following detection of input data, and rises at the same timing as RERR following the lapse of a given period.
- In the unlock stage, the $\overline{CKST}$ "L" pulse falls at the same timing as PLL lock detection signal RERR and rises following a given number of word clocks generated from the XIN clock has been counted.
- The PLL lock status change and clock change timing can be known through detection of the rising and falling edges of the $\overline{CKST}$ "L" pulse.



(a) Lock-in stage



(b) Unlock stage

Figure 8.4. Clock Switch Timing

8.2 Bi-Phase Signal Input/Output

8.2.1 Bi-phase signal input reception range

- The input data reception range depends on the PLL lock frequency setting done with PLLSEL. The relationship between this setting and the guaranteed reception range is shown below.

Table 8.4. Relationship between PLL Output Clock Setting and Reception Range (FSLIM0,1 = 0)

PLL Output Clock Setting	Input Data Reception Range
512fs (PLLSEL = 0)	28kHz to 105kHz
256fs (PLLSEL = 1)	28kHz to 195kHz

- The fs reception range for input data within the above PLL output clock setting range can be controlled. This setting is performed with FSLIM0,1. When this function is used, input data that exceeds the setting range is considered as an error and the clock source is automatically switched to the XIN source and RDATA output data is according to the RDTSEL setting.

8.2.2 Bi-phase signal input/output pins (RX0 to RX6, RXOUT)

- There are 7 digital data input pins. Moreover, data modulated with the modulation function can also be selected and thus selection from among 8 signals including this signal is possible. However, the pins that can be selected is restricted by the setting conditions.

  (1) The six pins RX0 and RX2 to RX6 are TTL level input pins with 5V input level tolerable.
  (2) RX1 is a coaxial-compatible input pin with built-in amplifier that can receive up to 200mVp-p data.

- The demodulation input and RXOUT output signals can each be selected independently.

  (1) The demodulation data is selected with RISEL0 to 2.
  (2) The RXOUT output data is selected with ROSEL0 to 2.

- RXOUT can be muted with RXOFF. Muting is recommended when not using RXOUT in order to reduce clock jitter.
- The data input status can be monitored with the RXMON setting. The status of each data input pin is stored in CCB address 0xEA and output registers DO0 to DO7. Since this function uses the XIN clock, the oscillation amplifier must be set to the continuous operation mode when RXMON is set.
- Demodulation input pin switching can be performed via PLL unlock with the ULSEL setting. As a result, data switching can be accurately communicated to peripheral devices.
  The interval from pin switching through RISEL0 to 2 until data is received is about 250µs to 350µs. This function also requires that the oscillation amplifier be set to the continuous operation mode.

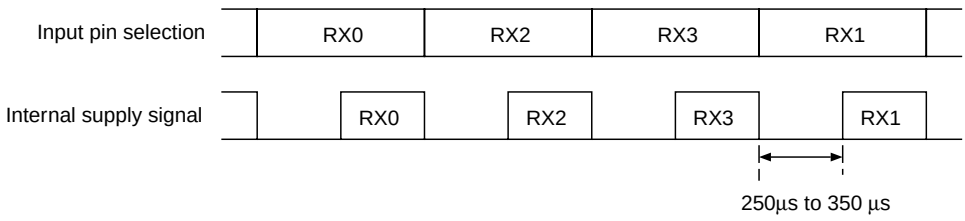
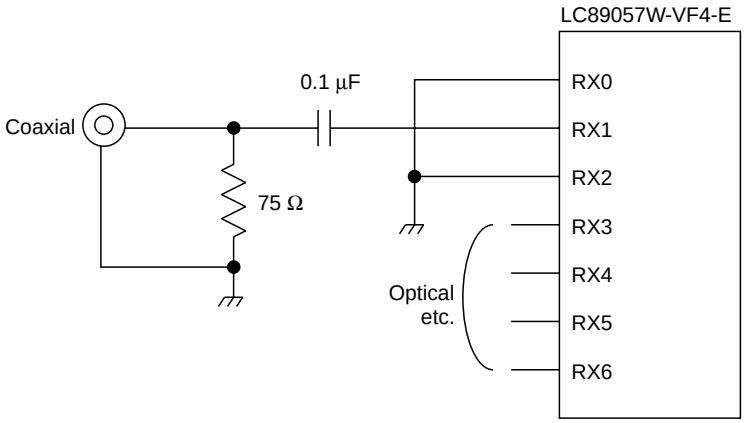


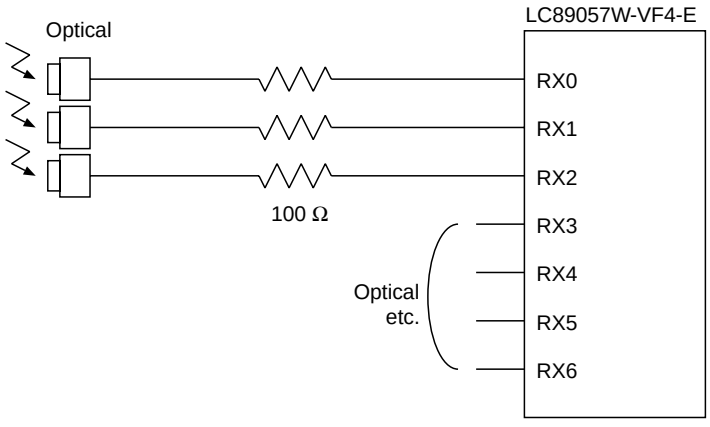
Figure 8.5. Input Pin Selection Processing via PLL Unlock

8.2.3 Bi-phase signal input circuits (RX0, RX1, RX2)

- If using RX1, which has a built-in amplifier, as a coaxial input pin, malfunction may occur due to the influence of the adjacent RX0 and RX2 input pins. To prevent them from influencing RX1, fix RX0 and RX2 to "L".
- If, when RX1 is selected, the input signal to RX1 is temporarily open because of AC coupling, the RX0 and RX2 potential must be fixed. In this case, there are 5 bi-phase signal input pins that can be selected, RX1 and RX3 to RX 6.
- If, when RX1 is selected, the input signal to RX1 is absolutely fixed to either "H" or "L", RX0 and RX2 handling is not required. In this case, all 7 input pins are valid and can be used.



(a) Coaxial input circuit



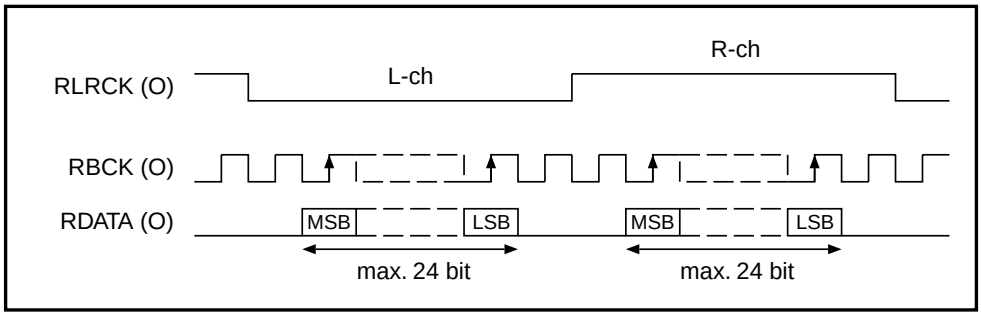
(b) Optical input circuit

Figure 8.6. Bi-Phase Signal Input Circuits

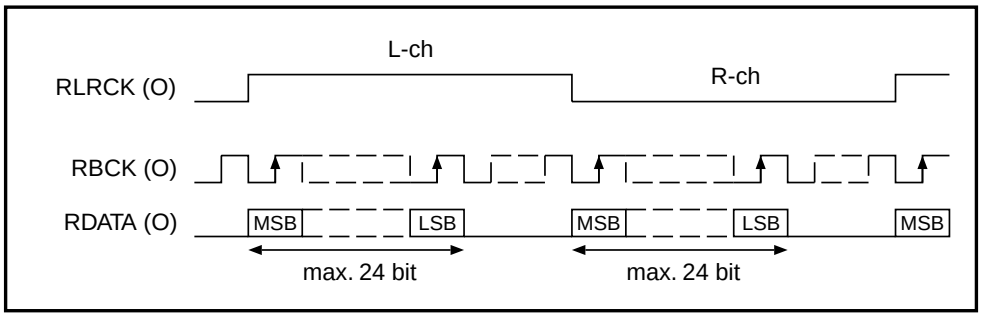
8.3 Serial Audio Data Input/Output

8.3.1 Output data format (RDATA)

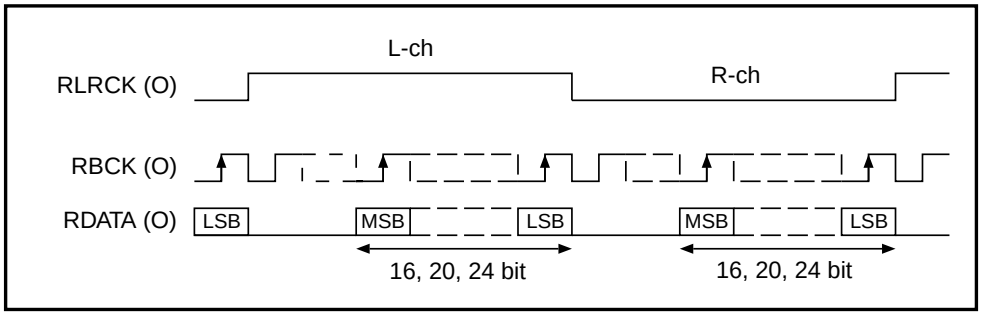
- The output format is set with OFSEL0 to OFSEL2.
- I^2S is the initial output format setting.
- Back-loading output is valid only in the master mode. In the slave mode, correct data is not output.
- Output data is output in synchronization with the RLRCK edge immediately after the RERR output becomes "L".



(0): I2S data output



(1) MSB-first front-loading data output

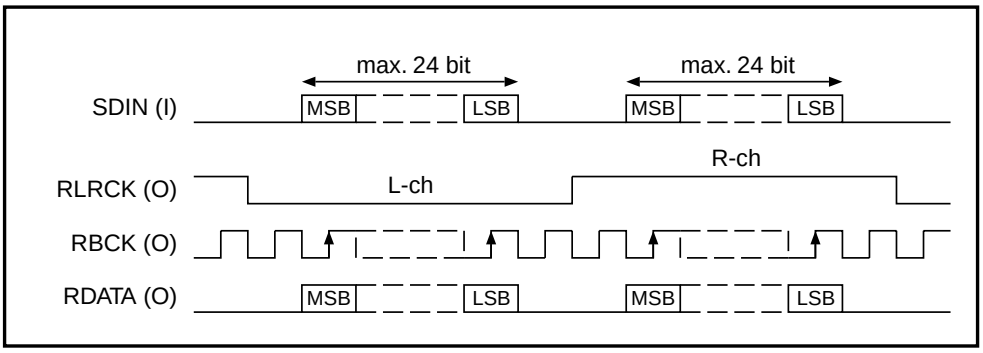


(2) MSB-first back-loading data output

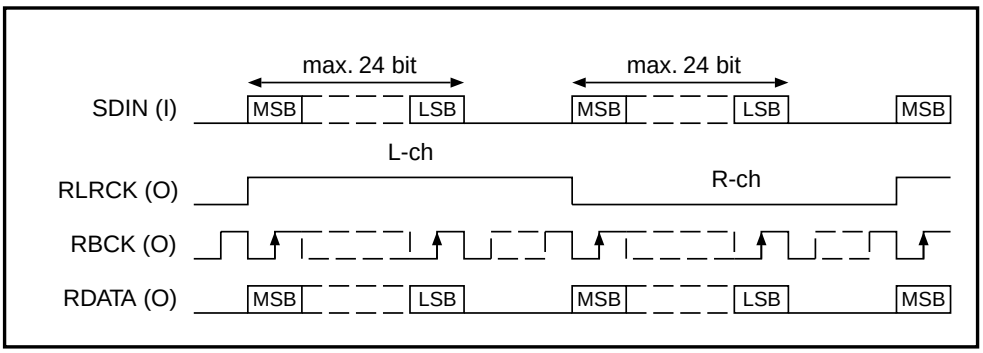
Figure 8.7. Data Output Timing

8.3.2 Serial audio data input format (SDIN)

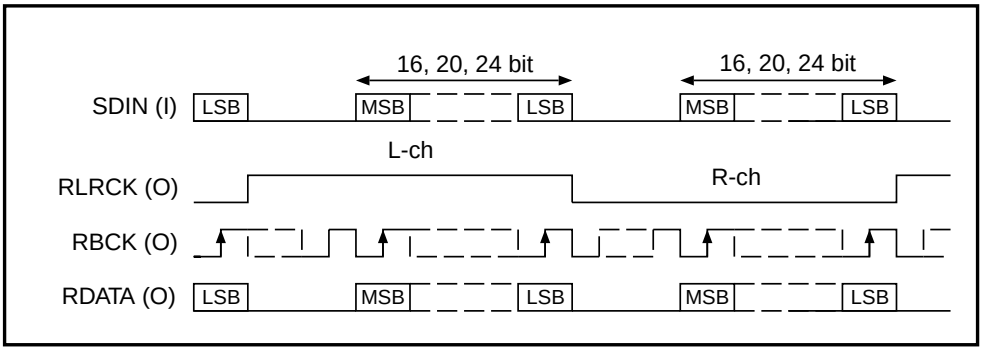
- A 24 bit input serial digital audio data input pin, the SDIN, is provided.
- Make the format of the serial audio data input to SDIN the same as the demodulation data output format.



(0): I2S data input



(1) MSB-first front-loading data input

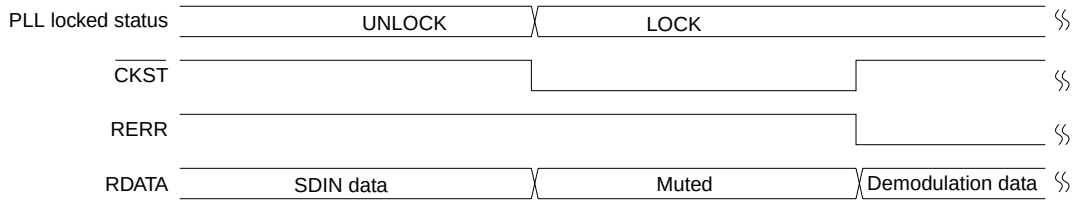


(2) MSB-first back-loading data input

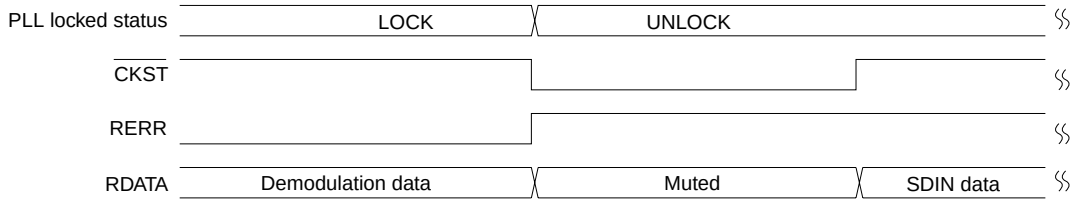
Figure 8.8. Serial Audio Data Input Timing

8.3.3 Output data switching (SDIN, RDATA)

- RDATA outputs demodulation data when the PLL is locked, and SDIN input data when the PLL is unlocked. This switching is automatically performed according to the locked/unlocked status of the PLL. For details, see the timing charts below.
- When SDIN input data is selected, switch to a clock source synchronized to the SDIN data.
- With the RDTSTA setting, the SDIN input data is output to RDATA regardless of the locked/unlocked status of the PLL.
- With the RDTMUT setting, the RDATA output data can be forcibly muted.
- Even when the clock source is set to XIN with OCKSEL and RCKSEL, the PLL continues operating as long as its operation is not stopped with PLLOPR. At this time, the PLL status is continuously output from RERR as long as error output is not forcibly set with RESTA. Moreover, the processed information can be read with the microcontroller interface regardless of the PLL status.



(a) Lock-in stage



(b) Unlock stage

Figure 8.9. RDATA Output Data Switch Timing Chart

8.3.4 Data block diagram (RX0 to RX6, TX0, RXOUT, TDATA, RDATA, SDIN)

- The RDATA output data is switched to SDIN input data with RDTSEL.
- The SDIN input data can be input to the modulation function with TDTSEL.
- Since the modulation output is input to the input switch multiplexer, it can be fetched from RXOUT. Using this function, it is possible to use a signal that has been digitized with the A/D converter for digital recording output, etc.

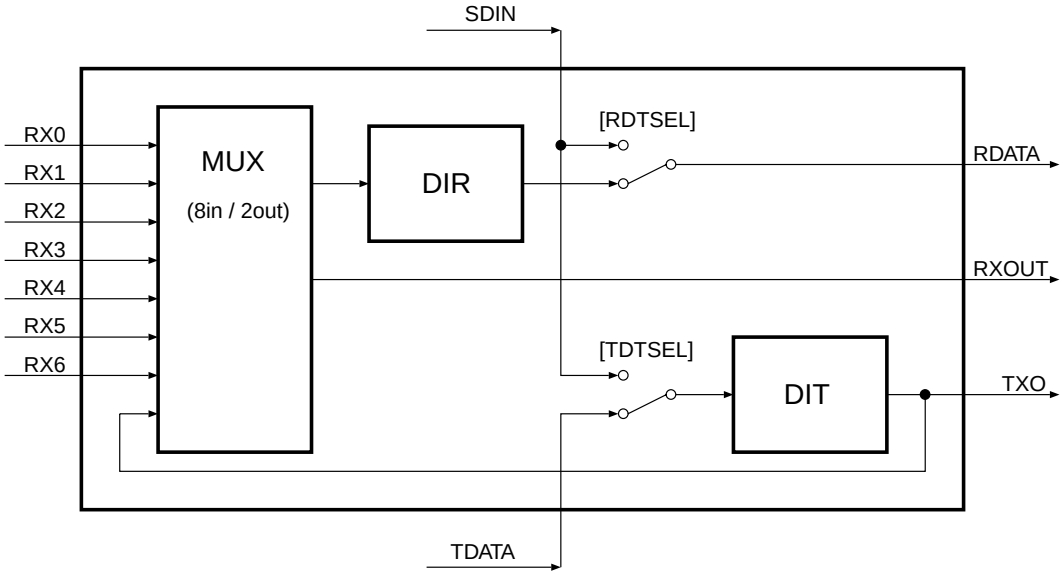


Figure 8.10. Data Block Diagram

8.3.5 Calculation of input data sampling frequency

- The input data sampling frequency is calculated using the XIN clock.
- In the mode where the oscillation amplifier automatically stops when the PLL becomes locked, the input data sampling frequency is calculated during the RERR error period, the calculation is completed at the same time that the oscillation amplifier stops, and that value is then held. Therefore, following calculation completion, the value remains unchanged until the PLL becomes unlocked.
- In the mode where the oscillation amplifier operates continuously, calculation processing is performed continuously. Even if sampling changes within the PLL capture range for input data whose channel status sampling information does not change, the calculation results that follow the input data can be read.
- The calculation result can be read from CCB address 0xEB and output registers DO4 to DO7 and DO8 to DO15. Registers DO4 through DO7 hold the encoded result, while DO8 through DO15 hold the calculation value. However, as the calculation count value is output in 8-bit units, the sampling frequencies that can be calculated are greater than 24kHz. For details, see Chapter 10 Microcontroller Interface.

8.4 Error Output Processing

8.4.1 Lock error, data error output (RERR)

- RERR outputs an error flag when a PLL lock error or a data error occurs.
- Non-PCM data reception can be treated as an error with the RESEL setting.
- The RERR output conditions are set with RESTA. Since the PLL status can be output at all times, the PLL status can be monitored at all times, even when the clock source is XIN.

8.4.2 PLL lock error

- The PLL gets unlocked for input data that has lost bi-phase modulation regularity, or input data for which preambles B, M, and W cannot be detected.
- RERR goes "H" upon occurrence of a PLL lock error, and returns to "L" when data demodulation returns to normal and "H" is maintained for between 45ms and 300ms.
- The rising and falling edges of RERR are synchronized with RLRCK.

8.4.3 Input data parity error

- Odd number of parity bits in input data errors and input parity errors are detected.
- If an input parity error occurs 9 or more times in succession, RERR goes "H" indicating that the PLL is locked, and after holding "H" for between 45ms and 300ms, it returns to "L".
- The error flag output format for when an input parity error is output 8 times in succession can be selected with REDER.

8.4.4 Other errors

- Even if RERR goes "L", the channel status bits 24 to 27 (sampling frequency) are always fetched and the data of the previous block is compared with the current data. Moreover, the input data sampling frequency is calculated from the fs clock extracted from the input data, and fs calculation value comparison is performed as described above. If a difference is detected, RERR is instantly made "H" and the same processing as for PLL lock errors is performed.
- The PLL causes a lock error when the sampling frequency changes as described above. However, in order to support sources with a variable sampling frequency (for example a CD player with a variable pitch function), it is possible to perform a setting with FSERR so that no error flag is output if the sampling frequency variation falls within the PLL capture range.
  Moreover, the FSERR setting prevents fs calculation results for input data within the reception range set with FSLIM0,1 from being reflected to the error flag, and if the PLL status changes to the locked status, it causes RERR to go "L".
- If a setting such that an error occurs when non-PCM data is input is performed with RESEL, RERR changes to "H" output upon detection of non-PCM data input. At this time, the PLL locked status and various output clocks are according to the input data, but the output data is muted.

8.4.5 Data processing upon error occurrence (lock error, parity error)

- The data processing upon occurrence of an error is described below. If 8 or fewer input parity errors occur in succession, transfer data is replaced by the data saved to L-ch and R-ch in the previous frame in the case of PCM audio data. However, if the transfer data is non-PCM data, the error data is output as is. Non-PCM data is data when bit 1 non-PCM data detection bit of the channel status goes "H" based on data detected prior to occurrence of an input parity error.
- Output data is muted upon occurrence of a PLL lock error or when a parity error occurs 9 or more times in succession.
- For the channel status, the data of the previous block is held in 1-bit units when a parity error occurs.

Table 8.5. Data Processing upon Error Occurrence

Data	PLL Lock Error	Input Parity Error (a)	Input Parity Error (b)	Input Parity Error (c)
RDATA output	"L"	"L"	Previous value data	Output
fs calculation result	"L"	Output	Output	Output
Channel status	"L"	"L"	Previous value data	Previous value data
Validity flag	"L"	"L"	Output	Output
User data	"L"	"L"	Output	Output

* Input parity error (a): If occurs 9 or more times in succession
* Input parity error (b): If occurs 8 or fewer times in succession, in case of audio data
* Input parity error (c): If occurs 8 or fewer times in succession, in case of non-PCM burst data

- Figure 8.11 shows an example of data processing upon occurrence of a parity error.

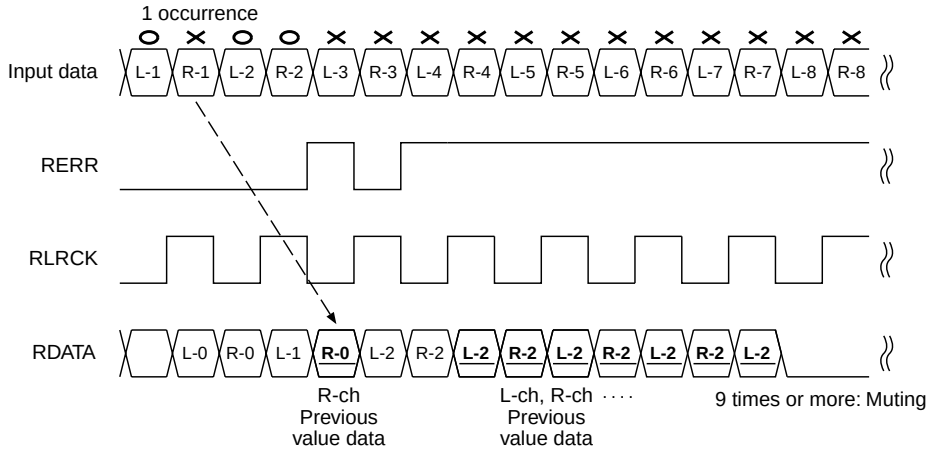


Figure 8.11. Data Processing upon Parity Error Occurrence

8.4.6 Processing during error recovery

- When preambles B, M, and W are detected, PLL becomes locked and data demodulation begins.
- RDATA output data is output from the RLRCK edge after RERR goes "L".

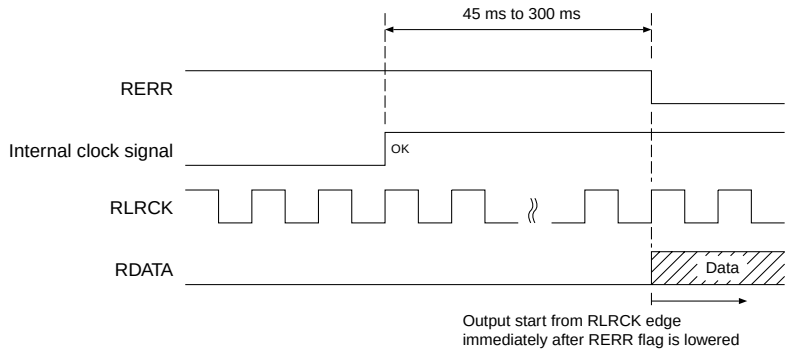


Figure 8.12. Internal Lock Signal

8.5 Channel Status Output

8.5.1 Data category specification bit 1 output ($\overline{\text{AUDIO}}$)

- $\overline{\text{AUDIO}}$ outputs bit 1 of the channel status that indicates whether the input bi-phase data is PCM audio data. $\overline{\text{AUDIO}}$ is immediately output upon detection of RERR even during "H" output.
- ORed output with IEC61937 or the DTS-CD/LD detection flag is also possible with AOSEL.

Table 8.6. $\overline{\text{AUDIO}}$ Output

$\overline{\text{AUDIO}}$	Output Conditions
0	PCM audio data (CS bit 1 = "L")
1	Non-audio data (CS bit 1 = "H"

8.5.2 Emphasis information output (EMPHA)

- EMPHA outputs a signal that indicates the presence or absence of 50/15μs emphasis for consumer and broadcast studio.
  EMPHA is immediately output upon detection of RERR even during "H" output.

Table 8.7. EMPHA Output

EMPHA	Output Conditions
0	No pre-emphasis
1	50/15 μs pre-emphasis

8.6 Other Outputs

8.6.1. Validity flag output (VO)

- The validity flag can be output from $\overline{\text{AUDIO}}$ /VO by switching the $\overline{\text{AUDIO}}$ /VO output contents with VOSEL.
- The validity flags transferred at each sub-frame are output in the following timing.

Table 8.8. VO Output

VO	Output Conditions
0	No error (not burst data)
1	Error (May be burst data)

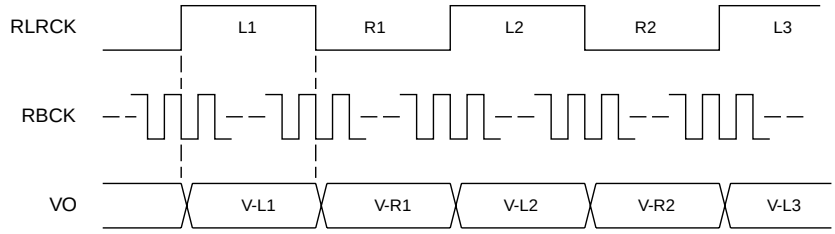


Figure 8.13. Validity Flag Output Timing

8.6.2 User data output (UO)

- User data can be output from EMPHA/UO by switching the EMPHA/UO output contents with UOSEL.
- The user data transferred at each sub-frame is output in the following timing.

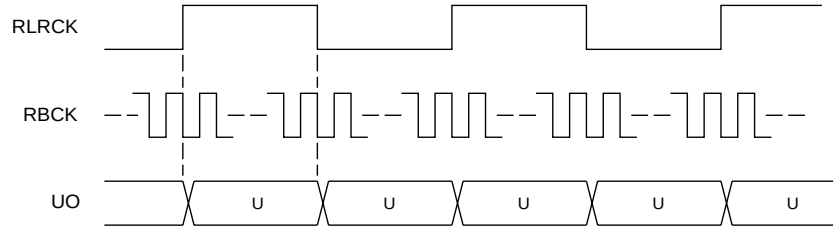
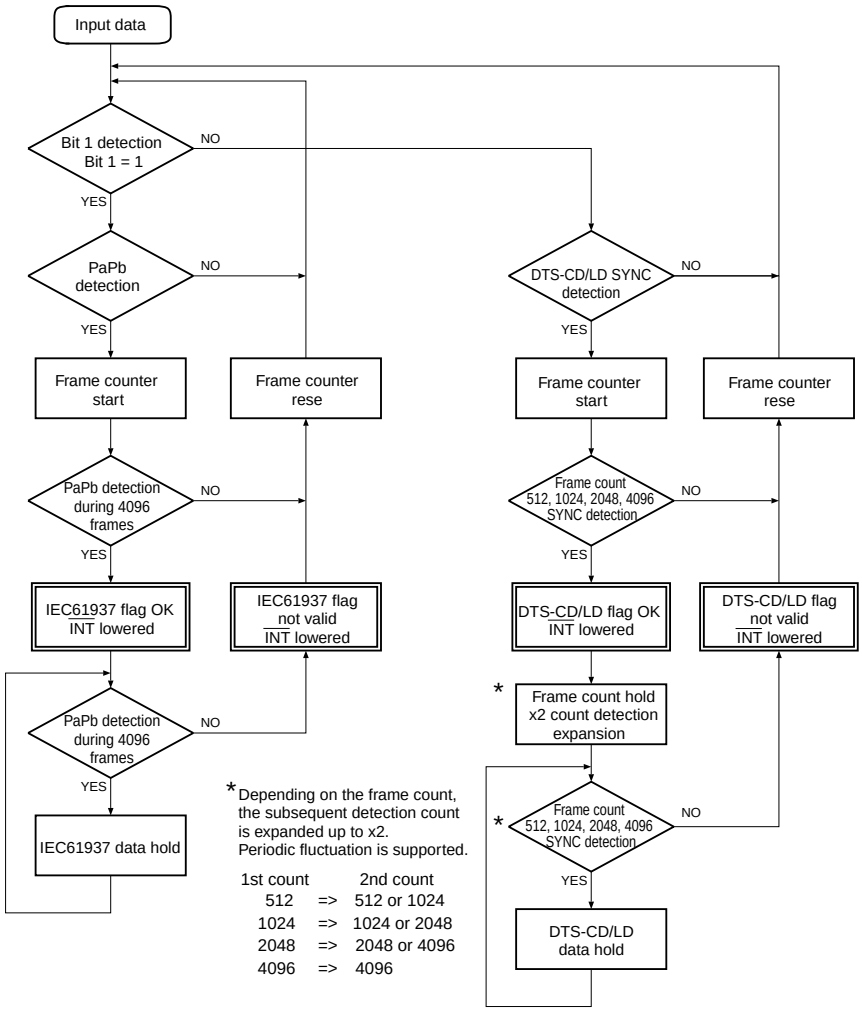


Figure 8.14. User Data Output Timing

8.7 IEC61937, DTS-CD/LD Detection Flag Output

- A function to output IEC61937 and DTS-CD/LD detection flags for non-PCM data is provided.
- When the UNPCM non-PCM signal output setting is selected through the $\overline{\text{INT}}$ output contents setting, an interrupt signal is output from $\overline{\text{INT}}$ upon detection of an IEC61937 or DTS-CD/LD sync signal. Non-PCM signal details can be known by reading this information from the output register.
- When channel status bit 1 is non-PCM data ("1"), the IEC61937 sync signal is detected and output. If bit 1 is PCM data, the IEC61937 sync signal is not output.
- DTS-CD/LD sync signal detection is done based on the sync pattern and the base frequency. In the case of DTS-ES data detection, output is performed when the DTS5.1 channel sync signal is detected and the DTS-ES sync pattern has been verified.
- The IEC61937 and DTS-CD/LD detection flags are cleared when fs has changed or upon occurrence of a PLL lock error or data error.
- Since the DTS sync signal is provided within the audio data, digital data with the same code as the DTS sync signal may in rare cases exist for regular CD/LD records that are not recorded in the DTS format. Protection using the sync pattern or base frequency is provided so that such data is not misinterpreted as DTS-CD/LD detection flags. The detection sequence is shown below.



9 Description of Modulation Function and General-Purpose I/Os

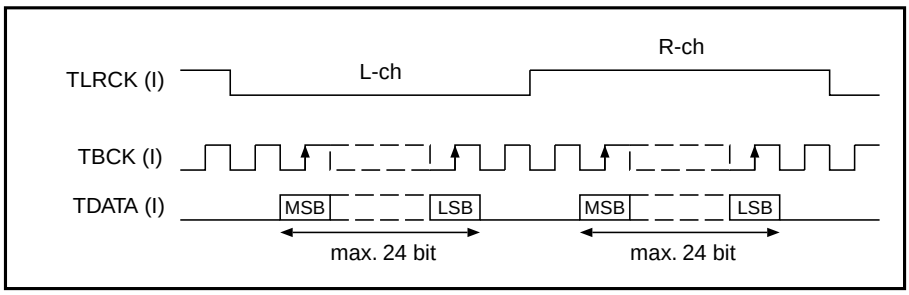
9.1 Modulation function usage method

9.1.1 Initial setting

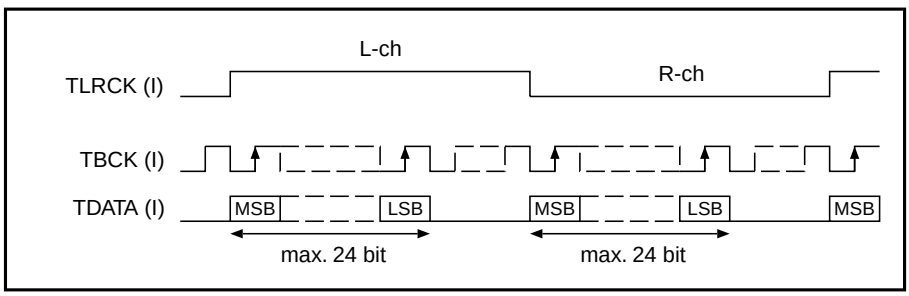
- The modulation function and general-purpose I/O port function cannot be used simultaneously because they share the same pins. To select the modulation function, pull down $\overline{INT}$ with a 10kΩ resistor. For the setting method, see Chapter 7.
- In the initial setting, the modulation function is stopped. The setting to use the modulation function is performed with TXOPR.

9.1.2 Data output (TMCK, TBCK, TLRCK, TDATA, TXO)

- Bi-phase modulated data is output from TXO by inputting a 256fs clock to TMCK, 64fs clock to TBCK, fs clock to TLRCK, and audio data to TDATA.
- The polarity of the TLRCK clock is set with TXLRP.
- Input data can be modulated in the sampling range of 32kHz to 192kHz, transfer rate of 4MHz to 25MHz, and up to 24 bit data.
- The initial value for the input data format is I^2S. Switching to MSB-first front-loading input is set with TXDFS.
- For the channel status, the first 48 bits of data can be written with the microcontroller interface.
- TXO is fixed to "L" by setting TXOPR to Stop.



(0) I2S data input



(1) MSB first front-loading data input

Figure 9.1. Data Input Timing

9.1.3 Validity flag input (VI)

- Validity flags can be input from RX5/VI by switching the RX5/VI input contents with VISEL.
- The validity flag write timing is shown below. The validity flag can be written with the microcontroller interface, but port settings have priority.
- Writing validity flags with the microcontroller interface is done using VMODE.

Table 9.1. RX5/V1 Input

RX5/VI	Output Conditions
0	No error
1	Error

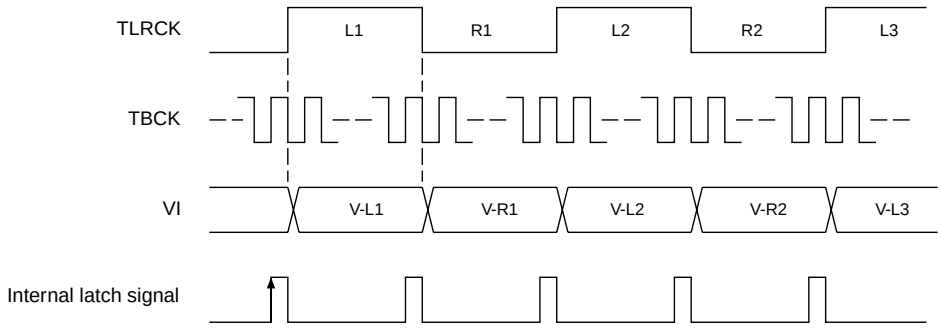


Figure 9.2. Validity Flag Input Timing

9.1.4 User data input (UI)

- User data can be input from RX6/UI by switching the RX6/UI input contents with UISEL.
- The user data write timing is shown below.

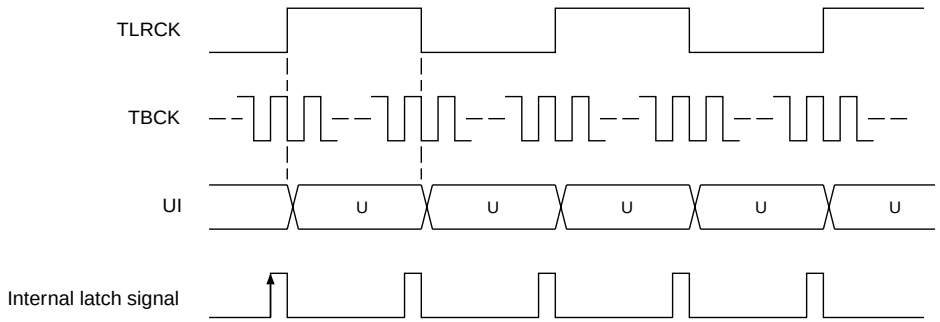


Figure 9.3. User Data Input Timing

9.1.5 Modulated output of SDIN input data

- SDIN input data is modulated and that output can be fetched from TXO and RXOUT.
- The setting to modulate SDIN input data is performed with TDTSEL.
- Input a clock synchronized with SDIN to TMCK, TBCK, and TLRCK.
- Match the SDIN input data format to the setting used during modulation processing.

9.1.6 Monaural output

- It is possible to output the data of only one input data channel at the rate of 1/2 the input fs with TXMOD0,1.
- This operation maintains the bi-phase modulation regularity, but there is no correlation between the data and preambles.
- Channel status write is synchronized with the output rate.
- The validity flag and user data are written in frame units. Input the same data to the L and R channels.
- To process the stereo signals of two channels with this setting, two LC89057W-VF4-E are required.

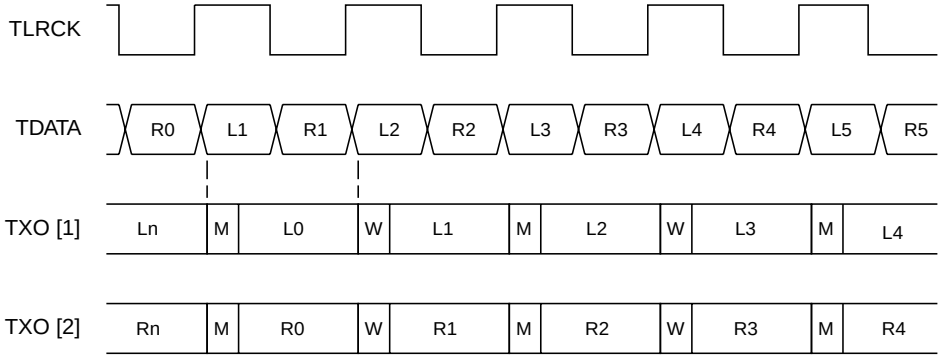


Figure 9.4. Modulation of Data of Single Channel

9.2 General-Purpose I/Os (PIO0, PIO1, PIO2, PIO3 PIOEN)

9.2.1 Initial settings

- The modulation function and general-purpose parallel I/Os share the same pins and therefore cannot be used simultaneously. To use the general-purpose I/Os, pull up $\overline{\text{INT}}$ with a 10kΩ resistor. For the setting method, see Chapter 7.
- The general-purpose parallel I/O output function performs parallel conversion of the serial data input from the microcontroller interface and outputs the resulting data from PIO0 PIO1, PIO2, and PIO3. The input function saves the parallel data input to PIO0, PIO1, PIO2, and PIO3 to internal registers and reads the contents of these registers with the microcontroller interface.
- 4 bit general-purpose I/Os cannot be used for both input and output in mix. Switching between input and output is done with PIOEN. When PIOEN is "H", the general-purpose I/Os all become input pins. When PIOEN is "L", the general-purpose I/Os are all output pins.

9.2.2 Input/output settings

- Data handling for general-purpose I/Os is performed using the microcontroller interface and write/read registers. For details, see Chapter 10 Microcontroller Interface.
- General-purpose I/O write settings (Microcontroller → Write register → General-purpose I/O output)

  (1) To output data from general-purpose I/Os, set PIOEN to "L".
  (2) Set the data to be output to CCB address 0xE8, command address 0x10, and input registers DI12 to DI15.
  (3) During write operation, be sure to input "0" to modulation function setting registers DI8 to DI11.
  (4) The data written to PI0 to PI3 is output from the general-purpose I/Os.

- General-purpose I/O read settings (General-purpose I/O input → Read register → Microcontroller)

  (1) To input data to general-purpose I/Os, set PIOEN to "H".
  (2) The input data is saved to CCB address 0xEB and output registers DO0 to DO3.
  (3) Data can be sent to the microcontroller by reading PO0 to PO3.

10 Microcontroller Interface ($\overline{INT}$, CL, CE, DI, DO)

10.1 Description of Microcontroller Interface

10.1.1 Interrupt output ($\overline{INT}$)

- Interrupts are output when a change has occurred in the PLL lock status or output data information.
- Interrupt output is determined by the register for selecting the interrupt source, the INT pin that outputs that state transition, and the registers that store the interrupt source data.
- Normally $\overline{INT}$ outputs "L" upon occurrence of an interrupt while "H" is output. Following "L" output, it returns to "H" as dictated by the INTOPF setting.
- Select with INTOPF whether to hold the "L" pulse for a certain period and then clear it (to "H"), or clear it at the same time that the output register is read.
- The interrupt sources can be selected from among the following items. Multiple sources can be selected at the same time with the contents of CCB address 0xE8 and command address 0x08. $\overline{INT}$ outputs the result of ORing(addition) the selected interrupt sources.

$\overline{INT}$ output = (selected source 1) + (selected source 2) + ... + (selected source n)

Table 10.1. Interrupt Source Setting Contents

No.	Command Name	Description
1	ERROR	Output when RERR pin status has changed
2	INDET	Output when input data pin status has changed (Oscillation amplifier operation condition)
3	FSCHG	Output when input fs calculation result has changed. (Output amplifier condition)
4	CSRNW	Output when channel status data of first 48 bits has changed
5	UNPCM	Output when $\overline{AUDIO}$ pin status has changed
6	PCRNW	Output when burst preamble Pc has been updated
7	SLIPO	Output when data is read twice during slave setting and missing data is detected
8	EMPF	Output when emphasis information has changed

- The set interrupt source contents are saved to output registers DO8 to DO15 of CCB address 0xEA. However, the status of the RERR and $\overline{AUDIO}$ pins is output when the read registers for source items 1 and 5 are read. Except for source items 1 and 5, other data are saved to the registers upon occurrence of an interrupt source.
- If monitoring is performed even while the PLL is locked because the oscillation amplifier clock is used, the oscillation amplifier must be set to the continuous operation mode for source items 2 and 3.
- Clearing of $\overline{INT}$ at the same time that the output registers are read following the occurrence of an interrupt source is done immediately after output register 0xEA is set.
- The pulse width when the $\overline{INT}$ output following the occurrence of an interrupt source is set to the "L" pulse output mode is between 1/2fs and 3/2fs for one interrupt source.

10.1.2 CCB format

- The various function settings as well as information writing and reading are performed with the microcontroller interface.
- The data format of the microcontroller interface conforms to Sanyo's original serial bus format (CCB), but three-state instead of open-drain is employed for the data output format.
- Data input/output is performed following CCB address input. For the data input/output timing, see the input/output timing chart.

Table 10.2. Relationship between Register Input/Output Contents and CCB Addresses

Register input/output contents	R/W	CCB address	B0	B1	B2	B3	A0	A1	A2	A3
Function setting data input	write	0xE8	0	0	0	1	0	1	1	1
CS data input	write	0xE9	1	0	0	1	0	1	1	1
Interrupt data output	read	0xEA	0	1	0	1	0	1	1	1
fs data output	read	0xEB	1	1	0	1	0	1	1	1
CS data output	read	0xEC	0	0	1	1	0	1	1	1
Pc data output	read	0xED	1	0	1	1	0	1	1	1

10.1.3 Data write method

- Input is performed in the following sequence: CCB addresses of A0 to A3 and B0 to B3, chip addresses of DI0 and DI1, command addresses of DI4 to DI7, and data of DI8 to DI15. DI2 and DI3 are reserved for the system. Input "0".
- For the chip addresses, DI0 corresponds to CAL (low-order), and DI1 to CAU (high-order). For details, see section 7.2.

10.1.4 Data read method

- Read data is output from DO. DO is in the high impedance state when CE is "L", and begins output from the rising edge of CE after output setting is satisfied at the CCB address. DO then returns to the high impedance state at the falling edge of CE.
- If DO outputs using multiple LC89057W-VF4-E units are shared, the DO outputs of the LC89057W-VF4-E units for which data read is to be performed can be set to always be in the high impedance state with DOEN. With this setting, it is possible to read only the desired outputs.

10.1.5 Input/output timings

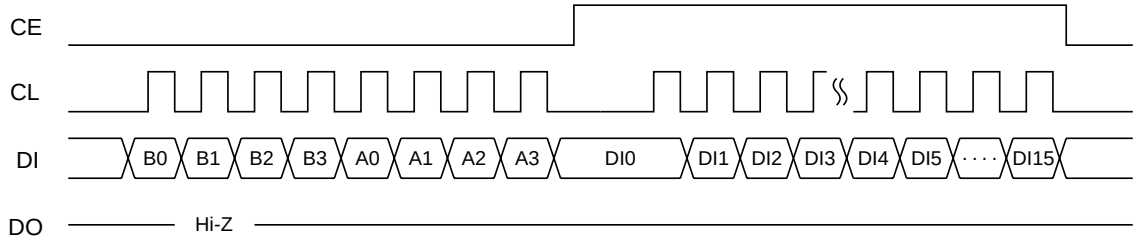


Figure 10.1. Input Timing Chart (Normal L Clock)

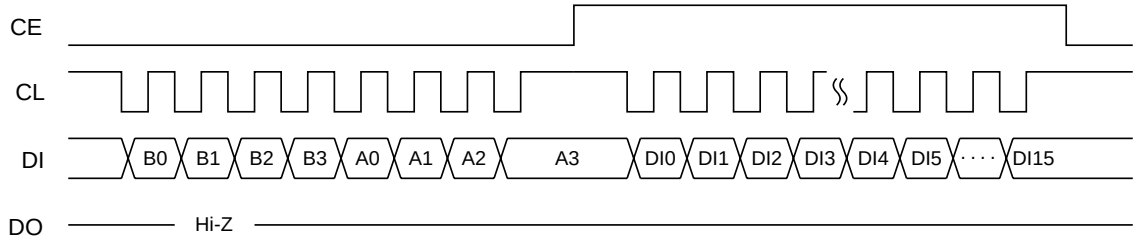


Figure 10.2. Input Timing Chart (Normal H Clock)

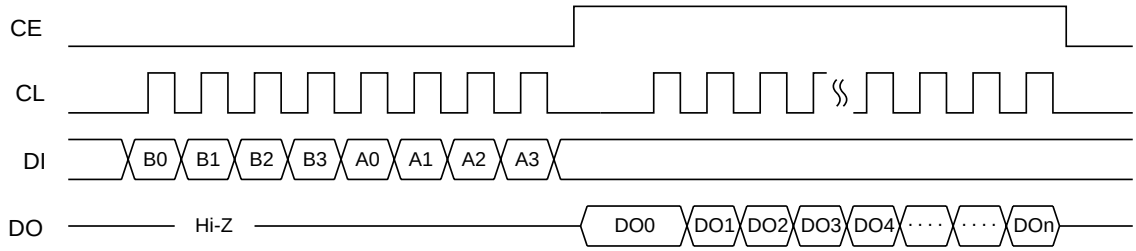


Figure 10.3. Output Timing Chart (Normal L Clock)

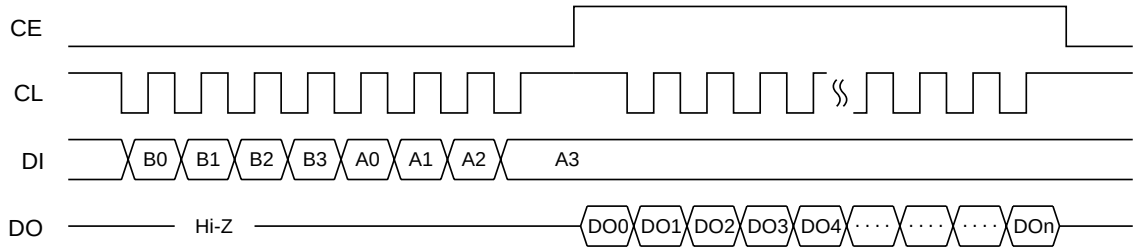


Figure 10.4. Output Timing Chart (Normal H Clock, DO0 Need Not Be Read with Port)

10.2 Write Data

10.2.1 Write Command List

- A list of the write commands is shown below.
- To write the commands shown in the following table, set the CCB address to 0xE8.

Add.	Setting Items	DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8
0	All system setting	TESTM	0	TXOPR	RXOPR	INTOPF	0	DOEN	SYSRST
1	Demodulation system setting	0	0	FSLIM1	FSLIM0	RXMON	AOSEL	VOSEL	UOSEL
2	Master clock	AMPOPR1	AMPOPR0	EXSYNC	PLLOPR	XMSEL1	XMSEL0	XINSEL	PLLSEL
3	R system output clock	XRLRCK1	XRLRCK0	XRBCK1	XRBCK0	XRSEL1	XRSEL0	PRSEL1	PRSEL0
4	S system output clock	XSLRCK1	XSLRCK0	XSBCK1	XSBCK0	PSLRCK1	PSLRCK0	PSBCK1	PSBCK0
5	Source switch	0	RDTMUT	RDTSTA	RDTSEL	0	RCKSEL	OCKSEL	SELMTD
6	Data input/output	RXOFF	ROSEL2	ROSEL1	ROSEL0	ULSEL	RISEL2	RISEL1	RISEL0
7	Output format setting	SLRCKP	SBCKP	RLRCKP	RBCKP	0	OFSEL2	OFSEL1	OFSEL0
8	$\overline{\text{INT}}$ source selection	EMPF	SLIPO	PCRNW	UNPCM	CSRNW	FSCHG	INDET	ERROR
9	RERR condition setting	ERWT1	ERWT0	FSERR	RESTA	XTWT1	XTWT0	REDER	RESEL
10	Modulation system setting	P13	P12	P11	P10	0	VMODE	VISEL	UISEL
11	Modulation data setting	0	0	TXMOD1	TXMOD0	TXMUT	TDTSEL	TWLRP	TXDFS
12	TEST	0	0	0	0	0	0	0	0
13	TEST	0	0	0	0	0	0	0	0
14	TEST	0	0	0	0	0	0	0	0
15	TEST	0	0	0	0	0	0	0	0

- The shaded parts in command area DI8 to DI15 are reserved bits. Input "0".
- Command addresses 0x12 to 0x15 are reserved for testing purposes. Writing to these addresses is prohibited.

10.2.2 Write command details

CCB address: 0xE8; Command address: 0; All system settings

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
0	0	0	0	0	0	CAU	CAL

DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8
TESTM	0	TXOPR	RXOPR	INTOPF	0	DOEN	SYSRST

SYSRST — System reset
0: Don't reset (initial value)
1: Reset circuits other than command registers

DOEN — DO output setting
0: Output (initial value)
1: Always high impedance state (read disabled)

INTOPF — $\overline{\text{INT}}$ pin output setting
0: Output "L" level during source occurrence (initial value)
1: Output "L" pulse during source occurrence

RXOPR — Demodulation function operation setting
0: Operate (initial value)
1: Stop

TXOPR — Modulation function operation setting
0: Stop (initial value)
1: Operate

TESTM — Test mode setting
0: Normal operation (initial value)
1: Enter test mode

- When reset through SYSRST or the demodulation function stop setting is performed, RBCK and SBCK output "L", and RLRCK and SLRCK output "H".

CCB address: 0xE8; Command address: 1; Demodulation function: System setting

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
0	0	0	1	0	0	CAU	CAL

DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8
0	0	FSLIM1	FSLIM0	RXMON	AOSEL	VOSEL	UOSEL

UOSEL EMPHA/UO pin setting
0: EMPHA emphasis output (initial value)
1: UO user data output

VOSEL $\overline{\text{AUDIO}}$/VO pin setting
0: $\overline{\text{AUDIO}}$ channel status bit 1 output (initial value)
1: VO validity flag output

AOSEL Output contents when $\overline{\text{AUDIO}}$ is set with $\overline{\text{AUDIO}}$/VO pin
0: Channel status bit 1 read (initial value)
1: Channel status bit 1, IEC61937, DTS-CD/LD detection flag output

RXMON Digital data input status monitoring function setting
0: Don't monitor data input status (initial setting)
1: Monitor data input status

FSLIM [1:0] Setting of sampling frequency reception range for RX input signal
00: No limit (initial value)
01: fs ≤ 96kHz
10: fs ≤ 48kHz
11: Reserved

CCB address: 0xE8; Command address: 2; Demodulation function: Master clock setting

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
0	0	1	0	0	0	CAU	CAL

DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8
AMPOPR1	AMPOPR0	EXSYNC	PLLOPR	XMSEL1	XMSEL0	XINSEL	PLLSEL

PLLSEL — PLL lock frequency setting
0: 512fs (fs ≤ 96kHz commend) (initial value)
1: 256fs

XINSEL — XIN input frequency setting
0: 12.288MHz (initial value)
1: 24.576MHz

XMSEL [1:0] — XMCK output frequency setting
00: 1/1 of XIN input frequency (initial value)
01: 1/2 of XIN input frequency
10: Reserved
11: Muted

PLLOPR — PLL (VCO) operation setting
0: Operate (initial value)
1: Stop

EXSYNC — PLL unused demodulation function (external synchronization function) setting
0: PLL usage normal operation (initial value)
1: PLL unused external synchronization operation (supply 256fs clock to TMCK)

AMPOPR [1:0] — Oscillation amplifier operation setting
00: Automatic stopping of oscillation amplifier during PLL lock (initial value)
01: Normal continuous operation
10: Reserved
11: Stop

- If the PLL is stopped with PLLOPR while the PLL is locked, the output clocks are all muted and this muted status continues even if the PLL becomes unlocked.
- If the permanent continuous operation setting is performed with AMPOPR0,1 while the PLL is locked, RERR goes to into error status once. However, the RERR status can be set to be maintained if a setting so that no error is output according to the PLL status even if the sampling frequency changes with FSERR is performed.
- When the oscillation amplifier automatic stop mode is set with AMPOPR0,1, if the input sampling frequency changes within the capture range of the PLL and no lock error occurs, sampling frequency calculation is not performed in the oscillation amplifier stop status, so that the input data sampling frequency and the fs calculation result may differ. However, if the channel status sampling frequency information is rewritten together with input data changes, this information is reflected to the error flag and fs calculation of the input data is performed. Since the oscillation amplifier permanent continuous operation setting is performed by permanent fs calculation, sampling frequency changes are always reflected to the error flag.

CCB address: 0xE8; Command address: 3; Demodulation function: R system output clock setting

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
0	0	1	1	0	0	CAU	CAL

DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8
XRLRCK1	XRLRCK0	XRBCK1	XRBCK0	XRSEL1	XRSEL0	PRSEL1	PRSEL0

PRSEL [1:0] RMCK output frequency setting during PLL lock
00: 1/2 of PLLSEL setting frequency (initial value)
01: 1/1 of PLLSEL setting frequency
10: 1/4 of PLLSEL setting frequency
11: Muted

XRSEL [1:0] RMCK output frequency setting during XIN source
00: 1/1 of XINSEL setting frequency (initial value)
01: 1/2 of XINSEL setting frequency
10: 1/4 of XINSEL setting frequency
11: Muted

XRBCK [1:0] RBCK output frequency setting during XIN source
00: 3.072MHz output (initial value)
01: 6.144MHz output
10: 12.288MHz output
11: Muted

XRLRCK [1:0] RLRCK output frequency setting during XIN source
00: 48kHz output (initial value)
01: 96kHz output
10: 192kHz output
11: Muted

- If the RMCK frequency is set lower than RBCK when the XIN source is used, 3.072MHz is output from RBCK.

CCB address: 0xE8; Command address: 4; Demodulation function: S system output clock setting

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
0	1	0	0	0	0	CAU	CAL

DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8
XSLRCK1	XSLRCK0	XSBCK1	XSBCK0	PSLRCK1	PSLRCK0	PSBCK1	PSBCK0

PSBCK [1:0] SBCK frequency setting during PLL lock
00: 64fs output (initial value)
01: 128fs output
10: 32fs output
11: Muted

PSLRCK [1:0] SLRCK frequency setting during PLL lock
00: fs output (initial value)
01: 2fs output
10: fs/2 output
11: Muted

XSBCK [1:0] SBCK frequency setting during XIN source
00: 3.072MHz output (initial value)
01: 6.144MHz output
10: 12.288MHz output
11: Muted

XSLRCK [1:0] SLRCK frequency setting during XIN source
00: 48kHz output (initial value)
01: 96kHz output
10: 192kHz output
11: Muted

CCB address: 0xE8; Command address: 5; Demodulation function: Clock source; RDA TA output setting

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
0	1	0	1	0	0	CAU	CAL

DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8
0	RDTMUT	RDTSTA	RDTSEL	0	RCKSEL	OCKSEL	SELMTD

SELMTD Output clock source switching method setting
0: Simultaneously switch R system and S system according to OCKSEL. (initial value)
1: Switch R system according to RCKSEL and fix S system to XIN.

OCKSEL Clock source setting when SELMTD = 0
0: Use XIN clock as source during PLL lock. (initial value)
1: Use XIN clock as source regardless of PLL status.

RCKSEL Clock source setting when SELMTD = 1
0: Use XIN clock as source during PLL lock. (initial value)
1: Use XIN clock as source regardless of PLL status.

RDTSEL RDATA output setting during PLL unlock
0: Output SDIN data during PLL unlock. (initial value)
1. Mute during PLL unlock.

RDTSTA RDATA output setting
0: According to RDTSEL (initial value)
1: Output SDIN input data regardless of PLL status.

RDTMUT RDATA mute setting
0: Output data selected with RDTSEL.
1: Muted

- When the oscillation amplifier is set to permanent continuous operation with AMPOPR0,1 or f changes are set not to be reflected to the error flag with FSERR, OCKSEL and RCKSEL can switch the clock source while maintaining the RERR status. However, if none of these settings is performed, RERR outputs an error once during switching.
- To input data to SDIN, select a clock synchronized with the SDIN input data.
- The XIN source can be switched to while maintaining the PLL locked status. However, since clock and data output switching can be set individually for each, it is recommended to select mute or SDIN data for the output data during XIN source switching.
- If the setting to automatically stop the oscillation amplifier as the PLL gets locked, XIN source switching from the PLL locked status is executed after the resonator oscillates stably. Moreover, output data switching at this time is done according to XIN source switching.

CCB address: 0xE8; Command address: 6; Demodulation function: Digital data input/output port setting

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
0	1	1	0	0	0	CAU	CAL

DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8
RXOFF	ROSEL2	ROSEL1	ROSEL0	ULSEL	RISEL2	RISEL1	RISEL0

RISEL [2:0] Data demodulation input pin setting
000: RX0 selection (initial value)
001: RX1 selection
010: RX2 selection
011: RX3 selection
100: RX4 selection (However, VI input is performed when VISEL is set.)
101: RX5 selection (However, UI input is performed when UISEL is set.)
110: RX6 selection
111: Modulation function output (TXO output data) selection

ULSEL Input pin setting via PLL unlock
0: Normal setting (initial value)
1: Input data switch setting via PLL unlock

ROSEL [2:0] RXOUT output data setting
000: RX0 input data (initial value)
001: RX1 input data
010: RX2 input data
011: RX3 input data
100: RX4 input data
101: RX5/VI input data
110: RX6/UI input data
111: Modulation function output (TXO output data) selection

RXOFF RXOUT output status setting
0: ROSEL0, ROSEL1, ROSEL2 selection data output (initial value)
1: "L" fixed output

- ULSEL can be set when the oscillation amplifier is set to permanent continuous operation with AMPOPR0,1. It does not operate normally when the oscillation amplifier is stopped.

CCB address; 0xE8; Command address: 7; Demodulation function: Output data format setting

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
0	1	1	1	0	0	CAU	CAL

DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8
SLRCKP	SBCKP	RLRCKP	RBCKP	0	OFSEL2	OFSEL1	OFSEL0

OFSEL [2:0] Audio data output format setting
000: I^2S data output (initial value)
001: MSB-first front-loading data output
010: 24 bit MSB-first back-loading data output (master mode only)
011: 20 bit MSB-first back-loading data output (master mode only)
100: 16 bit MSB-first back-loading data output (master mode only)
101: Reserved
110: Reserved
111: Reserved

RBCKP RBCK output polarity setting
0: Falling RDATA data change (initial value)
1: Rising RDATA data change

RLRCKP RLRCK output polarity setting
0: "L" period: L-channel data; "H" period: R-channel data (initial value)
1: "L" period: R-channel data; "H" period: L-channel data

SBCKP SBCK output polarity setting
0: Falling RDATA data change (initial value)
1: Falling RDATA data change

SLRCKP SLRCK output polarity setting
0: "L" period: L-channel data; "H" period: R-channel data (initial value)
1: "L" period: R-channel data; "H" period: L-channel data

- The data output format and RLRCK output polarity can be set independently. Set the RLRCH polarity according to each data output format.

CCB address: 0xE8; Command address: 8; Demodulation function: INT output contents setting

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
1	0	0	0	0	0	CAU	CAL

DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8
EMPF	SLIPO	PCRNW	UNPCM	CSRNW	FSCHG	INDET	ERROR

ERROR
RERR signal output setting
0: Don't output. (initial value)
1: Output RERR pin status change.

INDET
Input data detection output setting
0: Don't output. (initial value)
1: Output input data pin status change.

FSCHG
PLL lock frequency calculation result update flag output setting
0: Don't output. (initial value)
1: Output PLL lock frequency calculation result update flag.

CSRNW
First 48 channel status bits update flag output setting
0: Don't output. (initial value)
1: Output first 48 channel status bits update flag.

UNPCM
Non-PCM data detection change flag output setting
0: Don't output. (initial value)
1: Output $\overline{\text{AUDIO}}$ pin status change.

PCRNW
Burst preamble Pc update flag output setting
0: Don't output. (initial value)
1: Output burst preamble Pc update flag.

SLIPO
Slip signal output setting during slave operation
0: Don't output. (initial value)
1: Read data output twice and output data loss detection flag.

EMPF
Emphasis detection flag output setting
0: Don't output. (initial value)
1: Output emphasis detection flag.

- The channel status update flag compares the first 48 bits of data of the previous block with those of the current block and outputs a flag in case they are the same, considering update has been performed.
- The burst preamble Pc update flag also compares the 16 bits of data of the previous block with those of the current data, and if they match, outputs an update flag.

CCB address: 0xE8, Command address: 9; Demodulation function: RERR output setting

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
1	0	0	1	0	0	CAU	CAL

DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8
ERWT1	ERWT0	FSERR	RESTA	XTWT1	XTWT0	REDER	RESEL

RESEL — RERR output contents setting
0: PLL lock error or data error (initial value)
1: PLL lock error or data error or non-PCM data

REDER — 8 continuous times parity error flag output setting
0: Output during non-PCM data recognition. (initial value)
1: Output only during sub-frame for which error was generated.

XTWT [1:0] — Clock switch wait time setting after PLL unlock
00: Clock switching after approx. 200µs following oscillation amplifier start (initial value)
01: Clock switching after approx. 100µs following oscillation amplifier start
10: Clock switching after approx. 50µs following oscillation amplifier start
11: Clock switching after approx. 400µs following oscillation amplifier start

RESTA — RERR output condition setting
0: Output permanent PLL status (Output PLL status even during XIN source) (initial status)
1: Forcibly output error (Set "H" forcibly to RERR)

FSERR — Setting of error flag output condition through fs change
0: Reflect fs changes to error flag. (initial value)
1: Don't reflect fs changes to error flag.

ERWT [1:0] — RERR wait time setting after PLL lock
00: Error release preamble B after 48 counts. (initial value)
01: Error release preamble B after 24 counts.
10: Error release preamble B after 12 counts.
11: Error release preamble B after 6 counts.

- Non-PCM data is reflected to data defined with AOSEL. In other words, it becomes the same as detection data output to $\overline{\text{AUDIO}}$.
- Output data is muted if an error occurs due to non-PCM data for RESEL.
- The RESTA setting is not reflected to the data and clock output pins.
- For FSERR, the fs calculation result in the oscillation amplifier stopped status is not reflected. In this case, fs changes consist only of channel status fs information.
- ERWT0,1 is a setting to define the interval until RERR outputs error cancellation ("L") following PLL lock. Since the audio data following demodulation is output following RERR error cancellation, do not perform this setting if cutting off of the beginning of data is a problem.

CCB address: 0xE8; Command address: 10; Modulation function:
System setting, general-purpose I/O data input

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
1	0	1	0	0	0	CAU	CAL

DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8
PI3	PI2	PI1	PI0	0	VMODE	VISEL	UISEL

UISEL RX6/UI pin setting
0: RX6 demodulation function data input (initial value)
1: UI modulation function user data input

VISEL RX5/VI pin setting
0: RX5 demodulation function data input (initial value)
1: VI modulation function validity flag input

VMODE Modulation function V flag setting
0: Write 0. (initial value)
1: Write 1.

PI0 Data input during general-purpose I/O PIO0 output setting
0: Output L. (initial value)
1: Output H.

PI1 Data input during general-purpose I/O PIO1 output setting
0: Output L. (initial value)
1: Output H.

PI2 Data input during general-purpose I/O PIO2 output setting
0: Output L. (initial value)
1: Output H.

PI3 Data input during general-purpose I/O PIO3 output setting
0: Output L. (initial value)
1: Output H.

- If using general-purpose I/Os PIO0 to PIO3 as outputs, set PIOEN to "L".

CCB address: 0xE8; Command address: 11; Modulation function: Digital audio input/output setting

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
1	0	1	1	0	0	CAU	CAL

DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8
0	0	TXMOD1	TXMOD0	TXMUT	TDTSEL	TXLRP	TXDFS

TXDFS — TDATA input data format setting
0: I^2S data input (initial value)
1: MSB-first front-loading data input

TXLRP — TLRCK input clock polarity setting
0: "L" period: L-channel data; "H" period: R-channel data (initial value)
1: "L" period: R-channel data; "H" period: L-channel data

TDTSEL — Input data setting
0: TDATA input data (initial value)
1: SDIN input data

TXMUT — TXO output setting
0: Conversion data output (initial value)
1: "L" fixed output

TXMOD [1:0] — Mode setting
00: Normal operation (L-channel, R-channel stereo mode) (initial value)
01: L-channel continuous (time-division mode)
10: R-channel continuous (time-division mode)
11: reserved

10.2.3 Channel status data write

- For channel status data write with the modulation function, set the CCB address to 0xE9.
- DI0 to DI7 are not channel status bits. Always input a chip address to DI0 and DI1. Input "0" to DI2, DI3, and DI7 because they are reserved for the system. Select the channel status data write length with DI4 to DI6. Up to 48 bits can be set, in 8-bit units.
- After CE becomes "L", input data is written from preamble B.

Table 10.3. Relation between Input Data Length Setting Register and Data Length

DI6	DI5	DI4	Inputtable Data Range
0	0	0	Bit 0 to bit 7
0	0	1	Bit 0 to bit 15
0	1	0	Bit 0 to bit 23
0	1	1	Bit 0 to bit 31

DI6	DI5	DI4	Inputtable Data Range
1	0	0	Bit 0 to bit 39
1	0	1	Bit 0 to bit 47
1	1	0	Reserved
1	1	1	Reserved

Table 10.4. Input Setting --Modulation Function Channel Status Data Setting--

Register	Bit No.	Description
DI0	CAL	Lower chip address
DI1	CAU	Higher chip address
DI2	0	Reserved
DI3	0	
DI4	0	Data length setting
DI5	0	
DI6	0	
DI7	0	Reserved
DI8	Bit 0	Application
DI9	Bit 1	Control
DI10	Bit 2	
DI11	Bit 3	
DI12	Bit 4	
DI13	Bit 5	
DI14	Bit 6	Not defined
DI15	Bit 7	
DI16	Bit 8	Category code
DI17	Bit 9	
DI18	Bit 10	
DI19	Bit 11	
DI20	Bit 12	
DI21	Bit 13	
DI22	Bit 14	
DI23	Bit 15	
DI24	Bit 16	Source number
DI25	Bit 17	
DI26	Bit 18	
DI27	Bit 19	

Register	Bit No.	Description
DI28	Bit 20	Channel number
DI29	Bit 21	
DI30	Bit 22	
DI31	Bit 23	
DI32	Bit 24	Sampling frequency
DI33	Bit 25	
DI34	Bit 26	
DI35	Bit 27	
DI36	Bit 28	Clock accuracy
DI37	Bit 29	
DI38	Bit 30	Not defined
DI39	Bit 31	
DI40	Bit 32	Word length
DI41	Bit 33	
DI42	Bit 34	
DI43	Bit 35	
DI44	Bit 36	Not defined
DI45	Bit 37	
DI46	Bit 38	
DI47	Bit 39	
DI48	Bit 40	
DI49	Bit 41	
DI50	Bit 42	
DI51	Bit 43	
DI52	Bit 44	
DI53	Bit 45	
DI54	Bit 46	
DI55	Bit 47	

10.3 Read Data

10.3.1 Read command list

- The following items can be read.
  - Digital data input status monitor output
  - Interrupt data output
  - General-purpose I/O input data output
  - fs calculation result, fs counter data (8 bit) output
  - First 48 channel status bit output
  - Burst preamble Pc data output
- CCB address 0XEB and output registers DO16 to DO23 are for testing.

Read Register Name	0xEA	0xEB	0xEC	0xED
DO0	RXDET0	PO0	CS bit 0	Pc bit 0
DO1	RXDET1	PO1	CS bit 1	Pc bit 1
DO2	RXDET2	PO2	CS bit 2	Pc bit 2
DO3	RXDET3	PO3	CS bit 3	Pc bit 3
DO4	RXDET4	FSC0	CS bit 4	Pc bit 4
DO5	RXDET5	FSC1	CS bit 5	Pc bit 5
DO6	RXDET6	FSC2	CS bit 6	Pc bit 6
DO7	RXDET7	FSC3	CS bit 7	Pc bit 7
DO8	OERROR	FSDAT0	CS bit 8	Pc bit 8
DO9	OINDET	FSDAT1	CS bit 9	Pc bit 9
DO10	OFSCHG	FSDAT2	CS bit 10	Pc bit 10
DO11	OCSRNW	FSDAT3	CS bit 11	Pc bit 11
DO12	OUNPCM	FSDAT4	CS bit 12	Pc bit 12
DO13	OPCRNW	FSDAT5	CS bit 13	Pc bit 13
DO14	OSLIPO	FSDAT6	CS bit 14	Pc bit 14
DO15	OEMPF	FSDAT7	CS bit 15	Pc bit 15
DO16	CSBITI	TEST0	CS bit 16	–
DO17	IEC1937	TEST1	CS bit 17	–
DO18	DTS51	TEST2	CS bit 18	–
DO19	DTSES	TEST3	CS bit 19	–
DO20	F0512	TSET4	CS bit 20	–
DO21	F1024	TEST5	CS bit 21	–
DO22	F2048	TEST6	CS bit 22	–
DO23	F4096	TEST7	CS bit 23	–
DO24	–	–	CS bit 24	–
...	–	–	...	–
DO46	–	–	CS bit 46	–
DO47	–	–	CS bit 47	–

10.3.2 Read register 1 (input detection, interrupt flag, IEC61937 flag, DTS flag)

CCB address: 0XEA, read register output contents

DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0
RXDET7	RXDET6	RXDET5	RXDET4	RXDET3	RXDET2	RXDET1	RXDET0

RXDET0 RX0 input detection
0: No input data to RX0
1: Input data to RX0

RXDET1 RX1 input detection
0: No input data to RX1
1: Input data to RX1

RXDET2 RX2 input detection
0: No input data to RX2
1: Input data to RX2

RXDET3 RX3 input detection
0: No input data to RX3
1: Input data to RX3

RXDET4 RX4 input detection
0: No input data to RX4
1: Input data to RX4

RXDET5 RX5 input detection
0: No input data to RX5
1: Input data to RX5

RXDET6 RX6 input detection
0: No input data to RX6
1: Input data to RX6

RXDET7 Modulation function output TXO data detection
0: No data to modulation function output TXO
1: Data to modulation function output TXO

- For RXDET0 to RXDET7 read, RXMON must be set to "H" beforehand.

CCB address; 0xEA; Read register output contents

DO15	DO14	DO13	DO12	DO11	DO10	DO9	DO8
DEMPF	OSLIPO	OPCRNW	OUNPCM	OCSRNW	OFSCHG	OINDET	OERROR

OERROR — RERR output (Output status during read)
0: No transfer error in PLL locked status
1: Transfer error in PLL unlocked status

OINDET — Data input pin status change (Clear following read)
0: No change in data input pin status
1: Change in data input pin status

OFSCHG — Input fs calculation update result (clear following read)
0: No input fs calculation update
1: Input fs calculation update

OCSRNW — First 48 bit channel status update result (Clear following read)
0: No update
1: Update

OUNPCM — $\overline{\text{AUDIO}}$ output (Output of status during read)
0: Non-PCM signal not detected
1: Non-PCM signal detected

OPCRNW — Burst preamble Pc update result (Clear following read)
0: No update
1: Update

OSLIPO — Read data twice and detect data loss during slave operation (Clear following read)
0: No detection
1: Two reads, lost data detected

OEMPF — Channel status emphasis detection (Output status during read)
0: No pre-emphasis
1: 50/15 μs pre-emphasis

- The status of RERR and $\overline{\text{AUDIO}}$ is read according to RESEL and AOSEL regardless of the $\overline{\text{INT}}$ output setting, from OERROR and OUNPCM.

CCB address: 0xEA; Read register output contents

DO23	DO22	DO21	DO20	DO19	DO18	DO17	DO16
F4096	F2048	F1024	F0512	DTSES	DTS51	IEC1937	CSBIT1

CSBIT1 Channel status bit 1 detection
0: PCM
1: Non-PCM

IEC1937 IEC61937 burst preamble detection
0: Pa, Pb not detected
1: Pa, Pb detected

DTS51 DTS-CD/LD 5.1 channel sync signal detection
0: DTS-CD-LD sync signal not detected
1: DTS-CD-LD sync signal detected

DTSES DTS ES-CD/LD 6.1 channel sync signal detection
0: DTS ES-CD/LD sync signal not detected
1: DTS ES-CD/LD sync signal detected

F0512 DTS-CD/LD IEC60958 frame interval
0: Sync signal not 512 or 1024 frame interval
1: Sync signal is 512 or 1024 frame interval

F1024 DTS-CD/LD IEC60958 frame interval
0: Sync signal not 1024 or 2048 frame interval
1: Sync signal is 1024 or 2048 frame interval

F2048 DTS-CD/LD IEC60958 frame interval
0: Sync signal not 2048 or 4096 frame interval
1: Sync signal is 2048 or 4096 frame interval

F4096 DTS-CD/LD IEC60958 frame interval
0: Sync signal not 4096 frame interval
1: Sync signal is 4096 frame interval

10.3.3 Read register 2 (General-purpose I/O input contents, fs calculation result, fs counter data)

CCB address: 0xEB, read register output contents

DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0
FSC3	FSC2	FSC1	FSC0	PO3	PO2	PO1	PO0

PO0 Read data output contents during general-purpose I/O PO0 input setting
0: PIO0 input = "L"
1: PIO0 input = "H"

PO1 Read data output contents during general-purpose I/O PIO1 input setting
0: PIO1 input = "L"
1: PIO1 input = "H"

PO2 Read data output contents during general-purpose I/O PIO2 input setting
0: PIO2 input = "L"
1: PIO2 input = "H"

PO3 Read data output contents during general-purpose I/O PIO3 input setting
0: PIO3 input = "L"
1: PIO3 input = "H"

FSC [3:0] Input data fs calculation result
"xxxx": See code table.

Table 10.5. Input fs Calculation Result Code Table (T_a = 25°C, AVDD = DVDD = 3.3 V)

FSC3	FSC2	FSC1	FSC0	Target Frequency	Calculation Range (Design Value)
0	0	0	0	Out of range	–
0	0	0	1	–	–
0	0	1	0	–	–
0	0	1	1	–	–
0	1	0	0	16kHz	15.4k to 16.6kHz
0	1	0	1	22.05kHz	21.2k to 22.9kHz
0	1	1	0	24kHz	23.1k to 24.9kHz
0	1	1	1	32kHz	30.8k to 33.3kHz
1	0	0	0	44.1kHz	42.4k to 45.8kHz
1	0	0	1	48kHz	46.2k to 49.9kHz
1	0	1	0	64kHz	615k to 66.7kHz
1	0	1	1	88.2kHz	85.4k to 91.7kHz
1	1	0	0	96kHz	93.1k to 100.7kHz
1	1	0	1	128kHz	122.9k to 1335kHz
1	1	1	0	176.4kHz	170.7k to 180.7kHz
1	1	1	1	192kHz	186.2k to 198.1kHz

CCB address: 0xEB; Read register output contents

DO15	DO14	DO13	DO12	DO11	DO10	DO9	DO8
FSDAT7	FSDAT6	FSDAT5	FSDAT4	FSDAT3	FSDAT2	FSDAT1	FSDAT0

FSDAT [7:0] fs counter data output

- FSDAT [7:0] is the fs calculation counter value. The data length is 8 bits, FSDAT0 is LSB, and FSDAT7 is MSB.
- The relation between the count value and fs is expressed by the following equation.

  fs = 6144/FSDAT (kHz)
- fs calculation is performed using a 6.144MHz clock, so the calculation accuracy is determined by this clock.
- The calculation counter value is 8 bit output, so the fs that can be calculated is higher than 24kHz.

10.3.4 Read register 3 (read of first 48 channel status bits)

- The first 48 channel status bits can be read with the demodulation function.
- The read channel status data is output LSB first.
- For read, set the CCB address to 0xEC.
- The channel status data cannot be updated after the CCB address is set.
- The relation between the read registers and the channel status data is shown below.

Register	Bit No.	Contents
DO0	Bit 0	Application
DO1	Bit 1	Control
DO2	Bit 2	
DO3	Bit 3	
DO4	Bit 4	
DO5	Bit 5	
DO6	Bit 6	Not defined
DO7	Bit 7	
DO8	Bit 8	Category code
DO9	Bit 9	
DO10	Bit 10	
DO11	Bit 11	
DO12	Bit 12	
DO13	Bit 13	
DO14	Bit 14	
DO15	Bit 15	
DO16	Bit 16	Source number
DO17	Bit 17	
DO18	Bit 18	
DO19	Bit 19	
DO20	Bit 20	Channel number
DO21	Bit 21	
DO22	Bit 22	
DO23	Bit 23	

Register	Bit No.	Contents
DO24	Bit 24	Sampling frequency
DO25	Bit 25	
DO26	Bit 26	
DO27	Bit 27	
DO28	Bit 28	Clock accuracy
DO29	Bit 29	
DO30	Bit 30	Not defined
DO31	Bit 31	
DO32	Bit 32	Word length
DO33	Bit 33	
DO34	Bit 34	
DO35	Bit 35	
DO36	Bit 36	Not defined
DO37	Bit 37	
DO38	Bit 38	
DO39	Bit 39	
DO40	Bit 40	
DO41	Bit 41	
DO42	Bit 42	
DO43	Bit 43	
DO44	Bit 44	
DO45	Bit 45	
DO46	Bit 46	
DO47	Bit 47	

10.3.5 Read register 4 (burst preamble Pc data)

- The burst preamble Pc data can be read with the demodulation function.
- The 16 bits of burst preamble Pc data are output LSB first.
- For read, set the CCB address to OxED.
- The relation between the read register and burst preamble Pc data is shown below.

Register	Bit No.	Contents
DO0	Bit 0	Data type
DO1	Bit 1	
DO2	Bit 2	
DO3	Bit 3	
DO4	Bit 4	
DO5	Bit 5	Reserved
DO6	Bit 6	
DO7	Bit 7	Error
DO8	Bit 8	Data type dependent information
DO9	Bit 9	
DO10	Bit 10	
DO11	Bit 11	
DO12	Bit 12	
DO13	Bit 13	Bit stream Nnumber
DO14	Bit 14	
DO15	Bit 15	

10.4 Burst Preamble Pc Field

- The burst preamble Pc field is shown below.
- For the latest information, check the standards issued by each licensor.

Table 10.6. Burst Preamble Pc Field

Register	Value	Contents
DO4 to 0	0	NULL data
	1	Dolby AC-3 data
	2	Reserved
	3	Pause
	4	MPEG-1, layer 1 data
	5	MPEG-1, layer 2, 3 data, or non-extended MPEG-2
	6	Extended MPEG-2 data
	7	Reserved
	8	MPEG-2, layer 1, low sampling rate
	9	MPEG-2, layer 2, 3, low sampling rate
	10	Reserved
	11	DTS type1
	12	DTS type2
	13	DTS type3
	14	ATRAC
	15	ATRACK2/3
	16 to 26	Reserved
	27	Reserved (MPEG-4, AAC data)
	28	MPEG-2, AAC data
	29 to 31	Reserved
DO6, 5	0	Reserved (fixed to "0")
DO7	0	Error flag indicating effective burst payload
	1	Error flag indicating burst payload error
DO12 to 8		Data type dependent information
DO15 to 13	0	Bit stream No. (fixed to "0")

11 Application Example

11.1 Basic Connection Diagram

- Connect a decoupling capacitance (0.1 μF) as close as possible to the power supply pin. Use a ceramic capacitor with high-frequency characteristics for the capacitance.
- Use a capacitor with a low temperature coefficient for the PLL loop filter.

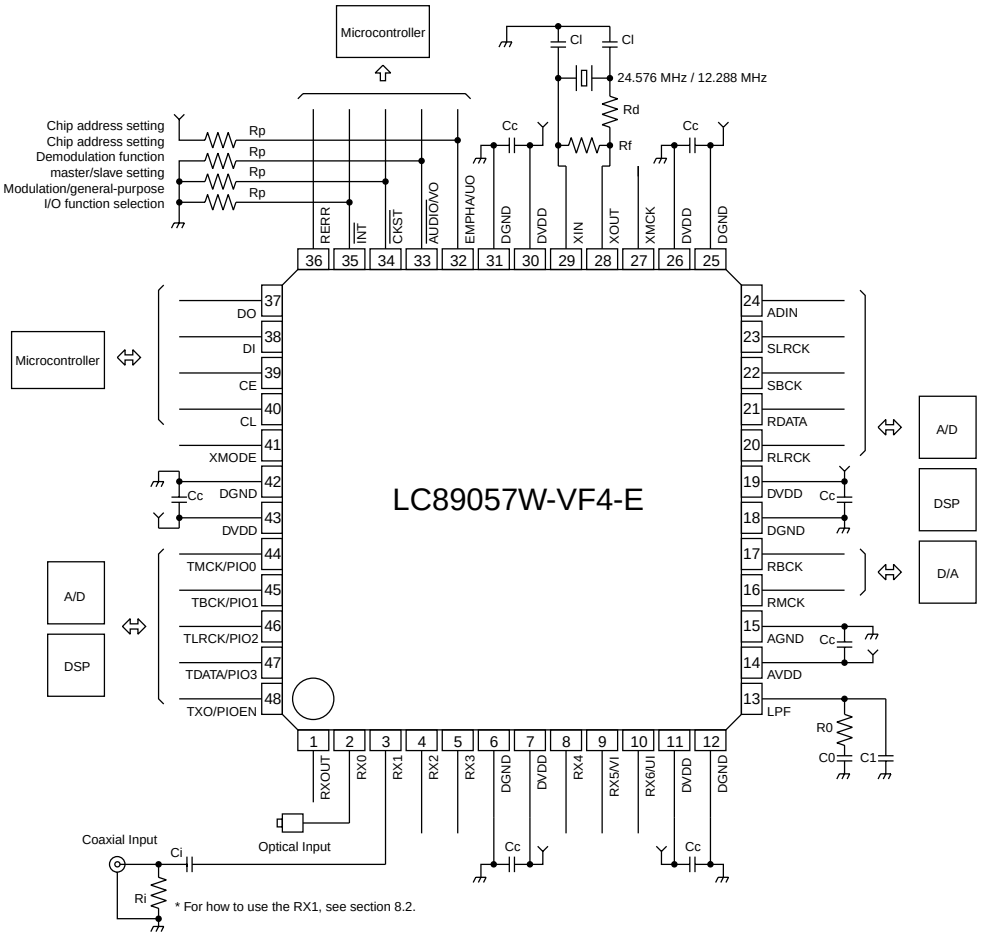


Table 11.1. Recommended Circuit Constants (**: See Section 8.1.1)

Element Symbol	Recommended Constant	Application	Remark
Cc	0.1 μF	Power supply decoupling	Ceramic capacitor
Rp	10 kΩ	Function setting pull-down/pull-up	
C1	1 pF to 33 pF	Crystal resonator load	NP0 characteristics ceramic capacitor
Rf	1 MΩ	Oscillation amplifier feedback	
Rd	220 Ω	Oscillation amplifier current limit	
Ci	01 μF	Coaxial input DC cut	Ceramic capacitor
Ri	75 Ω	Coaxial input termination	
C0	**	PLL loop filter	
C1	**	PLL loop filter	
R0	**	PLL loop filter	