

# LH5164A/AH

CMOS 64K (8K × 8) Static RAM

## FEATURES

- 8,192 × 8 bit organization
- Access times: 80/100 ns (MAX.)
- Low-power consumption:
  - Operating:
    - 303 mW (MAX.) LH5164A/D/N @ 80 ns
    - 248 mW (MAX.) LH5164A/D/N/T @ 100 ns
    - 275 mW (MAX.) LH5164AH/HD/HN/HT @ 100 ns
  - Standby:
    - LH5164A/D/N/T: 5.5 μW (MAX.)
    - LH5164AH/HD/HN/HT:
      - T<sub>A</sub> ≤ 85°C: 16.5 μW (MAX.)
      - T<sub>A</sub> ≤ 70°C: 5.5 μW (MAX.)

- Fully-static operation
- Three-state outputs
- Single +5 V power supply
- TTL compatible I/O
- Wide temperature range available
  - LH5164A: -10 to +70°C
  - LH5164AH: -40 to +85°C
- Packages:
  - 28-pin, 600-mil DIP
  - 28-pin, 300-mil SK-DIP
  - 28-pin, 450-mil SOP
  - 28-pin, 8 × 13 mm<sup>2</sup> TSOP (Type I)

## DESCRIPTION

The LH5164A/AH are static RAMs organized as 8,192 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

The LH5164AH is designed for wide temperature range from -40 to +85°C.

## PIN CONNECTIONS

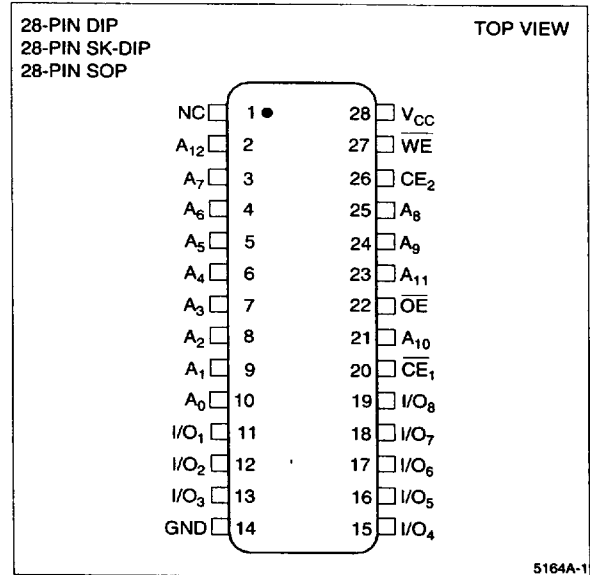


Figure 1. Pin Connections for DIP, SK-DIP, and SOP Packages

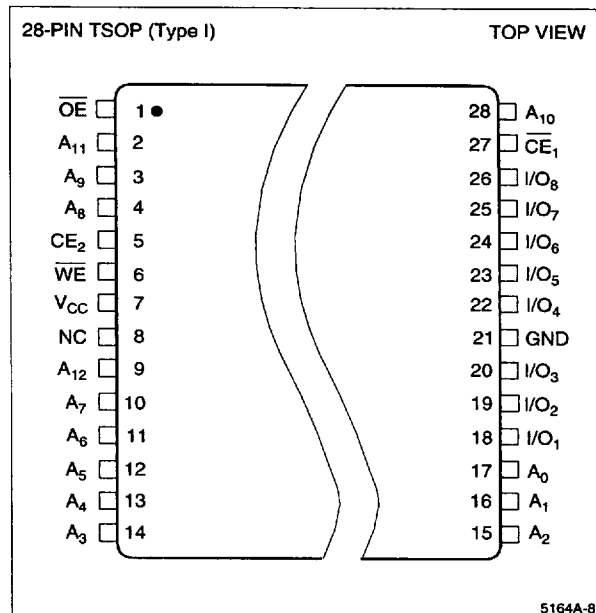


Figure 2. Pin Connections for TSOP Package

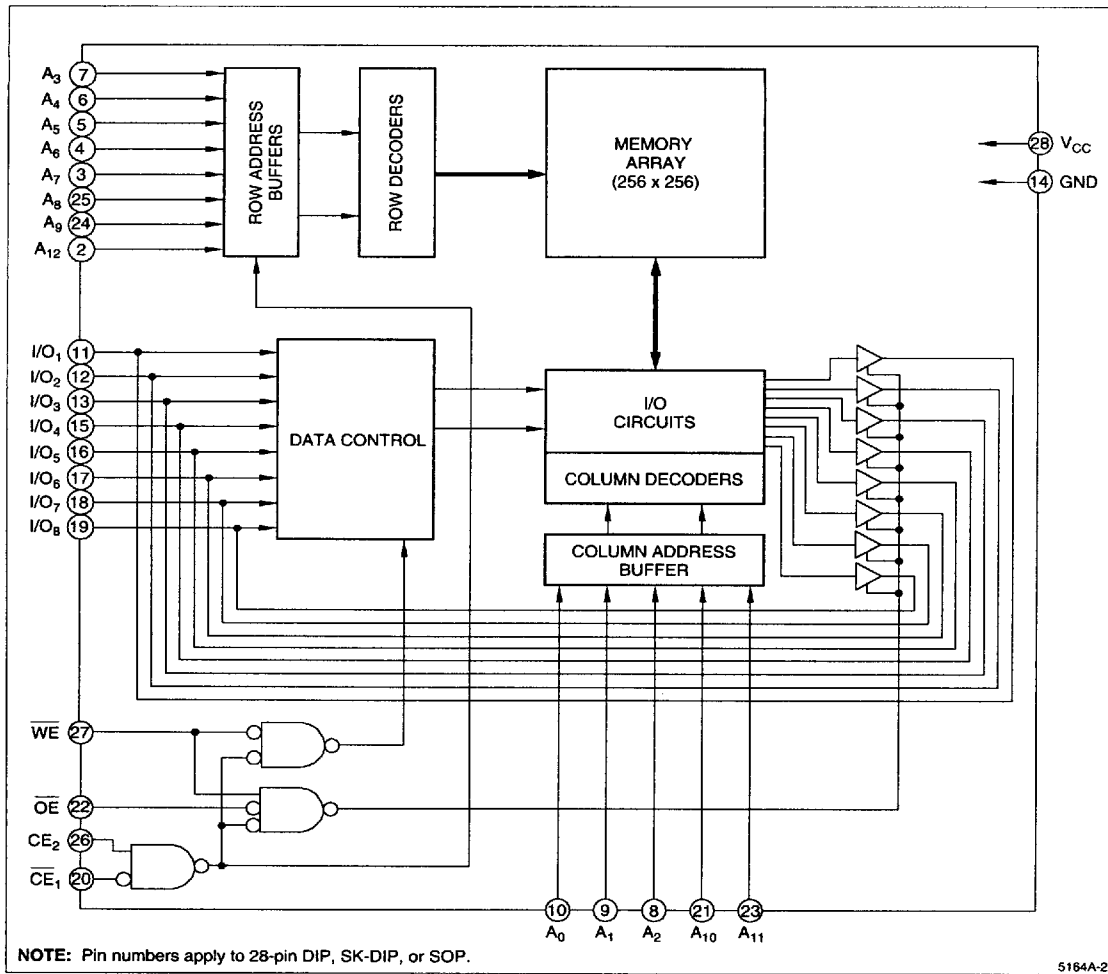


Figure 3. LH5164A/AH Block Diagram

**PIN DESCRIPTION**

SIGNAL	PIN NAME	SIGNAL	PIN NAME
A <sub>0</sub> - A <sub>12</sub>	Address inputs	I/O <sub>1</sub> - I/O <sub>8</sub>	Data inputs and outputs
CE <sub>1</sub> - CE <sub>2</sub>	Chip Enable input	V <sub>CC</sub>	Power supply
WE	Write Enable input	GND	Ground
OE	Output Enable input	NC	No connection

**TRUTH TABLE**

CE <sub>1</sub>	CE <sub>2</sub>	WE	OE	MODE	I/O <sub>1</sub> - I/O <sub>8</sub>	SUPPLY CURRENT	NOTE
H	X	X	X	Deselect	High-Z	Standby (I <sub>SB</sub> )	1
X	L	X	X	Deselect	High-Z	Standby (I <sub>SB</sub> )	1
L	H	L	X	Write	D <sub>IN</sub>	Operating (I <sub>CC</sub> )	1
L	H	H	L	Read	D <sub>OUT</sub>	Operating (I <sub>CC</sub> )	
L	H	H	H	Output disable	High-Z	Operating (I <sub>CC</sub> )	

NOTE:  
1. X = H or L

## ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	80 ns		UNIT	NOTE
		RATING	RATING		
Supply voltage	V <sub>CC</sub>	-0.3 to +7.0	-0.3 to +7.0	V	1
Input voltage	V <sub>IN</sub>	-0.3 to V <sub>CC</sub> + 0.3	-0.3 to V <sub>CC</sub> + 0.3	V	1, 2
Operating temperature	T <sub>opr</sub>	-10 to +70	-10 to +70	°C	3
Storage temperature	T <sub>stg</sub>	-55 to +150	-55 to +150	°C	4

## NOTES:

- The maximum applicable voltage on any pin with respect to GND.
- V<sub>IN</sub> (MIN.) = -3.0 V for pulse width ≤ 50 ns.
- LH5164A/AD/AN/AT
- LH5164AH/AHD/AHN/AHT

RECOMMENDED OPERATING CONDITIONS <sup>1</sup>

PARAMETER	SYMBOL	80 ns			100 ns			UNIT	NOTE
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
Supply voltage	V <sub>CC</sub>	4.5	5.0	5.5	4.5	5.0	5.5	V	
Input voltage	V <sub>IH</sub>	2.2		V <sub>CC</sub> + 0.3	2.2		V <sub>CC</sub> + 0.3	V	
	V <sub>IL</sub>	-0.3		0.8	-0.3		0.8	V	2

## NOTES:

- T<sub>A</sub> = -10 to +70°C (LH5164A/AD/AN/AT), T<sub>A</sub> = -40 to +85°C (LH5164AH/AHD/AHN/AHT).
- V<sub>IN</sub> (MIN.) = -3.0 V for pulse width ≤ 50 ns.

DC CHARACTERISTICS <sup>1</sup> (V<sub>CC</sub> = 5 V ± 10%)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE	
Input leakage current	I <sub>I</sub>	V <sub>IN</sub> = 0 to V <sub>CC</sub>	-1.0	1.0	μA		
Output leakage current	I <sub>LO</sub>	CE <sub>1</sub> = V <sub>IH</sub> or CE <sub>2</sub> = V <sub>IL</sub> or OE = V <sub>IH</sub> or WE = V <sub>IL</sub> V <sub>IO</sub> = 0 to V <sub>CC</sub>	-1.0	1.0	μA		
		CE <sub>1</sub> = V <sub>IL</sub> , V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> CE <sub>2</sub> = V <sub>IH</sub> , Outputs open	t <sub>CYCLE</sub> = 80 ns		55	mA	
Operating current	I <sub>CC</sub>	CE <sub>1</sub> = V <sub>IL</sub> , V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> CE <sub>2</sub> = V <sub>IH</sub> , Outputs open	t <sub>CYCLE</sub> = 100 ns	45		2	
		CE <sub>1</sub> = V <sub>IL</sub> , V <sub>IN</sub> = 0.2 V or V <sub>CC</sub> - 0.2 V CE <sub>2</sub> = V <sub>IH</sub> , Outputs open	t <sub>CYCLE</sub> = 1.0 μs	50		3	
		CE <sub>1</sub> = V <sub>IH</sub> or CE <sub>2</sub> = V <sub>IL</sub>		10		mA	
Standby current	I <sub>SB1</sub>	CE <sub>2</sub> ≤ 0.2 V or CE <sub>1</sub> ≥ V <sub>CC</sub> - 0.2 V	T <sub>A</sub> ≤ 70°C	5		mA	
			T <sub>A</sub> ≤ 85°C	1.0		μA	2, 3, 4
Output voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2.1 mA		3.0		μA	3, 4
	V <sub>OH</sub>	I <sub>OH</sub> = -1 mA	2.4	0.4		V	

## NOTES:

- T<sub>A</sub> = -10 to 70°C (LH5164A/AD/AN/AT), T<sub>A</sub> = -40 to +85°C (LH5164AH/AHD/AHN/AHT)
- LH5164A/AD/AN/AT
- LH5164AH/AHD/AHN/AHT
- CE<sub>2</sub> should be ≥ V<sub>CC</sub> - 0.2 V or ≤ 0.2 V when CE<sub>1</sub> ≥ V<sub>CC</sub> - 0.2 V

**AC CHARACTERISTICS**<sup>1</sup>**(1) READ CYCLE ( $V_{CC} = 5\text{ V} \pm 10\%$ )**

PARAMETER	SYMBOL	80 ns		100 ns		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
Read cycle time	$t_{RC}$	80		100		ns	
Address access time	$t_{AA}$		80		100	ns	
Chip enable access time	( $CE_1$ ) $t_{ACE1}$		80		100	ns	
	( $CE_2$ ) $t_{ACE2}$		80		100	ns	
Output enable access time	$t_{OE}$		40		40	ns	
Output hold time	$t_{OH}$	10		10		ns	
Chip enable to output in Low-Z	( $CE_1$ ) $t_{LZ1}$	10		10		ns	1
	( $CE_2$ ) $t_{LZ2}$	10		10		ns	1
Output enable to output in Low-Z	$t_{OLZ}$	5		5		ns	1
Chip enable to output in High-Z	( $CE_1$ ) $t_{HZ1}$	0	30	0	30	ns	1
	( $CE_2$ ) $t_{HZ2}$	0	30	0	30	ns	1
Output disable to output in High-Z	$t_{OHZ}$	0	20	0	20	ns	1

**(2) WRITE CYCLE ( $V_{CC} = 5\text{ V} \pm 10\%$ )**

PARAMETER	SYMBOL	80 ns		100 ns		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
Write cycle time	$t_{WC}$	80		100		ns	
Chip enable to end of write	$t_{CW}$	70		80		ns	
Address valid to end of write	$t_{AW}$	70		80		ns	
Address setup time	$t_{AS}$	0		0		ns	
Write pulse width	$t_{WP}$	60		60		ns	
Write recovery time	$t_{WR}$	0		0		ns	
Data valid to end of write	$t_{DW}$	40		40		ns	
Data hold time	$t_{DH}$	0		0		ns	
Output active from end of write	$t_{OW}$	10		10		ns	2
WE to output in High-Z	$t_{WZ}$	0	30	0	30	ns	2
OE to output in High-Z	$t_{OHZ}$	0	20	0	20	ns	2

**NOTES:**

- $T_A = -10$  to  $+70^\circ\text{C}$  (LH5164A/AD/AN/AT),  $T_A = -40$  to  $+85^\circ\text{C}$  (LH5164AH/AHD/AHN/AHT)
- Active output to high-impedance and high-impedance to output active tests specified for a  $\pm 200$  mV transition from steady state levels into the test load.

**AC TEST CONDITIONS**

PARAMETER	MODE	NOTE
Input voltage amplitude	0.6 to 2.4 V	
Input rise/fall time	10 ns	
Timing reference level	1.5 V	
Output load conditions	1TTL + $C_L$ (100 pF)	1

**NOTE:**

- Includes scope and jig capacitance.

**CAPACITANCE <sup>1</sup> (T<sub>A</sub> = 25°C, f = 1 MHz)**

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C <sub>IN</sub>	V <sub>IN</sub> = 0 V			7	pF
Input/output capacitance	C <sub>I/O</sub>	V <sub>I/O</sub> = 0 V			10	pF

**NOTE:**

1. This parameter is sampled and not production tested.

**DATA RETENTION CHARACTERISTICS <sup>1</sup>**

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Data retention voltage	V <sub>CCDR</sub>	CE <sub>2</sub> ≤ 0.2 V or CE <sub>1</sub> ≥ V <sub>CCDR</sub> - 0.2 V	2.0	5.5	V	2
		V <sub>CCDR</sub> = 3 V, CE <sub>2</sub> ≤ 0.2 V or CE <sub>1</sub> ≥ V <sub>CCDR</sub> - 0.2 V		0.2	μA	2, 3
				0.4	μA	2, 3
Data retention current	I <sub>CCDR</sub>			0.6	μA	2, 3
				0.2	μA	2, 4
				0.6	μA	2, 4
Chip disable to data retention	t <sub>CDR</sub>		0		ns	
Recovery time	t <sub>R</sub>		t <sub>RC</sub>		ns	5

**NOTES:**

- T<sub>A</sub> = -10 to +70°C (LH5164A/AD/AN/AT), T<sub>A</sub> = -40 to +85°C (LH5164AH/AHD/AHN/AHT)
- CE<sub>2</sub> should be ≥ V<sub>CCDR</sub> - 0.2 V or ≤ 0.2 V when CE<sub>1</sub> ≥ V<sub>CCDR</sub> - 0.2 V
- LH5164A/AD/AN/AT
- LH5164AH/AHD/AHN/AHT
- t<sub>RC</sub> = Read cycle time

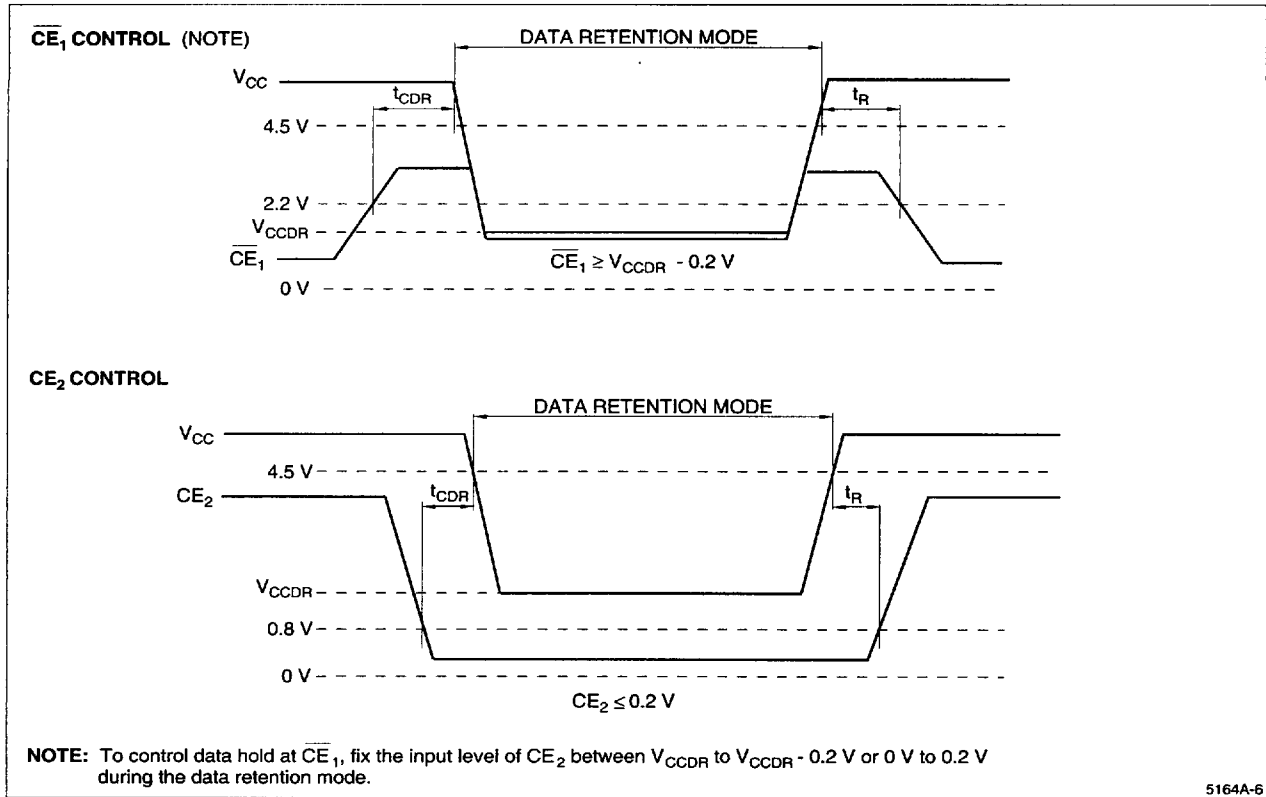


Figure 4. Low Voltage Data Retention

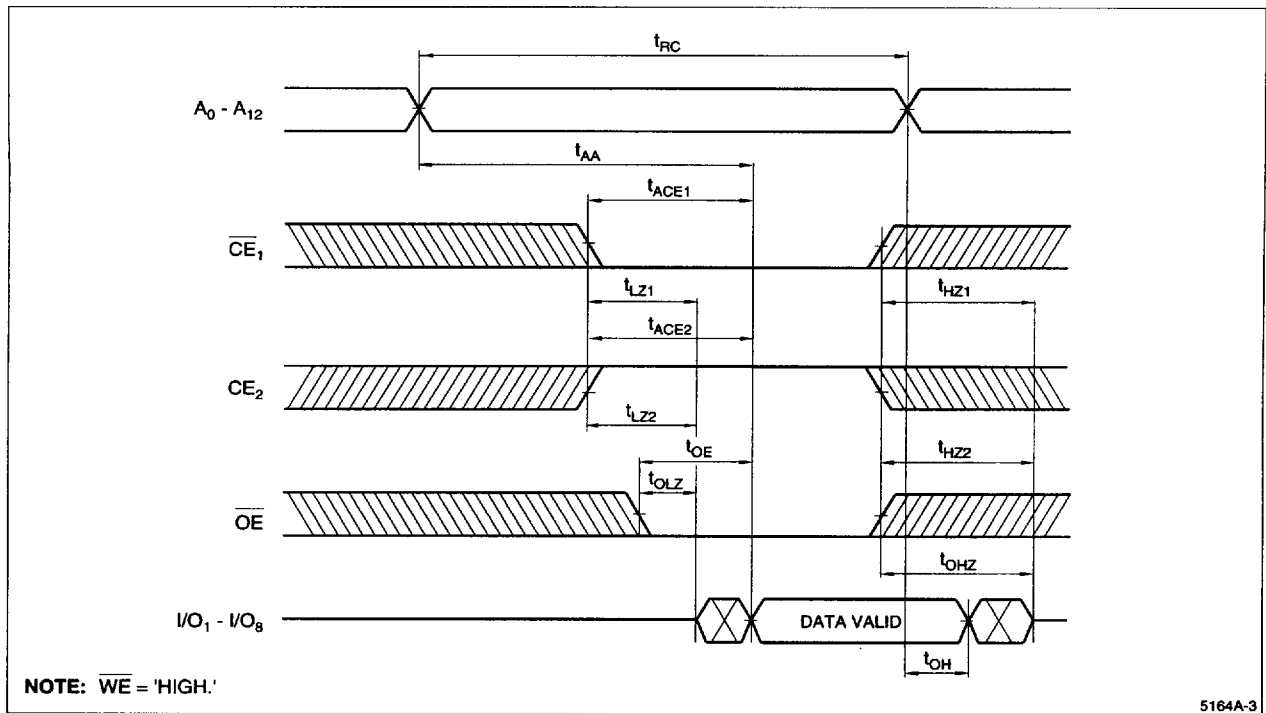
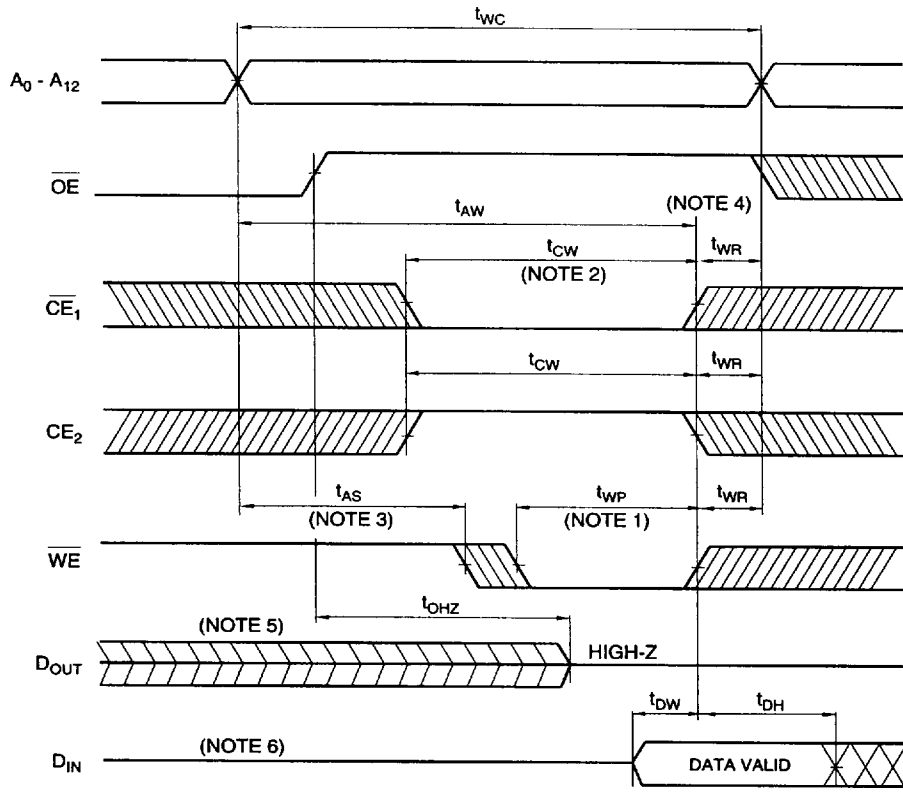


Figure 5. Read Cycle



**NOTES:**

1. The writing occurs during an overlapping period of  $\overline{CE}_1 = \text{'LOW'}$ ,  $CE_2 = \text{'HIGH'}$ , and  $\overline{WE} = \text{'LOW'}$  ( $t_{WP}$ ).
2.  $t_{CW}$  is defined as the time from the last occurring transition, either  $\overline{CE}_1$  LOW transition or  $CE_2$  HIGH transition, to the time when the writing is finished.
3.  $t_{AS}$  is defined as the time from address change to writing start.
4.  $t_{WR}$  is defined as the time from writing finish to address change.
5. If  $\overline{CE}_1$  LOW transition or  $CE_2$  HIGH transition occurs at the same time or after  $\overline{WE}$  LOW transition, the outputs will remain high-impedance.
6. While I/O pins are in the output state, input signals with the opposite logic level must not be applied.

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**Figure 6. Write Cycle 1**

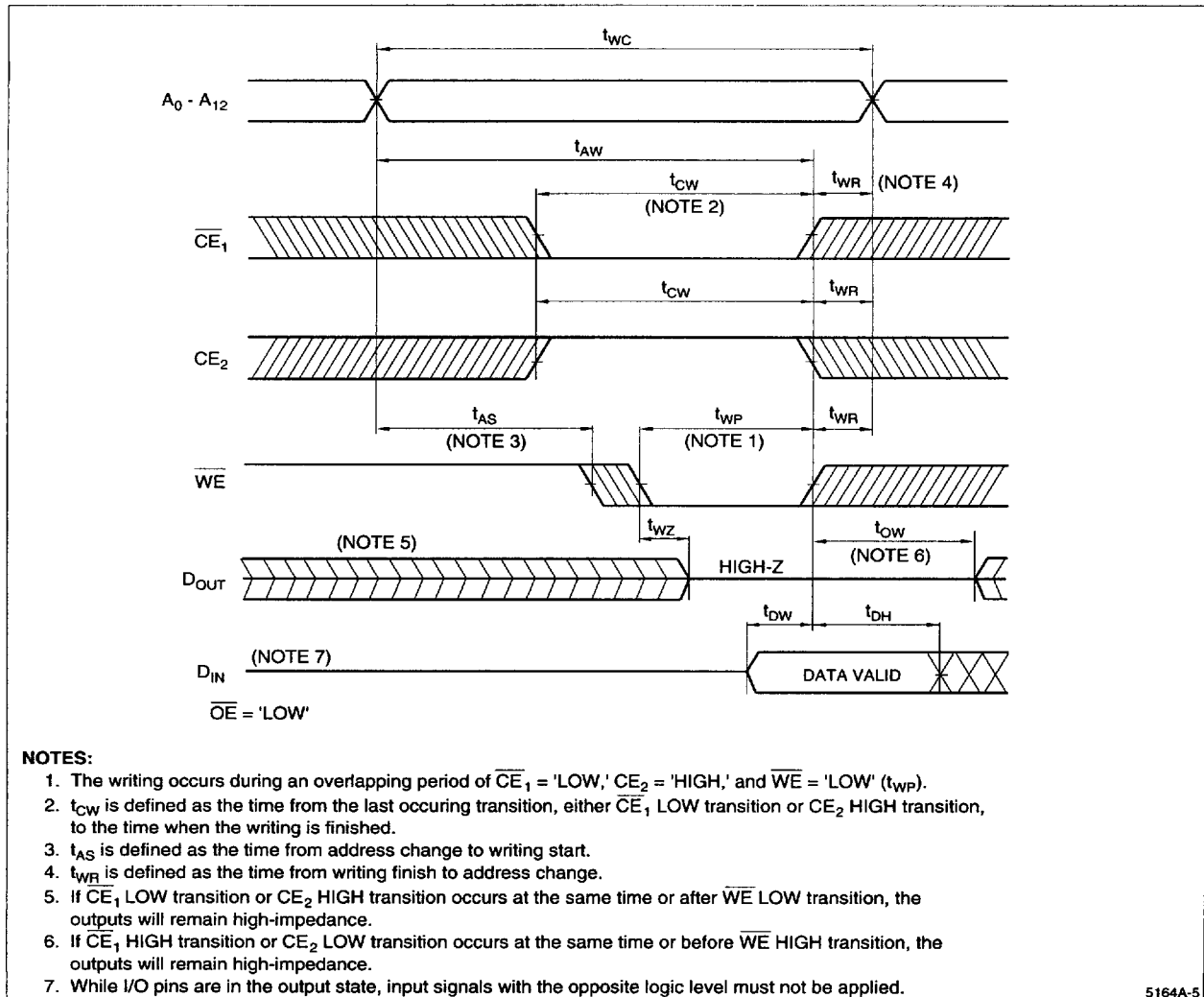
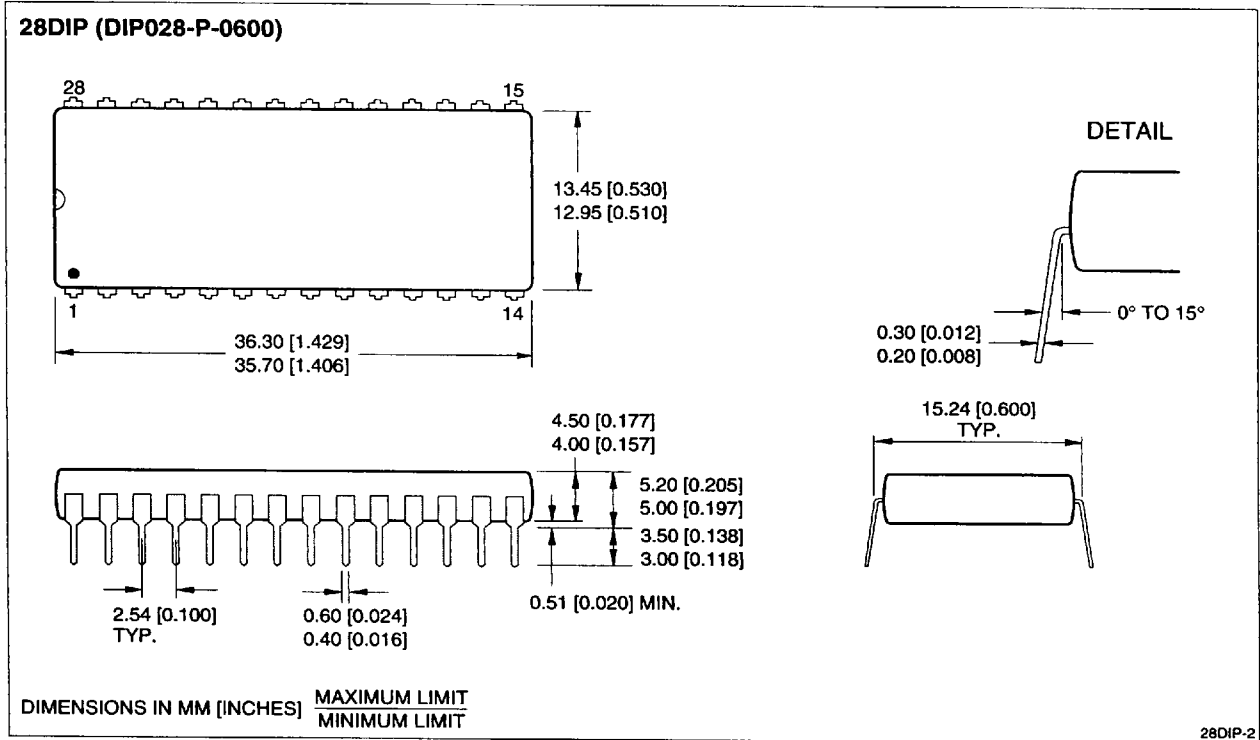
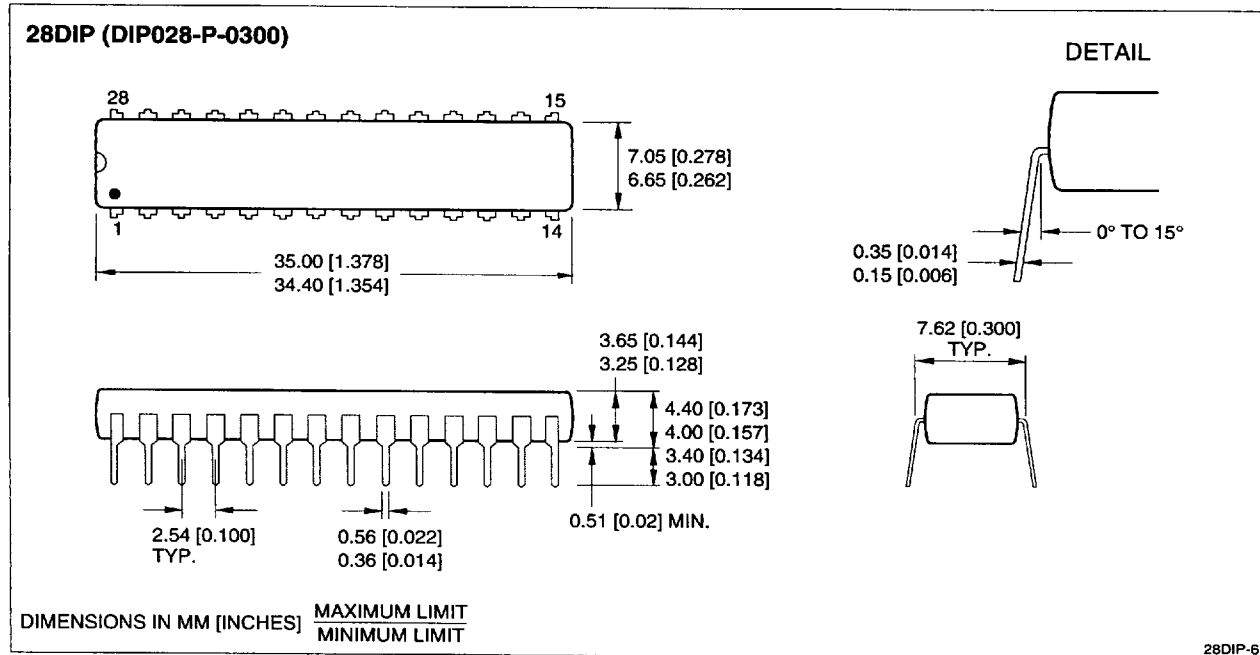


Figure 7. Write Cycle 2

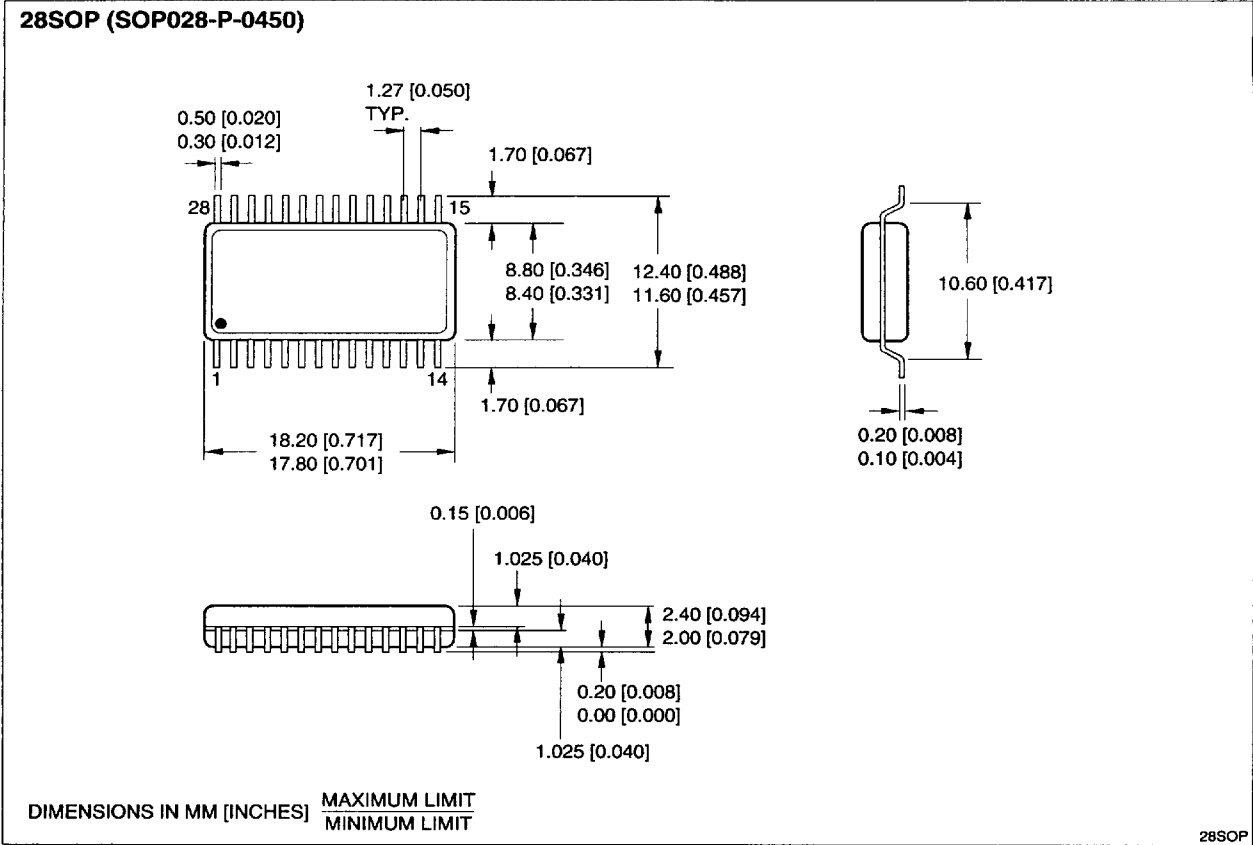
PACKAGE DIAGRAMS



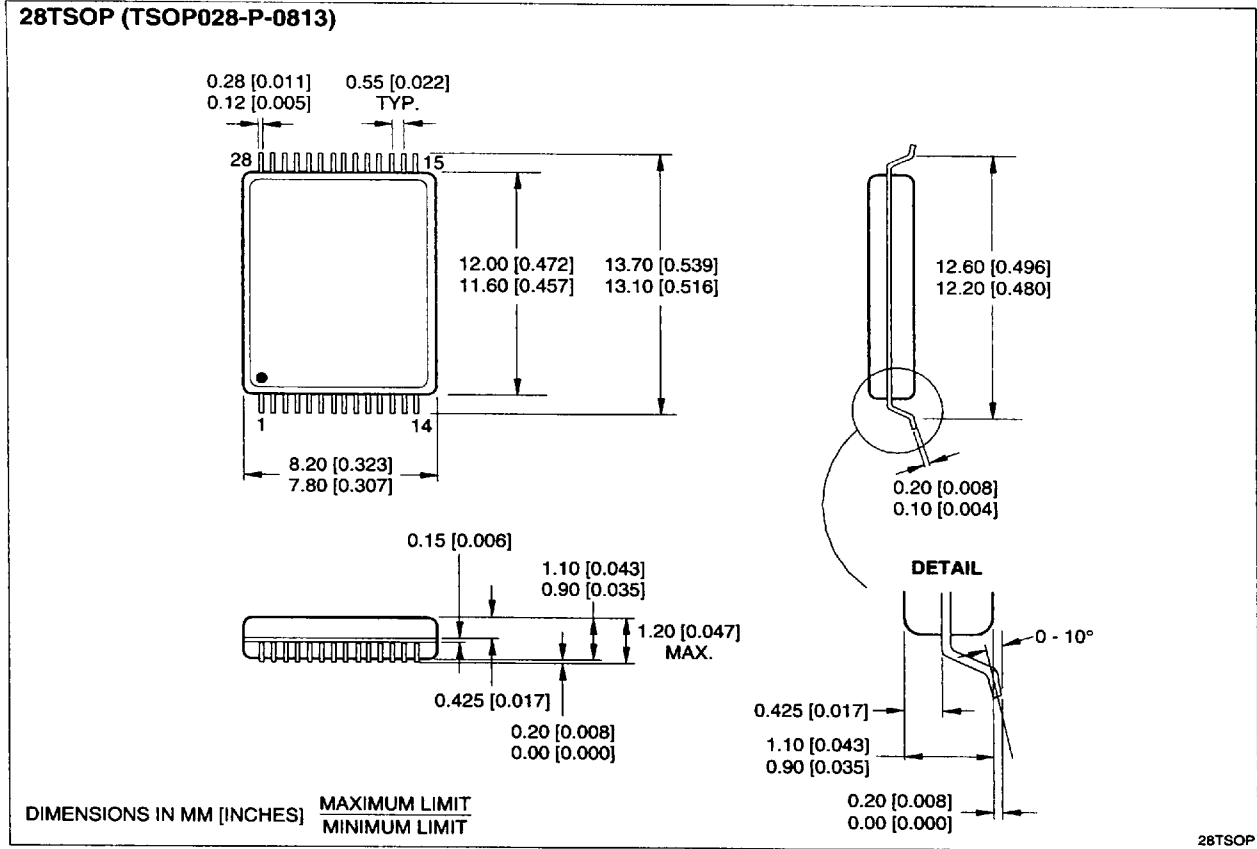
28-pin, 600-mil DIP



28-pin, 300-mil SK-DIP



28-pin, 450-mil SOP



28-pin, 8 × 13 mm<sup>2</sup> TSOP (Type I)

**ORDERING INFORMATION**

LH5164A	X	X	- ##	L
Device Type	Operating Temperature	Package	Speed	Power
				Low-power standby
			{ 10 100	Access Time (ns)
			{ 80 80	
				{ Blank 28 pin, 600-mil DIP (DIP028-P-0600)
				{ D 28-pin, 300-mil SK-DIP (SK-DIP028-P-0300)
				{ N 28-pin, 450-mil SOP (SOP028-P-0450)
				{ T 28-pin, 8 x 13 mm <sup>2</sup> TSOP (Type I) (TSOP028-P-0813)
				{ Blank -10 to 70°C
				{ H -40 to +85°C
				CMOS 64K (8K x 8) Static RAM

**Example:** LH5164AD-10L (CMOS 64K (8K x 8) Static RAM, 100 ns, Low-power standby, 28-pin, 300-mil SK-DIP)

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