

M37702M2AXXFP, M37702M2BXXFP

M37702M2-XXXFP and M37702S1FP are respectively unified into M37702M2AXXFP and M37702S1AFP.

M37702S1AFP, M37702S1BFP

SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M37702M2AXXFP is a single-chip microcomputers designed with high-performance CMOS silicon gate technology. This is housed in a 80-pin plastic molded QFP. This single-chip microcomputer has a large 16M bytes address space, three instruction queue buffers, and two data buffers for high-speed instruction execution. The CPU is a 16-bit parallel processor that can also be switched to perform 8-bit parallel processing. This microcomputer is suitable for office, business, and industrial equipment controller that require high-speed processing of large data.

The differences between M37702M2AXXFP, M37702M2BXXXFP, M37702S1AFP and M37702S1BFP are the ROM size and the external clock input frequency as shown below. Therefore, the following descriptions will be for the M37702M2AXXFP unless otherwise noted.

Type name	ROM size	External clock input frequency
M37702M2AXXFP	16K bytes	16MHz
M37702M2BXXXFP	16K bytes	25MHz
M37702S1AFP	External	16MHz
M37702S1BFP	External	25MHz

FEATURES

- Number of basic instructions.....103
- Memory size ROM.....16K bytes
RAM.....512 bytes
- Instruction execution time
M37702M2AXXFP, M37702S1AFP
(The fastest instruction at 16MHz frequency)..... 250ns.

M37702M2BXXXFP, M37702S1BFP

(The fastest instruction at 25MHz frequency)..... 160ns

- Single power supply.....5V±10%
- Low power dissipation (at 16MHz frequency)
..... 60mW (Typ.)
- Interrupts..... 19 types 7 levels
- Multiple function 16-bit timer..... 5+3
- UART (may also be synchronous)..... 2
- 8-bit A-D converter..... 8-channel inputs
- 12-bit watchdog timer
- Programmable input/output
(ports P0, P1, P2, P3, P4, P5, P6, P7, P8)..... 68

APPLICATION

Control devices for office equipment such as copiers, printers, typewriters, facsimiles, word processors, and personal computers

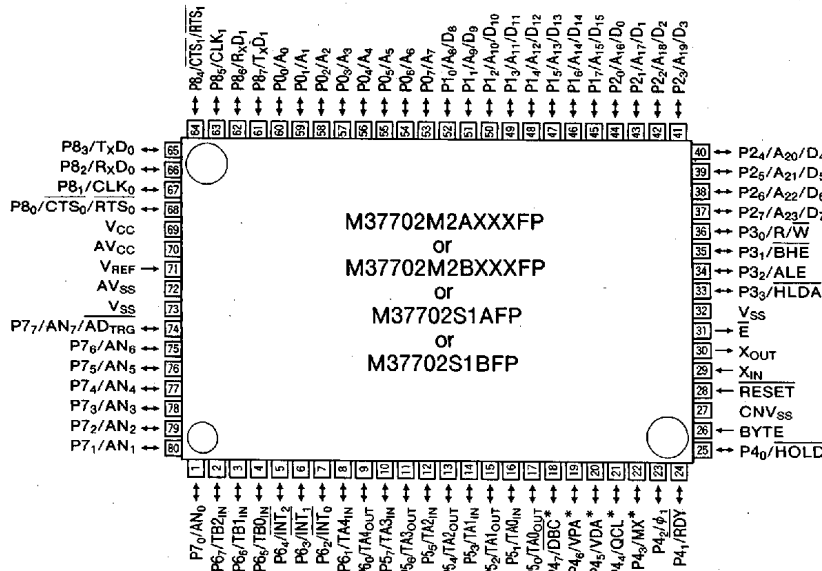
Control devices for industrial equipment such as ME, NC, communication and measuring instruments

NOTE

Refer to "Chapter 5 PRECAUTIONS" when using this microcomputer.

The M37702M2AXXFP and M37702S1AFP satisfy the timing requirements and the switching characteristics of the former M37702M2-XXXFP and M37702S1FP.

PIN CONFIGURATION (TOP VIEW)



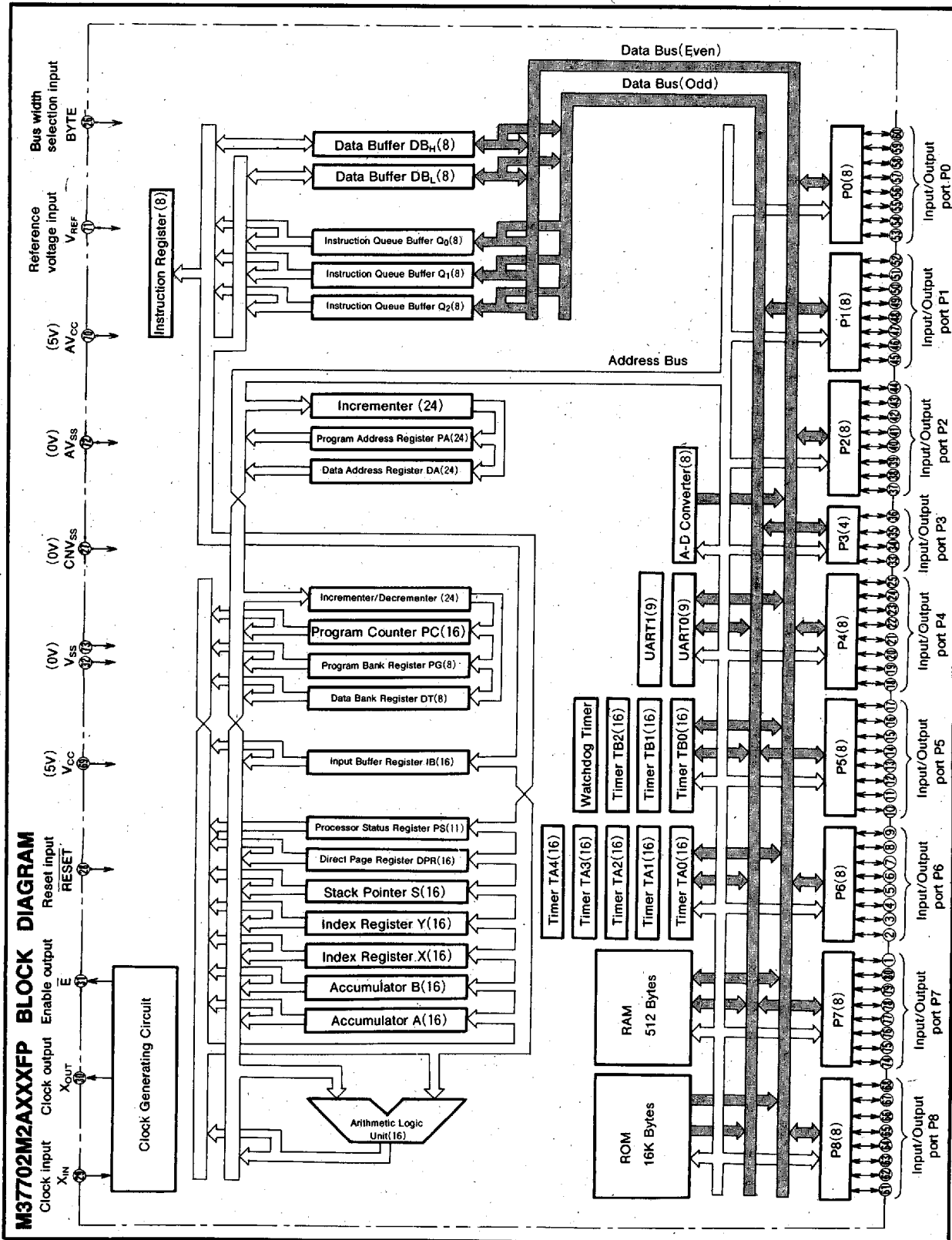
Outline 80P6N-A

*: Used in the evaluation chip mode only

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SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER

FUNCTIONS OF M37702M2AXXFP

Parameter		Functions
Number of basic instructions		103
Instruction execution time	M37702M2AXXFP, M37702S1AFP	250ns (the fastest instruction at external clock 16MHz frequency)
	M37702M2BXXFP, M37702S1BFP	160ns (the fastest instruction at external clock 25MHz frequency)
Memory size	ROM	16K bytes
	RAM	512 bytes
Input/Output ports	P0~P2, P4~P8	8-bitX 8
	P3	4-bitX 1
Multi-function timers	TA0, TA1, TA2, TA3, TA4	16-bitX 5
	TB0, TB1, TB2	16-bitX 3
Serial I/O		(UART or clock synchronous serial I/O)X2
A-D converter		8-bitX 1 (8 channels)
Watchdog timer		12-bitX 1
Interrupts		3 external types, 16 internal types (Each interrupt can be set the priority levels to 0~7.)
Clock generating circuit		Built-in(externally connected to a ceramic resonator or quartz crystal resonator)
Supply voltage		5V±10%
Power dissipation		60mW(at external clock 16MHz frequency)
Input/Output characteristic	Input/Output voltage	5V
	Output current	5mA
Memory expansion		Maximum 16M bytes
Operating temperature range		-20~85°C
Device structure		CMOS high-performance silicon gate process
Package		80-pin plastic molded QFP

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PIN DESCRIPTION

Pin	Name	Input/Output	Functions
V _{CC} , V _{SS}	Power supply		Supply 5 V ± 10% to V _{CC} and 0 V to V _{SS} .
CNV _{SS}	CNV _{SS} input	Input	This pin controls the processor mode. Connect to V _{SS} for single-chip mode, and to V _{CC} for external ROM types.
RESET	Reset input	Input	To enter the reset state, this pin must be kept at a "L" condition which should be maintained for the required time.
X _{IN}	Clock input	Input	These are I/O pins of internal clock generating circuit. Connect a ceramic or quartz crystal resonator between X _{IN} and X _{OUT} . When an external clock is used, the clock source should be connected to the X _{IN} pin and the X _{OUT} pin should be left open.
X _{OUT}	Clock output	Output	
E	Enable output	Output	Data or instruction read and data write are performed when output from this pin is "L".
BYTE	Bus width selection input	Input	In memory expansion mode or microprocessor mode, this pin determines whether the external data bus is 8-bit width or 16-bit width. The width is 16 bits when "L" signal inputs and 8 bits when "H" signal inputs.
AV _{CC} AV _{SS}	Analog supply input		Power supply for the A-D converter. Connect AV _{CC} to V _{CC} and AV _{SS} to V _{SS} externally.
V _{REF}	Reference voltage input	Input	This is reference voltage input pin for the A-D converter.
P0 ₀ ~P0 ₇	I/O port P0	I/O	In single-chip mode, port P0 becomes an 8-bit I/O port. An I/O direction register is available so that each pin can be programmed for input or output. These ports are in input mode when reset. Address(A ₇ ~A ₀) is output in memory expansion mode or microprocessor mode.
P1 ₀ ~P1 ₇	I/O port P1	I/O	In single-chip mode, these pins have the same functions as port P0. When the BYTE pin is set to "L" in memory expansion mode or microprocessor mode and external data bus is 16-bit width, high-order data (D ₁₅ ~D ₈) is input or output when E output is "L" and an address (A ₁₅ ~A ₈) is output when E output is "H". If the BYTE pin is "H" that is an external data bus is 8-bit width, only address(A ₁₅ ~A ₈) is output.
P2 ₀ ~P2 ₇	I/O port P2	I/O	In single-chip mode, these pins have the same functions as port P0. In memory expansion mode or microprocessor mode low-order data(D ₇ ~D ₀) is input or output when E output is "L" and an address(A ₂₃ ~A ₁₆) is output when E output is "H".
P3 ₀ ~P3 ₃	I/O port P3	I/O	In single-chip mode, these pins have the same functions as port P0. In memory expansion mode or microprocessor mode, R/W, BHE, ALE, and HLDA signals are output.
P4 ₀ ~P4 ₇	I/O port P4	I/O	In single-chip mode, these pins have the same functions as port P0. In memory expansion mode or microprocessor mode, P4 ₀ and P4 ₁ become HOLD and RDY input pin respectively. Functions of other pins are the same as in single-chip mode. In single-chip mode or memory expansion mode, port P4 ₂ can be programmed for φ ₁ output pin divided the clock to X _{IN} pin by 2. In microprocessor mode, P4 ₂ always has the function as φ ₁ output pin.
P5 ₀ ~P5 ₇	I/O port P5	I/O	In addition to having the same functions as port P0 in single-chip mode, these pins also function as I/O pins for timer A0, timer A1, timer A2 and timer A3.
P6 ₀ ~P6 ₇	I/O port P6	I/O	In addition to having the same functions as port P0 in single-chip mode, these pins also function as I/O pins for timer A4, external interrupt input INT ₀ , INT ₁ , and INT ₂ pins, and input pins for timer B0, timer B1 and timer B2.
P7 ₀ ~P7 ₇	I/O port P7	I/O	In addition to having the same functions as port P0 in single-chip mode, these pins also function as analog input AN ₀ ~AN ₇ input pins. P7 ₇ also has an A-D conversion trigger input function.
P8 ₀ ~P8 ₇	I/O port P8	I/O	In addition to having the same functions as port P0 in single-chip mode, these pins also function as RxD, TxD, CLK, CTS/RTS pins for UART 0 and UART 1.

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M37702M2AXXFP

ELECTRICAL CHARACTERISTICS ($V_{CC}=5V$, $V_{SS}=0V$, $T_a=25^\circ C$, $f(X_{IN})=16MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	High-level output voltage P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ , P3 ₀ , P3 ₁ , P3 ₃ , P4 ₀ ~P4 ₇ , P5 ₀ ~P5 ₇ , P6 ₀ ~P6 ₇ , P7 ₀ ~P7 ₇ , P8 ₀ ~P8 ₇	$I_{OH}=-10mA$	3			V
V_{OH}	High-level output voltage P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ , P3 ₀ , P3 ₁ , P3 ₃	$I_{OH}=-400\mu A$	4.7			V
V_{OH}	High-level output voltage P3 ₂	$I_{OH}=-10mA$ $I_{OH}=-400\mu A$	3.1 4.8			V
V_{OH}	High-level output voltage \bar{E}	$I_{OH}=-10mA$ $I_{OH}=-400\mu A$	3.4 4.8			V
V_{OL}	Low-level output voltage P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ , P3 ₀ , P3 ₁ , P3 ₃ , P4 ₀ ~P4 ₇ , P5 ₀ ~P5 ₇ , P6 ₀ ~P6 ₇ , P7 ₀ ~P7 ₇ , P8 ₀ ~P8 ₇	$I_{OL}=10mA$			2	V
V_{OL}	Low-level output voltage P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ , P3 ₀ , P3 ₁ , P3 ₃	$I_{OL}=2mA$			0.45	V
V_{OL}	Low-level output voltage P3 ₂	$I_{OL}=10mA$ $I_{OL}=2mA$			1.9 0.43	V
V_{OL}	Low-level output voltage \bar{E}	$I_{OL}=10mA$ $I_{OL}=2mA$			1.6 0.4	V
$V_{T+}-V_{T-}$	Hysteresis HOLD, RDY, TA0 _{IN} ~TA4 _{IN} , TB0 _{IN} ~TB2 _{IN} , INT0~INT2, AD _{TRG} , CTS0, CTS1, CLK0, CLK1		0.4		1	V
$V_{T+}-V_{T-}$	Hysteresis RESET		0.2		0.5	V
$V_{T+}-V_{T-}$	Hysteresis X _{IN}		0.1		0.3	V
I_{IH}	High-level input current P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ , P3 ₀ ~P3 ₃ , P4 ₀ ~P4 ₇ , P5 ₀ ~P5 ₇ , P6 ₀ ~P6 ₇ , P7 ₀ ~P7 ₇ , P8 ₀ ~P8 ₇ , X _{IN} , RESET, CNV _{SS} , BYTE	$V_I=5V$			5	μA
I_{IL}	Low-level input current P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ , P3 ₀ ~P3 ₃ , P4 ₀ ~P4 ₇ , P5 ₀ ~P5 ₇ , P6 ₀ ~P6 ₇ , P7 ₀ ~P7 ₇ , P8 ₀ ~P8 ₇ , X _{IN} , RESET, CNV _{SS} , BYTE	$V_I=0V$			-5	μA
V_{RAM}	RAM hold voltage	When clock is stopped.	2			V
I_{CC}	Power supply current	In single-chip mode output only pin is open and other pins are V_{SS} during reset.		12	24	μA
		$f(X_{IN})=16MHz$, square waveform $T_a=25^\circ C$ when clock is stopped. $T_a=85^\circ C$ when clock is stopped.			1 20	μA

A-D CONVERTER CHARACTERISTICS ($V_{CC}=5V$, $V_{SS}=0V$, $T_a=25^\circ C$, $f(X_{IN})=16MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution	$V_{REF}=V_{CC}$			8	Bits
—	Absolute accuracy	$V_{REF}=V_{CC}$			± 3	LSB
R_{LADDER}	Ladder resistance	$V_{REF}=V_{CC}$	2		10	$k\Omega$
t_{CONV}	Conversion time		14.25			μs
V_{REF}	Reference voltage		2		V_{CC}	V
V_{IA}	Analog input voltage		0		V_{REF}	V

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		-0.3~7	V
AV_{CC}	Analog supply voltage		-0.3~7	V
V_I	Input voltage RESET, CNV _{SS} , BYTE		-0.3~12	V
V_I	Input voltage P ₀ ~P ₀₇ , P ₁ ~P ₁₇ , P ₂ ~P ₂₇ , P ₃ ~P ₃₃ , P ₄ ~P ₄₇ , P ₅ ~P ₅₇ , P ₆ ~P ₆₇ , P ₇ ~P ₇₇ , P ₈ ~P ₈₇ , V _{REF} , X _{IN}		-0.3~ $V_{CC}+0.3$	V
V_O	Output voltage P ₀ ~P ₀₇ , P ₁ ~P ₁₇ , P ₂ ~P ₂₇ , P ₃ ~P ₃₃ , P ₄ ~P ₄₇ , P ₅ ~P ₅₇ , P ₆ ~P ₆₇ , P ₇ ~P ₇₇ , P ₈ ~P ₈₇ , X _{OUT} , \bar{E}		-0.3~ $V_{CC}+0.3$	V
P_d	Power dissipation	T _a =25°C	300	mW
T _{opr}	Operating temperature		-20~85	°C
T _{stg}	Storage temperature		-40~150	°C

RECOMMENDED OPERATING CONDITIONS ($V_{CC}=5V\pm 10\%$, T_a=-20~85°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
AV_{CC}	Analog supply voltage		V_{CC}		V
V_{SS}	Supply voltage		0		V
AV_{SS}	Analog supply voltage		0		V
V_{IH}	High-level input voltage P ₀ ~P ₀₇ , P ₃ ~P ₃₃ , P ₄ ~P ₄₇ , P ₅ ~P ₅₇ , P ₆ ~P ₆₇ , P ₇ ~P ₇₇ , P ₈ ~P ₈₇ , X _{IN} , RESET, CNV _{SS} , BYTE	0.8 V_{CC}		V_{CC}	V
V_{IH}	High-level input voltage P ₁ ~P ₁₇ , P ₂ ~P ₂₇ (in single-chip mode)	0.8 V_{CC}		V_{CC}	V
V_{IH}	High-level input voltage P ₁ ~P ₁₇ , P ₂ ~P ₂₇ (in memory expansion mode and microprocessor mode)	0.5 V_{CC}		V_{CC}	V
V_{IL}	Low-level input voltage P ₀ ~P ₀₇ , P ₃ ~P ₃₃ , P ₄ ~P ₄₇ , P ₅ ~P ₅₇ , P ₆ ~P ₆₇ , P ₇ ~P ₇₇ , P ₈ ~P ₈₇ , X _{IN} , RESET, CNV _{SS} , BYTE	0		0.2 V_{CC}	V
V_{IL}	Low-level input voltage P ₁ ~P ₁₇ , P ₂ ~P ₂₇ (in single-chip mode)	0		0.2 V_{CC}	V
V_{IL}	Low-level input voltage P ₁ ~P ₁₇ , P ₂ ~P ₂₇ (in memory expansion mode and microprocessor mode)	0		0.16 V_{CC}	V
$I_{OH(peak)}$	High-level peak output current P ₀ ~P ₀₇ , P ₁ ~P ₁₇ , P ₂ ~P ₂₇ , P ₃ ~P ₃₃ , P ₄ ~P ₄₇ , P ₅ ~P ₅₇ , P ₆ ~P ₆₇ , P ₇ ~P ₇₇ , P ₈ ~P ₈₇			-10	mA
$I_{OH(avg)}$	High-level average output current P ₀ ~P ₀₇ , P ₁ ~P ₁₇ , P ₂ ~P ₂₇ , P ₃ ~P ₃₃ , P ₄ ~P ₄₇ , P ₅ ~P ₅₇ , P ₆ ~P ₆₇ , P ₇ ~P ₇₇ , P ₈ ~P ₈₇			-5	mA
$I_{OL(peak)}$	Low-level peak output current P ₀ ~P ₀₇ , P ₁ ~P ₁₇ , P ₂ ~P ₂₇ , P ₃ ~P ₃₃ , P ₄ ~P ₄₇ , P ₅ ~P ₅₇ , P ₆ ~P ₆₇ , P ₇ ~P ₇₇ , P ₈ ~P ₈₇			10	mA
$I_{OL(avg)}$	Low-level average output current P ₀ ~P ₀₇ , P ₁ ~P ₁₇ , P ₂ ~P ₂₇ , P ₃ ~P ₃₃ , P ₄ ~P ₄₇ , P ₅ ~P ₅₇ , P ₆ ~P ₆₇ , P ₇ ~P ₇₇ , P ₈ ~P ₈₇			5	mA
f(X _{IN})	External clock frequency input			16	MHz
				25	

- Note 1. Average output current is the average value of a 100ms interval.
 2. The sum of I_{OL(peak)} for ports P₀, P₁, P₂, P₃, and P₈ must be 80mA or less, the sum of I_{OH(peak)} for ports P₀, P₁, P₂, P₃, and P₈ must be 80mA or less, the sum of I_{OL(peak)} for ports P₄, P₅, P₆, and P₇ must be 80mA or less, and the sum of I_{OH(peak)} for ports P₄, P₅, P₆, and P₇ must be 80mA or less.

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TIMING REQUIREMENTS ($V_{CC}=5V \pm 10\%$, $V_{SS}=0V$, $T_a=25^\circ C$, unless otherwise noted)

External clock input

Symbol	Parameter	Limits				Unit
		16MHz		25MHz		
		Min.	Max.	Min.	Max.	
t_c	External clock input cycle time	62		40		ns
$t_{w(H)}$	External clock input high-level pulse width	25		15		ns
$t_{w(L)}$	External clock input low-level pulse width	25		15		ns
t_r	External clock rise time		10		8	ns
t_f	External clock fall time		10		8	ns

Single-chip mode

Symbol	Parameter	Limits				Unit
		16MHz		25MHz		
		Min.	Max.	Min.	Max.	
$t_{su(P0D-E)}$	Port P0 input setup time	100		60		ns
$t_{su(P1D-E)}$	Port P1 input setup time	100		60		ns
$t_{su(P2D-E)}$	Port P2 input setup time	100		60		ns
$t_{su(P3D-E)}$	Port P3 input setup time	100		60		ns
$t_{su(P4D-E)}$	Port P4 input setup time	100		60		ns
$t_{su(P5D-E)}$	Port P5 input setup time	100		60		ns
$t_{su(P6D-E)}$	Port P6 input setup time	100		60		ns
$t_{su(P7D-E)}$	Port P7 input setup time	100		60		ns
$t_{su(P8D-E)}$	Port P8 input setup time	100		60		ns
$t_{h(E-P0D)}$	Port P0 input hold time	0		0		ns
$t_{h(E-P1D)}$	Port P1 input hold time	0		0		ns
$t_{h(E-P2D)}$	Port P2 input hold time	0		0		ns
$t_{h(E-P3D)}$	Port P3 input hold time	0		0		ns
$t_{h(E-P4D)}$	Port P4 input hold time	0		0		ns
$t_{h(E-P5D)}$	Port P5 input hold time	0		0		ns
$t_{h(E-P6D)}$	Port P6 input hold time	0		0		ns
$t_{h(E-P7D)}$	Port P7 input hold time	0		0		ns
$t_{h(E-P8D)}$	Port P8 input hold time	0		0		ns

Memory expansion mode and microprocessor mode

Symbol	Parameter	Limits				Unit
		16MHz		25MHz		
		Min.	Max.	Min.	Max.	
$t_{su(P1D-E)}$	Port P1 input setup time	45		30		ns
$t_{su(P2D-E)}$	Port P2 input setup time	45		30		ns
$t_{su(RDY-\phi_1)}$	RDY input setup time	60		55		ns
$t_{su(HOLD-\phi_1)}$	HOLD input setup time	60		55		ns
$t_{h(E-P1D)}$	Port P1 input hold time	0		0		ns
$t_{h(E-P2D)}$	Port P2 input hold time	0		0		ns
$t_{h(\phi_1-RDY)}$	RDY input hold time	0		0		ns
$t_{h(\phi_1-HOLD)}$	HOLD input hold time	0		0		ns

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M37702M2BXXFP

ELECTRICAL CHARACTERISTICS ($V_{CC}=5V$, $V_{SS}=0V$, $T_a=25^\circ C$, $f(X_{IN})=25MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	High-level output voltage P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ , P3 ₀ , P3 ₁ , P3 ₃ , P4 ₀ ~P4 ₇ , P5 ₀ ~P5 ₇ , P6 ₀ ~P6 ₇ , P7 ₀ ~P7 ₇ , P8 ₀ ~P8 ₇	$I_{OH}=-10mA$	3			V
V_{OH}	High-level output voltage P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ , P3 ₀ , P3 ₁ , P3 ₃	$I_{OH}=-400\mu A$	4.7			V
V_{OH}	High-level output voltage P3 ₂	$I_{OH}=-10mA$ $I_{OH}=-400\mu A$	3.1 4.8			V
V_{OH}	High-level output voltage \bar{E}	$I_{OH}=-10mA$ $I_{OH}=-400\mu A$	3.4 4.8			V
V_{OL}	Low-level output voltage P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ , P3 ₀ , P3 ₁ , P3 ₃ , P4 ₀ ~P4 ₇ , P5 ₀ ~P5 ₇ , P6 ₀ ~P6 ₇ , P7 ₀ ~P7 ₇ , P8 ₀ ~P8 ₇	$I_{OL}=10mA$			2	V
V_{OL}	Low-level output voltage P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ , P3 ₀ , P3 ₁ , P3 ₃	$I_{OL}=2mA$			0.45	V
V_{OL}	Low-level output voltage P3 ₂	$I_{OL}=10mA$ $I_{OL}=2mA$			1.9 0.43	V
V_{OL}	Low-level output voltage \bar{E}	$I_{OL}=10mA$ $I_{OL}=2mA$			1.6 0.4	V
$V_{T+}-V_{T-}$	Hysteresis HOLD, RDY, TA0 _{IN} ~TA4 _{IN} , TB0 _{IN} ~TB2 _{IN} , INT0~INT2, AD _{TRG} , CTS0, CTS1, CLK0, CLK1		0.4		1	V
$V_{T+}-V_{T-}$	Hysteresis RESET		0.2		0.5	V
$V_{T+}-V_{T-}$	Hysteresis X _{IN}		0.1		0.3	V
I_{IH}	High-level input current P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ , P3 ₀ ~P3 ₃ , P4 ₀ ~P4 ₇ , P5 ₀ ~P5 ₇ , P6 ₀ ~P6 ₇ , P7 ₀ ~P7 ₇ , P8 ₀ ~P8 ₇ , X _{IN} , RESET, CNV _{SS} , BYTE	$V_I=5V$			5	μA
I_{IL}	Low-level input current P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ , P3 ₀ ~P3 ₃ , P4 ₀ ~P4 ₇ , P5 ₀ ~P5 ₇ , P6 ₀ ~P6 ₇ , P7 ₀ ~P7 ₇ , P8 ₀ ~P8 ₇ , X _{IN} , RESET, CNV _{SS} , BYTE	$V_I=0V$			-5	μA
V_{RAM}	RAM hold voltage	When clock is stopped.	2			V
I_{CC}	Power supply current	In single-chip mode output only pin is open and other pins are V _{SS} during reset.		19	38	mA
		$f(X_{IN})=25MHz$, square waveform $T_a=25^\circ C$ when clock is stopped. $T_a=85^\circ C$ when clock is stopped.			1 20	μA

A-D CONVERTER CHARACTERISTICS ($V_{CC}=5V$, $V_{SS}=0V$, $T_a=25^\circ C$, $f(X_{IN})=25MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution	$V_{REF}=V_{CC}$			8	Bits
—	Absolute accuracy	$V_{REF}=V_{CC}$			± 3	LSB
R_{LADDER}	Ladder resistance	$V_{REF}=V_{CC}$	2		10	k Ω
t_{CONV}	Conversion time		9.12			μs
V_{REF}	Reference voltage		2		V_{CC}	V
V_{IA}	Analog input voltage		0		V_{REF}	V

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Timer A input (Count input in event counter mode)

Symbol	Parameter	Limits				Unit
		16MHz		25MHz		
		Min.	Max.	Min.	Max.	
$t_{C(TA)}$	TA _{IN} input cycle time	125		80		ns
$t_{W(TAH)}$	TA _{IN} input high-level pulse width	62		40		ns
$t_{W(TAL)}$	TA _{IN} input low-level pulse width	62		40		ns

Timer A input (Gating input in timer mode)

Symbol	Parameter	Limits				Unit
		16MHz		25MHz		
		Min.	Max.	Min.	Max.	
$t_{C(TA)}$	TA _{IN} input cycle time	500		320		ns
$t_{W(TAH)}$	TA _{IN} input high-level pulse width	250		160		ns
$t_{W(TAL)}$	TA _{IN} input low-level pulse width	250		160		ns

Timer A input (External trigger input in one-shot pulse mode)

Symbol	Parameter	Limits				Unit
		16MHz		25MHz		
		Min.	Max.	Min.	Max.	
$t_{C(TA)}$	TA _{IN} input cycle time	250		160		ns
$t_{W(TAH)}$	TA _{IN} input high-level pulse width	125		80		ns
$t_{W(TAL)}$	TA _{IN} input low-level pulse width	125		80		ns

Timer A input (External trigger input in pulse width modulation mode)

Symbol	Parameter	Limits				Unit
		16MHz		25MHz		
		Min.	Max.	Min.	Max.	
$t_{W(TAH)}$	TA _{IN} input high-level pulse width	125		80		ns
$t_{W(TAL)}$	TA _{IN} input low-level pulse width	125		80		ns

Timer A input (Up-down input in event counter mode)

Symbol	Parameter	Limits				Unit
		16MHz		25MHz		
		Min.	Max.	Min.	Max.	
$t_{C(UP)}$	TA _{OUT} input cycle time	2500		2000		ns
$t_{W(UPH)}$	TA _{OUT} input high-level pulse width	1250		1000		ns
$t_{W(UPL)}$	TA _{OUT} input low-level pulse width	1250		1000		ns
$t_{SU(UP-TIN)}$	TA _{OUT} input setup time	500		400		ns
$t_{H(TIN-UP)}$	TA _{OUT} input hold time	500		400		ns

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Timer B input (Count input in event counter mode)

Symbol	Parameter	Limits				Unit
		16MHz		25MHz		
		Min.	Max.	Min.	Max.	
$t_{C(TB)}$	TBI _N input cycle time (one edge count)	125		80		ns
$t_{W(TBH)}$	TBI _N input high-level pulse width (one edge count)	62		40		ns
$t_{W(TBL)}$	TBI _N input low-level pulse width (one edge count)	62		40		ns
$t_{C(TB)}$	TBI _N input cycle time (both edges count)	250		160		ns
$t_{W(TBH)}$	TBI _N input high-level pulse width (both edges count)	125		80		ns
$t_{W(TBL)}$	TBI _N input low-level pulse width (both edges count)	125		80		ns

Timer B input (Pulse period measurement mode)

Symbol	Parameter	Limits				Unit
		16MHz		25MHz		
		Min.	Max.	Min.	Max.	
$t_{C(TB)}$	TBI _N input cycle time	500		320		ns
$t_{W(TBH)}$	TBI _N input high-level pulse width	250		160		ns
$t_{W(TBL)}$	TBI _N input low-level pulse width	250		160		ns

Timer B input (Pulse width measurement mode)

Symbol	Parameter	Limits				Unit
		16MHz		25MHz		
		Min.	Max.	Min.	Max.	
$t_{C(TB)}$	TBI _N input cycle time	500		320		ns
$t_{W(TBH)}$	TBI _N input high-level pulse width	250		160		ns
$t_{W(TBL)}$	TBI _N input low-level pulse width	250		160		ns

A-D trigger input

Symbol	Parameter	Limits				Unit
		16MHz		25MHz		
		Min.	Max.	Min.	Max.	
$t_{C(AD)}$	AD _{TRG} input cycle time (minimum allowable trigger)	1000		1000		ns
$t_{W(ADL)}$	AD _{TRG} input low-level pulse width	125		125		ns

Serial I/O

Symbol	Parameter	Limits				Unit
		16MHz		25MHz		
		Min.	Max.	Min.	Max.	
$t_{C(CLK)}$	CLK _j input cycle time	250		200		ns
$t_{W(CLKH)}$	CLK _j input high-level pulse width	125		100		ns
$t_{W(CLKL)}$	CLK _j input low-level pulse width	125		100		ns
$t_{d(C-O)}$	TxD _j output delay time		90		80	ns
$t_{h(C-O)}$	TxD _j hold time	0		0		ns
$t_{SU(D-C)}$	RxD _j input setup time	30		20		ns
$t_{h(C-D)}$	RxD _j input hold time	90		90		ns

External interrupt INT_j input

Symbol	Parameter	Limits				Unit
		16MHz		25MHz		
		Min.	Max.	Min.	Max.	
$t_{W(INH)}$	INT _j input high-level pulse width	250		250		ns
$t_{W(INL)}$	INT _j input low-level pulse width	250		250		ns

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SWITCHING CHARACTERISTICS ($V_{CC}=5V\pm 10\%$, $V_{SS}=0V$, $T_a=25^\circ C$, unless otherwise noted)

Single-chip mode

Symbol	Parameter	Test conditions	Limits				Unit
			16MHz		25MHz		
			Min.	Max.	Min.	Max.	
$t_{d(E-P0Q)}$	Port P0 data output delay time	Fig. 58		100		80	ns
$t_{d(E-P1Q)}$	Port P1 data output delay time			100		80	ns
$t_{d(E-P2Q)}$	Port P2 data output delay time			100		80	ns
$t_{d(E-P3Q)}$	Port P3 data output delay time			100		80	ns
$t_{d(E-P4Q)}$	Port P4 data output delay time			100		80	ns
$t_{d(E-P5Q)}$	Port P5 data output delay time			100		80	ns
$t_{d(E-P6Q)}$	Port P6 data output delay time			100		80	ns
$t_{d(E-P7Q)}$	Port P7 data output delay time			100		80	ns
$t_{d(E-P8Q)}$	Port P8 data output delay time			100		80	ns

Memory expansion mode and microprocessor mode (when wait bit = "1")

Symbol	Parameter	Test conditions	Limits				Unit
			16MHz		25MHz		
			Min.	Max.	Min.	Max.	
$t_{d(P0A-E)}$	Port P0 address output delay time	Fig. 58	30		12		ns
$t_{d(E-P1Q)}$	Port P1 data output delay time (BYTE="L")			70		45	ns
$t_{PXZ(E-P1Z)}$	Port P1 floating start delay time (BYTE="L")			5		5	ns
$t_{d(P1A-E)}$	Port P1 address output delay time		30		12		ns
$t_{d(P1A-ALE)}$	Port P1 address output delay time		24		5		ns
$t_{d(E-P2Q)}$	Port P2 data output delay time			70		45	ns
$t_{PXZ(E-P2Z)}$	Port P2 floating start delay time			5		5	ns
$t_{d(P2A-E)}$	Port P2 address output delay time		30		12		ns
$t_{d(P2A-ALE)}$	Port P2 address output delay time		24		5		ns
$t_{d(\phi_1-HLDA)}$	HLDA output delay time			50		50	ns
$t_{d(ALE-E)}$	ALE output delay time		4		4		ns
$t_{W(ALE)}$	ALE pulse width		35		22		ns
$t_{d(BHE-E)}$	BHE output delay time		30		20		ns
$t_{d(R/W-E)}$	R/W output delay time		30		20		ns
$t_{d(E-\phi_1)}$	ϕ_1 output delay time		0	20	0	18	ns
$t_h(E-P0A)$	Port P0 address hold time		25		18		ns
$t_h(ALE-P1A)$	Port P1 address hold time (BYTE="L")		9		9		ns
$t_h(E-P1Q)$	Port P1 data hold time (BYTE="L")		25		18		ns
$t_{PZX(E-P1Z)}$	Port P1 floating release delay time (BYTE="L")		25		18		ns
$t_h(E-P1A)$	Port P1 address hold time (BYTE="H")		25		18		ns
$t_h(ALE-P2A)$	Port P2 address hold time		9		9		ns
$t_h(E-P2Q)$	Port P2 data hold time		25		18		ns
$t_{PZX(E-P2Z)}$	Port P2 floating release delay time		25		18		ns
$t_h(E-BHE)$	BHE hold time		18		18		ns
$t_h(E-R/W)$	R/W hold time		18		18		ns
$t_w(EL)$	\bar{E} pulse width		95		50		ns

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Memory expansion mode and microprocessor mode (when wait bit = "0", and external memory area accessed)

Symbol	Parameter	Test conditions	Limits				Unit
			16MHz		25MHz		
			Min.	Max.	Min.	Max.	
$t_{d(P0A-E)}$	Port P0 address output delay time	Fig. 58	30		12		ns
$t_{d(E-P1Q)}$	Port P1 data output delay time (BYTE="L")			70		45	ns
$t_{PXZ(E-P1Z)}$	Port P1 floating start delay time (BYTE="L")			5		5	ns
$t_{d(P1A-E)}$	Port P1 address output delay time		30		12		ns
$t_{d(P1A-ALE)}$	Port P1 address output delay time		24		5		ns
$t_{d(E-P2Q)}$	Port P2 data output delay time			70		45	ns
$t_{PXZ(E-P2Z)}$	Port P2 floating start delay time			5		5	ns
$t_{d(P2A-E)}$	Port P2 address output delay time		30		12		ns
$t_{d(P2A-ALE)}$	Port P2 address output delay time		24		5		ns
$t_{d}(\phi_1-HLDA)$	HLDA output delay time			50		50	ns
$t_{d(ALE-E)}$	ALE output delay time		4		4		ns
$t_{W(ALE)}$	ALE pulse width		35		22		ns
$t_{d(BHE-E)}$	BHE output delay time		30		20		ns
$t_{d(R/W-E)}$	R/W output delay time		30		20		ns
$t_{d(E-\phi_1)}$	ϕ_1 output delay time		0	20	0	18	ns
$t_{h(E-P0A)}$	Port P0 address hold time		25		18		ns
$t_{h(ALE-P1A)}$	Port P1 address hold time (BYTE="L")		9		9		ns
$t_{h(E-P1Q)}$	Port P1 data hold time (BYTE="L")		25		18		ns
$t_{PZX(E-P1Z)}$	Port P1 floating release delay time (BYTE="L")		25		18		ns
$t_{h(E-P1A)}$	Port P1 address hold time (BYTE="H")		25		18		ns
$t_{h(ALE-P2A)}$	Port P2 address hold time		9		9		ns
$t_{h(E-P2Q)}$	Port P2 data hold time		25		18		ns
$t_{PZX(E-P2Z)}$	Port P2 floating release delay time		25		18		ns
$t_{h(E-BHE)}$	BHE hold time		18		18		ns
$t_{h(E-R/W)}$	R/W hold time		18		18		ns
$t_{W(EL)}$	\bar{E} pulse width		220		130		ns

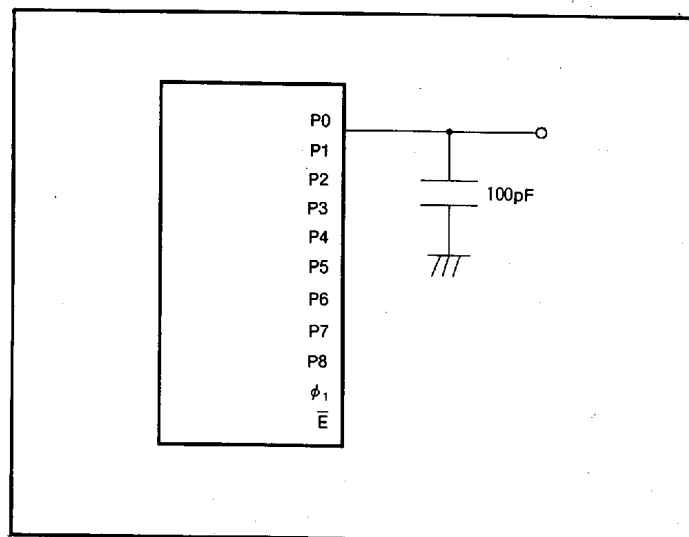


Fig. 58 Testing circuit for ports P0~P8, ϕ_1

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