M50734SP/FP
M50734SP/FP-10

8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M50734SP is a microcomputer designed with CMOS sillicon gate technology. It is housed in a 64-pin shrink plastic molded DIP (flat package type also available). This microcomputer is useful for business equipment and other consumer applications.

In addition to its simple instruction sets, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

The differences between the M50734SP-10 and the M50734SP are noted below.

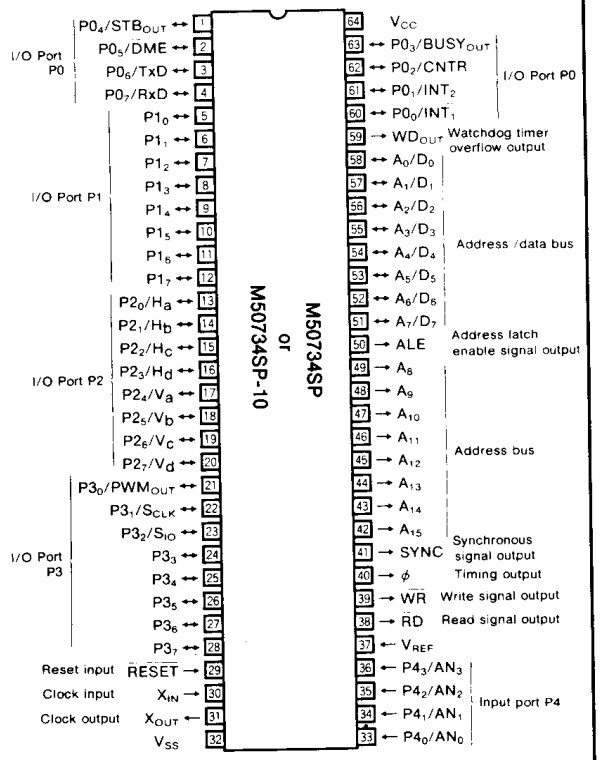
Type name	maximum value of clock generating frequency
M50734SP	8MHz
M50734SP-10	10MHz

The differences between the M50734SP and the M50734FP, and M50734SP-10 and M50734FP-10 are the package outline, the voltage input pins for A-D, and power dissipation ability (absolute maximum ratings).

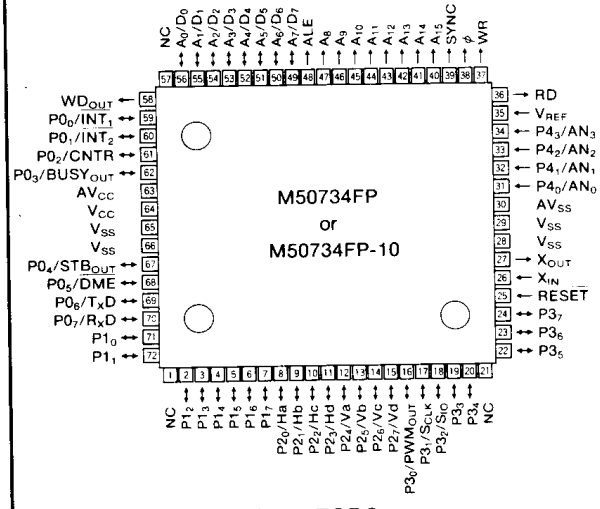
FEATURES

- Number of basic instructions 69
- Memory size (internal memories are not provided)
  - Memory area programmable memory ..... 64K bytes
  - data memory ..... 64K bytes
- Instruction execution time (minimum instructions)
  - ..... 1μs (at 8MHz frequency M50734SP)
  - ..... 0.8μs (at 10MHz frequency, M50734SP-10)
- Single power supply ..... 5V$\pm$10%
- Power dissipation
  - normal operation mode (at 8MHz frequency) 30mW
  - (at 10MHz frequency) 35mW
- Subroutine nesting ..... 128 levels (Max.)
- Interrupt ..... 11 types, 5 vectors
- Timers
  - 16-bit timer/event counter (general purpose) 1
  - 8-bit timer (general purpose) 3
  - 8-bit timer (watchdog timer) 1
  - 8-bit timer (strobe timer) 1
  - 8-bit timer (baud rate timer) 1
  - 8-bit counter (control for stepper motor) 2
- Stepper motor control circuit
  - ..... 1 channel for the X or Y direction
- Programmable I/O ports (Ports P0, P1, P2, P3) 32
- Input port (Port P4) 4
- Serial I/O
  - 8-bit clock synchronous 1
  - 8-bit UART 1
  - Baud rate (at 7.37MHz frequency) ... 75bps~57600bps
  - (at 9.83MHz frequency) ... 75bps~76800bps
- A-D converter ..... 8-bit successive approximation
- PWM function 1
- Multiplex-type bus
  - Address bus 16
  - Data bus (multiplexed with lower address bus) 8

PIN CONFIGURATION (TOP VIEW)



Outline 64P4B



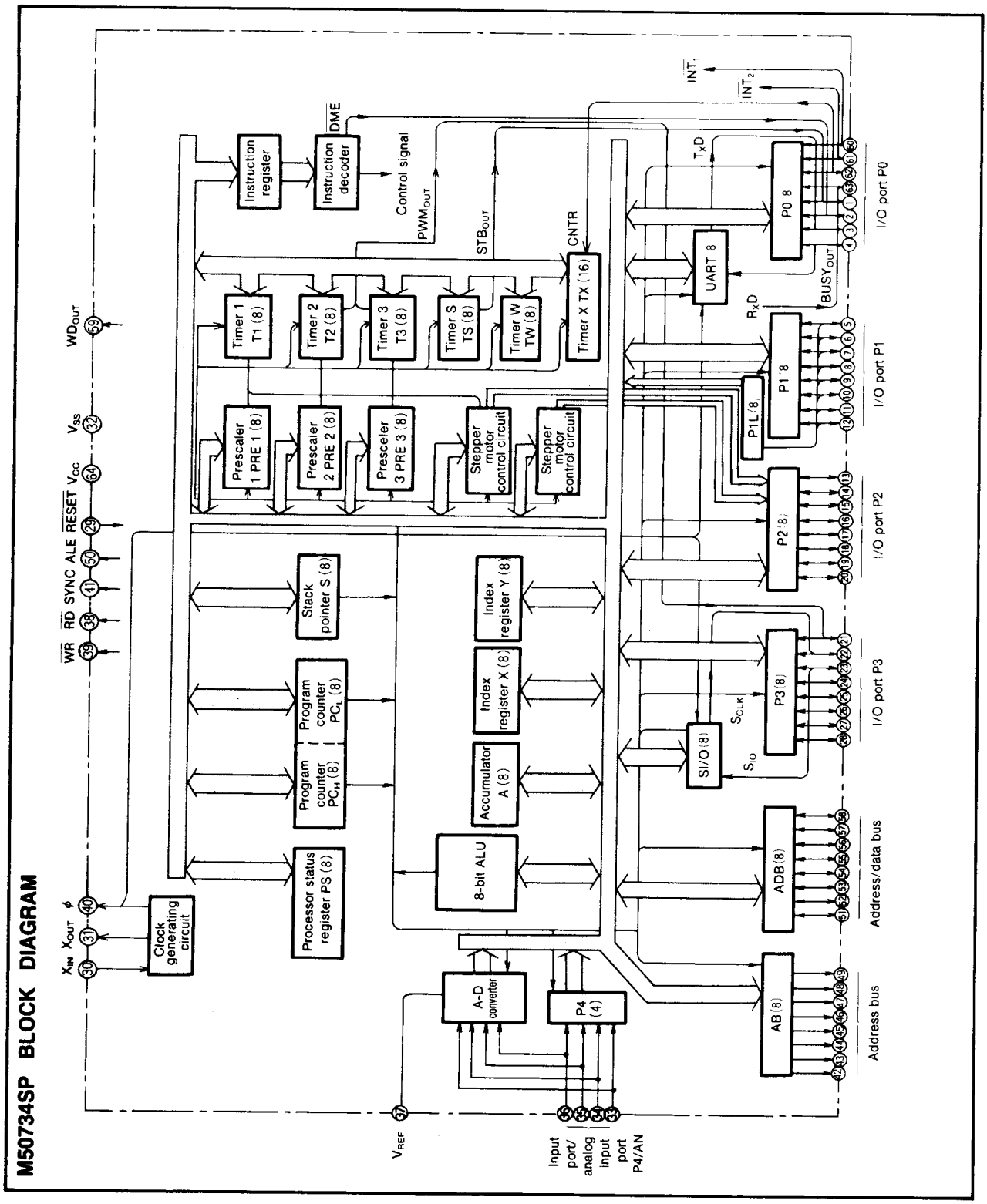
Outline 72P6

NC : No connection

APPLICATION

Printer/plotter, Electronic typewriter, PPC, FAX, Portable word processor, Robotics

M50734SP BLOCK DIAGRAM



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FUNCTIONS OF M50734SP and M50734SP-10

Parameter			Functions
Number of basic instructions			69
Instruction execution time	M50734SP		1μs (minimum instructions, at 8MHz frequency)
	M50734SP-10		0.8μs (minimum instructions, at 10MHz frequency)
Clock frequency	M50734SP		8MHz
	M50734SP-10		10MHz
Memory size			64K bytes (up to 128k bytes with $\overline{DME}$ signal)
Input/output ports	P0, P1, P2, P3	I/O	8-bit×4 (all pins of P0, P2, and part of P3 have double functions)
	P4	input	4-bit×1 (P4 is in common with analog input)
UART	M50734SP		1 (built-in baud rate generator 75~57600bps)
	M50734SP-10		1 (built-in baud rate generator 75~76800bps)
Clock synchronized serial I/O			8-bit×1
Timers	Timer X		16-bit×1
	Timer 1		8-bit×1 (with 8-bit prescaler)
	Timer 2		8-bit×1 (with 8-bit prescaler)
	Timer 3		8-bit×1 (with 8-bit prescaler)
	Timer S		8-bit×1 (with 1/4 frequency divider)
	Timer W		8-bit×1 (with 1/1024 frequency divider)
A-D converter			Four analog inputs, 8-bit successive approximation
Subroutine nesting			128 levels (max.)
Interrupt			Three external interrupts, four timer interrupts Two counter interrupts, one UART interrupt
Clock generating circuit			Built-in (externally connected to a ceramic resonater or a quartz crystal resonator)
Supply voltage			5V±10%
Power dissipation	at normal operation		30mW (M50734SP) 35mW (M50734SP-10)
	at wait mode		5mW
	at stop mode		5μW
Operating temperature range			−10~70℃
Device structure			CMOS sillicon gate process
Package	M50734SP, M50734SP-10		64-pin shrink plastic molded DIP
	M50734FP, M50734FP-10		72-pin plastic molded QFP

M50734SP ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}. Output transistors are at "off" state.	−0.3~7	V
V_I	Input voltage, $\overline{RESET}$, X_{IN}		−0.3~7	V
V_{REF}	Input voltage, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_3$, AD_0~AD_7, V_{REF}		−0.3~V_{CC}+0.3	V
V_O	Onput voltage, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, AD_0~AD_7, A_8~A_{15}, $\overline{RD}$, $\overline{WR}$, ϕ, SYNC, ALE, WD_{OUT}, X_{OUT}		−0.3~V_{CC}+0.3	V
P_d	Power dissipation	T_a=25℃	1000	mW
T_{opr}	Operating temperature		−10~70	℃
T_{stg}	Storage temperature		−40~125	℃

Note 1 : 300mW for QFP types.

RECOMMENDED OPERATING CONDITIONS

(V_{CC} = 5V±10%, V_{SS} = 0V, T_a = −10~70℃, f(X_{IN}) = 8MHz, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	"H" input voltage, $P0_0$~$P0_7$ (During using as a port), $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_3$, AD_0~AD_7	2.0		V_{CC}+0.3	V
V_{IH}	"H" input voltage, R_XD, CNTR, $\overline{INT_1}$, $\overline{INT_2}$, $\overline{RESET}$, X_{IN}	0.8V_{CC}		V_{CC}+0.3	V
V_{IL}	"L" input voltage, $P0_0$~$P0_7$ (During using as a port), $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_3$, AD_0~AD_7	−0.3		0.8	V
V_{IL}	"L" input voltage, R_XD, CNTR $\overline{INT_1}$, $\overline{INT_2}$	−0.3		0.2V_{CC}	V
V_{IL}	"L" input voltage, $\overline{RESET}$	−0.3		0.12V_{CC}	V
V_{IL}	"L" input voltage, X_{IN}	−0.3		0.16V_{CC}	V
V_{REF}	Standard voltage input	0.5V_{CC}		V_{CC}	V
V_{IA}	Analog input voltage, $P4_0$~$P4_3$	−0.3		V_{CC}+0.3	V
$I_{OL(perk)}$	"L" peak output current, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, AD_0~AD_7, A_8~A_{15}, $\overline{RD}$, $\overline{WR}$, ϕ, SYNC, ALE, WD_{OUT}			5	mA
$I_{OL(avg)}$	"L" average output current (Note1), $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, AD_0~AD_7, A_3~A_{15}, $\overline{RD}$, $\overline{WR}$, ϕ, SYNC ALE, WD_{OUT}			2	mA
$I_{OH(peak)1}$	"H" peak output current, $P0_0$~$P0_7$, AD_0~AD_7, A_8~A_{15}, $\overline{RD}$, $\overline{WR}$, ϕ, SYNC, ALE, WD_{OUT}			−5	mA
$I_{OH(peak)2}$	"H" peak output current, $P0_0$~$P0_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$			−10	mA
$I_{OH(avg)1}$	"H" average output current, (Note1) $P0_0$~$P0_7$, AD_0~AD_7, A_8~A_{15}, $\overline{RD}$, $\overline{WR}$, ϕ, SYNC, ALE, WD_{OUT}			−2	mA
$I_{OH(avg)2}$	"H" average output current, (Note1) $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$			−10	mA

Note 1 : $I_{OL(avg)}$, $I_{OH(avg)}$ is the average current in 100ms.

2 : The total of $I_{OL(peak)}$, of $P0_0$~$P0_7$, AD_0~AD_7, A_8~A_{15}, $\overline{RD}$, $\overline{WR}$, ϕ, SYNC, ALE and WD_{OUT} should be 80mA max

The total of $I_{OL(peak)}$, of $P1_0$~$P1_7$, $P2_0$~$P2_7$ and $P3_0$~$P3_7$ should be 80mA max

The total of $I_{OH(peak)}$, of $P0_0$~$P0_7$, AD_0~AD_7 and A_8~A_{15}, $\overline{RD}$, $\overline{WR}$, ϕ, SYNC, ALE and WD_{OUT} should be −60mA max

The total of $I_{OH(peak)}$, of $P1_0$~$P1_7$, $P2_0$~$P2_7$ and $P3_0$~$P3_7$ should be −80mA max

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±10%, V_{SS} = 0V, T_a = −10~70℃, f(X_{IN}) = 8MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output voltage all output pin except X_{OUT} pin	I_{OH} = −200μA	2.4			V
		I_{OH} = −10μA	V_{CC}−0.7			
V_{OL}	"H" output voltage all output pin except X_{OUT} pin	I_{OL} = 1.6mA			0.5	V
I_I	Input leak current, $P0_0$~$P4_3$, $\overline{RESET}$	$V_{SS} \leqq V_I \leqq V_{CC}$	−5		5	μA
I_{OZ}	Three state leak current, all input/output pin	V_{SS} + 0.5V ≦ V_O ≦ V_{CC} − 0.5V	−5		5	μA
$V_{T+}-V_{T-}$	Hysteresis width, $\overline{INT_1}$, $\overline{INT_2}$, CNTR, R_XD, $\overline{RESET}$	When used as function except port		0.6		V
I_{OH}	"H" output current, $P2_0$~$P2_7$	V_{OH} = 1.5V	−1		−10	mA
I_{CC}	Supply current	During operating (Output transistors cut-off)		6	15	mA
		Wait mode (Output transistors cut-off)		1	3	
		Stop mode (Output transistors cut-off)		1	20	μA
I_{ACC}	A/D supply current	During executing A/D convert			6	mA

TIMING REQUIREMENTS (V_{CC} = 5V±10%, T_a = −10~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{SU(D-\phi)}$	Data input set-up time	Fig.32	80			ns
$t_{SU(P0-\phi)}$	Port P0 input set-up time		250			ns
$t_{SU(P1-\phi)}$	Port P1 input set-up time		250			ns
$t_{SU(P2-\phi)}$	Port P2 input set-up time		250			ns
$t_{SU(P3-\phi)}$	Port P3 input set-up time		250			ns
$t_{SU(P4-\phi)}$	Port P4 input set-up time		250			ns
$t_{SU(P1-\overline{INT_1})}$	Port P1 latch input set-up time		250			ns
$t_{SU(S_{IN}-S_{CLK})}$	Serial input set-up time		250			ns
$t_{h(\phi-D)}$	Data input hold time		0			ns
$t_{h(\phi-P0)}$	Port P0 input hold time		50			ns
$t_{h(\phi-P1)}$	Port P1 input hold time		50			ns
$t_{h(\phi-P2)}$	Port P2 input hold time		50			ns
$t_{h(\phi-P3)}$	Port P3 input hold time		50			ns
$t_{h(\phi-P4)}$	Port P4 input hold time		50			ns
$t_{h(\overline{INT_1}-P1)}$	Port P1 latch input hold time		50			nS
$t_{h(S_{CLK}-S_{IN})}$	Serial input hold time		50			ns
$t_{WL(\overline{INT_1})}$	$\overline{INT_1}$ input "L" pulse width		250			ns
$t_{WL(\overline{INT_2})}$	$\overline{INT_2}$ input "L" pulse width		1			μs
$t_{WL(CNTR)}$	CNTR input "L" pulse width		1			μs
$t_{WH(\overline{INT_1})}$	$\overline{INT_1}$ input "H" pulse width		1			μs
$t_{WH(\overline{INT_2})}$	$\overline{INT_2}$ input "H" pulse width		1			μs
$t_{WH(CNTR)}$	CNTR input "H" pulse width		1			μs
$t_{C(X_{IN})}$	External clock input cycle time		125			ns
$t_{WL(X_{IN})}$	External clock input "L" pulse width		45			ns
$t_{WH(X_{IN})}$	External clock input "H" pulse width		45			ns
$t_{W(\overline{RESET})}$	$\overline{RESET}$ input "L" pulse width		2			μs

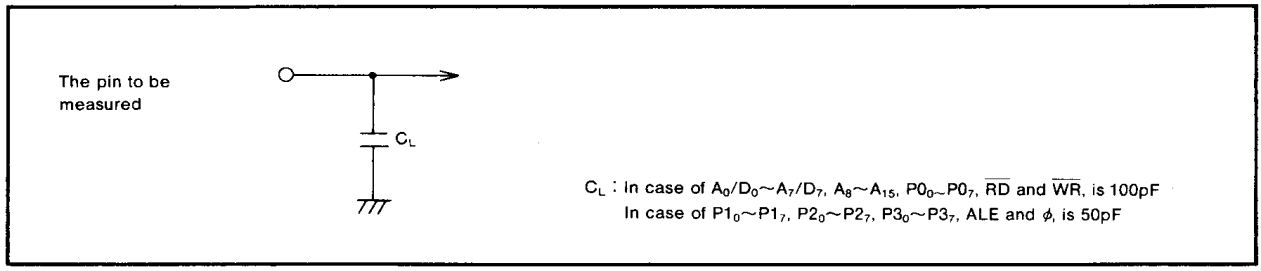

Fig.32 Measurement circuit diagram

SWITCHING CHARACTERISTICS (V_{CC} = 5V±10%, T_a = −10~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
*$t_{C(\phi)}$	Cycle time (Note 6)	Fig.32	500			ns
*$t_{WH(\phi)}$	ϕ clock pulse width (High level) (Note 2)		220			ns
*$t_{WL(\phi)}$	ϕ clock pulse width (Low level) (Note 2)		220			ns
$t_{r(\phi)}$	ϕ clock rising edge time				30	ns
$t_{f(\phi)}$	ϕ clock falling edge time				30	ns
*$t_{d(\phi-ALE)}$	Address strobe pulse delay time (Note 4)				60	ns
*$t_{W(ALE)}$	Address strobe pulse width (Note 3)		100			ns
$t_{d(A-ALE)}$	Address-ALE delay time		30			ns
$t_{V(ALE-A)}$	Address effective time after ALE		30			ns
$t_{d1(\phi-A)}$	Address delay time 1				130	ns
*$t_{d2(\phi-A)}$	Address delay time 2 (Note 1)				150	ns
$t_{V(\phi-A)}$	Address effective time after ϕ		10			ns
*$t_{W(RD)}$	$\overline{RD}$, $\overline{WR}$ pulse width (Note 2)		220			ns
$t_{d(\phi-RD)}$	$\overline{RD}$, $\overline{WR}$ delay time				20	ns
$t_{V(\phi-RD)}$	$\overline{RD}$, $\overline{WR}$ effective time after ϕ				10	ns
$t_{d(AZ-RD)}$	address floating-$\overline{RD}$ delay time		0			ns
$t_{d(\phi-D)}$	Data delay time (write cycle)				150	ns
*$t_{V(\phi-D)}$	Data effective time after ϕ (Note 5)		40			ns
$t_{d(\phi-P0)}$	Port P0 data output delay time				250	ns
$t_{d(\phi-P1)}$	Port P1 data output delay time				250	ns
$t_{d(\phi-P2)}$	Port P2 data output delay time				250	ns
$t_{d(\phi-P3)}$	Port P3 data output delay time				250	ns
$t_{d(\phi-S_{CLK})}$	Serial clock delay time				60	ns
$t_{V(\phi-S_{CLK})}$	Serial clock effective time after ϕ				40	ns
$t_{d(S_{CLK}-S_{OUT})}$	Serial output delay time				150	ns
$t_{V(S_{CLK}-S_{OUT})}$	Serial output effective time after serial clock		0			ns
$t_{d(\overline{INT_1}-BSY)}$	Busy output delay time				250	ns

※ This timing is changed by $t_C(X_{IN})$, The timing of this list is the value in $t_C(X_{IN})$ = 125ns

Note 1 : This value is defined as follows : $t_{dz}(\phi-A)=t_C(\phi)/8+8.75$
2 : This value is defined as follows : $t_W(RD)=t_C(\phi)/2-30$
3 : This value is defined as follows : $t_W(ALE)=t_C(\phi)/4-25$
4 : This value is defined as follows : $t_d(\phi-ALE)=t_C(\phi)/8-2.5$
5 : This value is defined as follows : $t_V(\phi-D)=t_C(\phi)/8-22.5$
6 : This value is defined as follows : $t_C(\phi)=4t_C(X_{IN})$

A-D CONVERTER CHARACTERISTICS (V_{CC}=5V±10%, V_{SS}=0V, T_a=−10~70℃, f(X_{IN})=8MHz, unless otherwise noded)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution		8			Bits
—	Absolute accuracy	$V_{CC}=V_{REF}$=5.12V		±1 1/2	±3	LSB
R_{LADDER}	Ladder resistance value		1			KΩ
t_{CONV}	Conversion time				36	μs
$I_{I(AD)}$	Input current in A-D convert	$0 \leq V_I \leq V_{REF}$			50	μA