

M51279SP/FP

NTSC/PAL DECODER

DESCRIPTION

The M51279SP/FP is a semiconductor integrated circuit designed for color signal processing, suitable for both NTSC and PAL systems. The outputs are R-Y and B-Y color difference signals, and the circuit has R-Y and B-Y output demodulation carriers. These carriers are also useful for modulating the color difference signals of another semiconductor integrated circuit, the M51272P/FP.

The M51279SP/FP consists of sync separator, ACC, tint control, APC and chroma demodulators.

Note that there is a burst signal at the ACC output in the M51279SP/FP, but not in the M51271SP/FP.

With respect to all other functions however, they are identical.

FEATURES

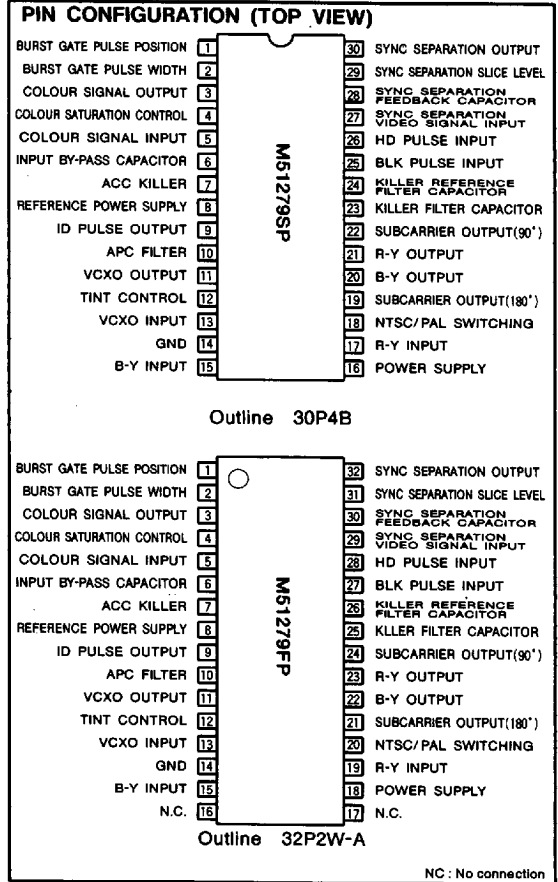
- Low power dissipation ($V_{cc}=5.0V$, $I_{cc}=50mA$ typ.)
- The demodulating angles for R-Y and B-Y are formed from a 4 fsc oscillator, so accurate that 90 deg demodulation is possible.
- Mute R-Y and B-Y output capability using external blanking pulse.
- Built-in ID pulse (for PAL) output.
- Individual burst gate pulse position and width set up capability using external constants.

APPLICATION

Color TV sets and VCRs.

RECOMMENDED OPERATING CONDITION

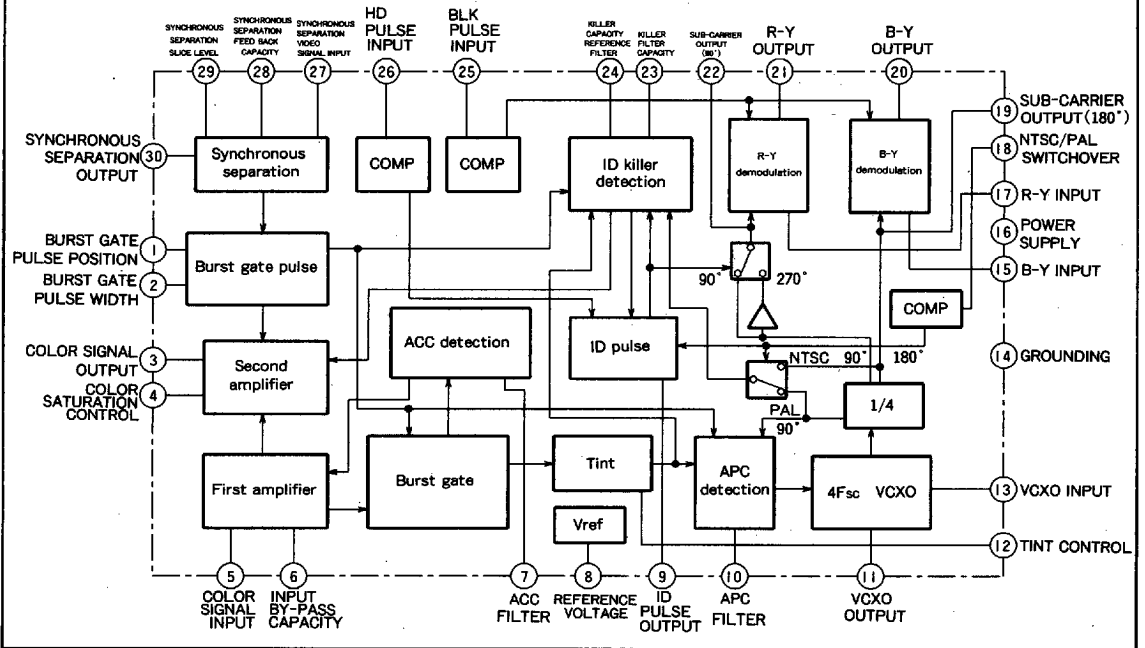
Supply voltage range.....4.0~6.0V
 Rated supply voltage.....5.0V



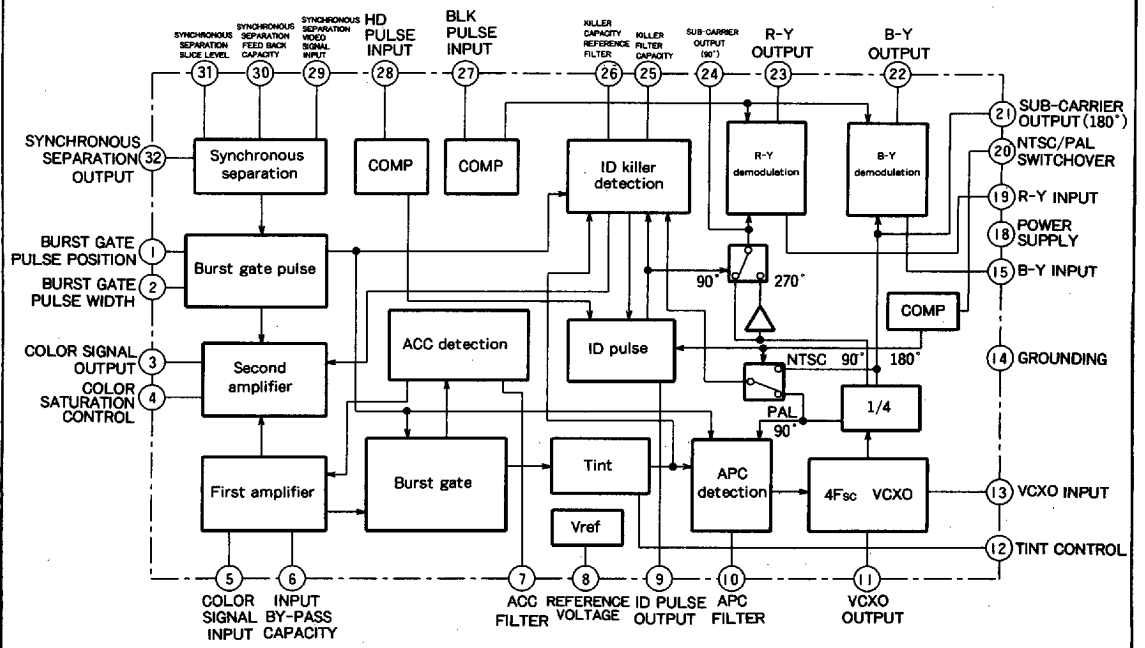
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BLOCK DIAGRAM (M51279SP)



BLOCK DIAGRAM (M51279FP)



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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Ratings	Unit
V _{cc}	Supply voltage	6	V
P _d	Power consumption	1.25(0.5)	W
T _{opr}	Operating temperature	-20~75	°C
T _{stg}	Storing ambient temperature	-40~125	°C
K _e	Heat reduction rate	12.5(5)	mW/°C

Note: Numerical values in () are FP version.

ELECTRICAL CHARACTERISTICS (T_a=25°C, V_{cc}=5.0V, unless otherwise noted)

DC CHARACTERISTICS

(PIN No. are M51279SP)

Symbol	Parameter	Test conditions	Test circuit	Limits			Unit
				Min.	Typ.	Max.	
I _{cc}	Circuit current	DC bias alone	A	40	50	60	mA
V ₁	Voltage at terminal 1	DC bias alone		2.6	2.9	3.2	V
V ₃	Voltage at terminal 3	DC bias alone		1.9	2.2	2.5	V
V ₄	Voltage at terminal 4	DC bias alone		2.3	2.5	2.7	V
V ₆	Voltage at terminal 6	DC bias alone		2.8	3.0	3.2	V
V ₇	Voltage at terminal 7	DC bias alone		4.4	4.7	5.0	V
V ₈	Voltage at terminal 8	DC bias alone		2.8	3.0	3.2	V
V ₁₀	Voltage at terminal 10	DC bias alone		2.6	2.9	3.2	V
V ₁₁	Voltage at terminal 11	DC bias alone		2.4	2.7	3.0	V
V ₁₂	Voltage at terminal 12	DC bias alone		2.3	2.5	2.7	V
V ₁₃	Voltage at terminal 13	DC bias alone		3.1	3.4	3.7	V
V ₁₅	Voltage at terminal 15	DC bias alone		2.6	2.9	3.2	V
V ₁₇	Voltage at terminal 17	DC bias alone		2.6	2.9	3.2	V
V ₁₈	Voltage at terminal 18	DC bias alone		0.6	0.8	1.0	V
V ₂₀	Voltage at terminal 20	DC bias alone		1.9	2.1	2.3	V
V ₂₁	Voltage at terminal 21	DC bias alone		1.9	2.1	2.3	V
V ₂₄	Voltage at terminal 24	DC bias alone		2.5	2.8	3.1	V
V ₂₇	Voltage at terminal 27	DC bias alone		2.6	2.9	3.2	V
V ₂₈	Voltage at terminal 28	DC bias alone		2.2	2.5	2.8	V
V ₂₉	Voltage at terminal 29	DC bias alone		2.2	2.5	2.8	V

INPUT TERMINAL CHARACTERISTICS

Pin No.	Input form	Internal bias voltage (standard)	Test conditions	Input resistance or current standard value			Unit
				Min.	Typ.	Max.	
②	Open base (PNP)	Not specified	V ₂ =2.5V	-2.0	-1.0	—	μA
④	Resistor	2.5V	—	20.0	25.0	30.0	kΩ
⑤	Open base (NPN)	Not specified	V ₅ =3.0V	—	1.0	2.0	μA
⑥	Resistor	3.0V	—	9.0	12.0	15.0	kΩ
⑫	Resistor	2.5V	—	20.0	25.0	30.0	kΩ
⑬	Resistor	3.4V	—	4.0	5.0	6.0	kΩ
⑮	Resistor	2.9V	—	4.0	5.0	6.0	kΩ
⑰	Resistor	2.9V	—	4.0	5.0	6.0	kΩ
⑳	Open base (NPN)	Not specified	V ₂₅ =5.0V	—	0.5	1.0	μA
㉑	Open base (NPN)	Not specified	V ₂₆ =5.0V	—	0.5	1.0	μA
㉒	Resistor	2.9V	—	16.0	20.0	24.0	kΩ

OUTPUT TERMINAL CHARACTERISTICS

Pin No.	Output form	Test conditions	Bias current			Unit
			Min.	Typ.	Max.	
③	Emitter follower (NPN)	Ammeter between ③ pin and V _{cc}	0.6	0.8	1.0	mA
⑪	Emitter follower (NPN)	Ammeter between ⑪ pin and V _{cc}	1.5	1.8	2.1	mA
⑲	Emitter follower (NPN)	Ammeter between ⑲ pin and V _{cc}	230	280	330	μA
㉐	Emitter follower (NPN)	Ammeter between ㉐ pin and V _{cc}	0.8	1.0	1.2	mA
㉑	Emitter follower (NPN)	Ammeter between ㉑ pin and V _{cc}	0.8	1.0	1.2	mA
㉒	Emitter follower (NPN)	Ammeter between ㉒ pin and V _{cc}	230	280	330	μA

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AC CHARACTERISTICS

Symbol	Parameter	Test conditions	Test circuit	Limits			Unit	
				Min.	Typ.	Max.		
V _{CCR}	Operating supply voltage range	The standard application circuit should have no abnormal operation		4.0	5.0	6.0	V	
Acc I	ACC characteristics	ACC characteristics I SG1 : 200mV Reference value determined by measuring output value when inputting 100mV signal from SG1.	B	0	1.0	3.0	dB	
Acc II		ACC characteristics II SG1 : 10mV Reference value determined by measuring output value when inputting 100mV signal from SG1.		-2.0	0	2.0	dB	
G _{CA}	Open-loop gain	SG1 5mV _{P-P} SW 7 ON		21.0	24.0	27.0	dB	
V _{cm}	Color control	Chroma maximum output amplitude		④pin 5V	160	200	240	mV _{P-P}
V _{ctyp}		Chroma typical output amplitude		④pin open	80	100	120	mV _{P-P}
V _{cm}		Chroma maximum attenuation		④pin GND	—	—	-35	dB
S _{d1}	Synchronous separation	Synchronous output delay 1		SG2 APL100% 500mV _{P-P}	—	—	500	ns
S _{d2}		Synchronous output delay 2		SG2 APL100% 500mV _{P-P}	—	—	500	ns
S _{v1}		Synchronous output amplitude 1		SG2 APL100% 500mV _{P-P}	4.0	4.2	4.4	V
S _{min}		Synchronous separation minimum input level		SG2 : APL100% Signal attenuation	—	—	350	mV _{P-P}
NC		Synchronous separation noise cancel		SG3 input	—	—	1.2	V
BGPp I		Burst gate pulse generator		Burst gate pulse position I	①pin 10kΩ, pull up=560kΩ ②pin 3.0V	2.0	2.5	3.0
BGPp II	Burst gate pulse position II		①pin 39kΩ, pull up=2.2MΩ ②pin 3.0V	8.0	8.5	9.0	μS	
BGPw I	Burst gate pulse width I		①pin 24kΩ, pull up=1.2MΩ ②pin 2.0V	3.5	4.0	4.5	μS	
BGPp II	Burst gate pulse width II		①pin 24kΩ, pull up=1.2MΩ ②pin 4.0V	0.8	1.3	1.8	μS	
G _{dr-y}	R-Y demodulator	Demodulation gain	SG5 100mV _{P-P} f (beat)=10kHz	10	12	14	dB	
ΔE _{r-y}		Residual carrier wave	No input at 17pin	—	—	30.0	mV _{P-P}	
V _{mr-y}		Demodulation maximum output	SG5 600mV _{P-P} f (beat)=10kHz	2.1	2.4	2.7	V _{P-P}	
B _{wr-y}	B-Y demodulator	Demodulation band width	Reference : f (beat) =10kHz Measuring point : f (beat) of -3dB	1.0	—	—	MHz	
BLK Δ _{vr}		Blanking DC offset	⑤pin 0V, 5V : ①pin DC fluctuation	—	—	50.0	mV _{P-P}	
G _{db-y}		Demodulation gain	SG5 100mV _{P-P} f (beat)=10kHz	10	12	14	dB	
ΔE _{b-y}	Demodulator	Residual carrier wave	No input 15pin	—	—	30.0	mV _{P-P}	
V _{mb-y}		Demodulation maximum output	SG5 600mV _{P-P} f (beat)=10kHz	2.1	2.4	2.7	V _{P-P}	
B _{Wb-y}		Demodulation band width	Reference : f (beat) =10kHz f (beat) of -3dB	1.0	—	—	MHz	
BLK Δ _{vb}	Blanking DC offset	⑤pin 0V, 5V, ①pin DC fluctuation	—	—	50.0	mV		
R-Y	Demodulator	R-Y, B-Y demodulation gain ratio	—	0.8	1.0	1.2	—	
ΔV		R-Y, B-Y DC voltage offset	DC difference between output values at pin④ and pin②	—	—	50.0	mV	

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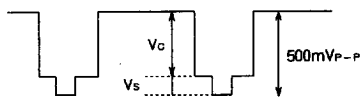
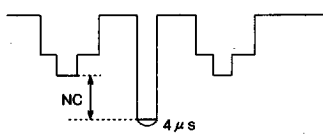
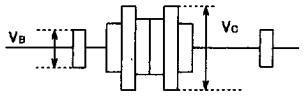

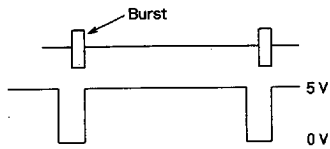
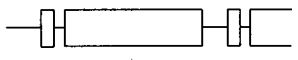
AC CHARACTERISTICS (cont.)

Symbol	Parameter		Test conditions	Test circuit	Limits			Unit
					Min.	Typ.	Max.	
TCP	TINT	PAL Center	Measure the value of V12 when output of ⑩ pin crosses 0.	C	2.30	2.35	2.40	V
TWP			Variable width		Measure the amount of phase shift when voltage at ⑩ pin changes between 0V and 5V.	80	85	—
TcN	NTSC	Center	—		2.40	2.45	2.50	V
TWN			Variable width		—	80	85	—
Kthp		Killer operation input level	Burst voltage 100mV _{p-p} is 0dB.		-33	-30	-27	dB
Kthn			Killer operation input level		Burst voltage 100mV _{p-p} is 0dB.	-36	-33	-30
ID	ID operation		Observe R-Y output (21pin).		There shall be no abnormality in operation.			
IDP	ID pulse output	ID pulse	—		There shall be no abnormality in operation.			
IDv		ID vsat	SW18 : OFF open collector Vsat DC 5mA		—	250	500	mV
BLKth	Blanking pulse input threshold		⑩pin DC variable		3.3	3.5	3.7	V
HDth	HD pulse input threshold		⑩pin DC variable	3.8	4.0	4.2	V	
SCob	S-C Sub-carrier Orthogonality	Output level	⑩pin output	500	550	600	mV _{p-p}	
SCdb		Duty	⑩pin output	45	50	55	%	
SCor		Output level	⑪pin output	500	550	600	mV _{p-p}	
SCdr		Duty	⑪pin output	45	50	55	%	
Or-y,b-y	Sub-carrier orthogonality		Phase difference between output carrier of ⑩pin and of ⑪pin	85	90	95	deg	
FCPP	PAL frequency-locking range		⑩pin input frequency variable	1.0	—	—	kHz	
FCPN	NTSC frequency-locking range		⑩pin input frequency variable	1.0	—	—	kHz	

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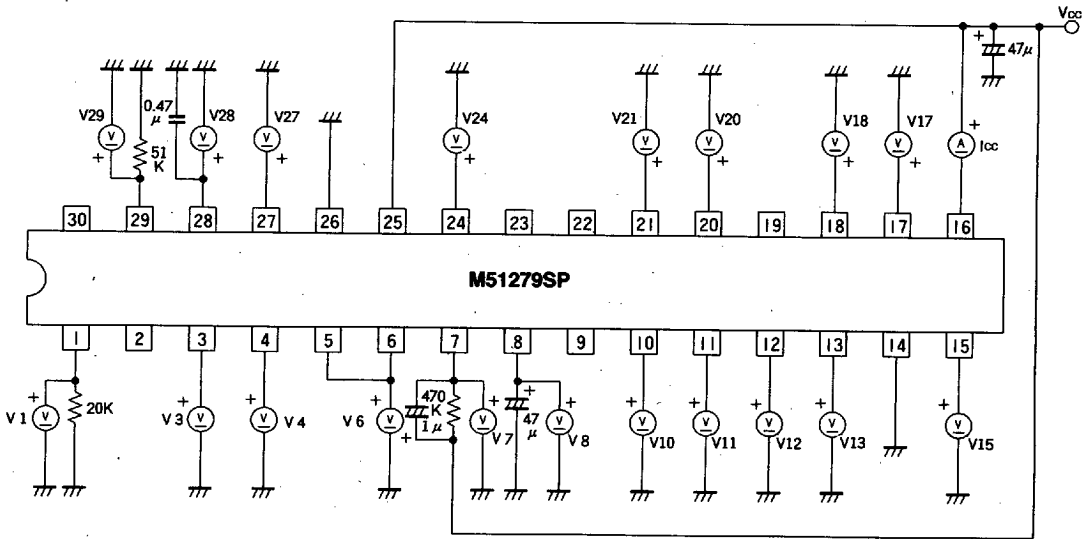


INPUT SIGNAL

SG No.	Waveform	Standard	Remarks
SG1	 <p>3.579545MHz 4.433618MHz</p>	Sine wave CW, 100mV _{P-P} (standard)	Frequency and output level should be variable.
SG2	 <p>500mV_{P-P}</p>	APL100 signal 500mV _{P-P} (standard), V _c : V _s = 10 : 4	Level should be variable.
SG3	 <p>4µs</p>	Mix noise to SG2 standard signal (500mV _{P-P}).	NC should be variable (noise level alone).
SG4	 <p>NTSC, PAL chroma standard signal</p>	V _c : V _b = 2 : 1, V _b = 100mV _{P-P} (standard)	Level shall be variable.
SG5	 <p>3 ~ 5 MHz 0 ~ 1 V_{P-P}</p>	Sine wave CW	Frequency and output level should be variable.
HD pulse	 <p>Burst</p> <p>5V 0V</p>	Pulse should have last transition preceding the burst in horizontal blanking interval.	Vertical blanking interval should also appear with the same timing
SG6		Burst and chroma should show the same phase. Amplitude ratio of burst and chroma can take any value. Burst : 100mV _{P-P}	Frequency : 3.579545MHz 4.433618MHz

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TEST CIRCUIT A

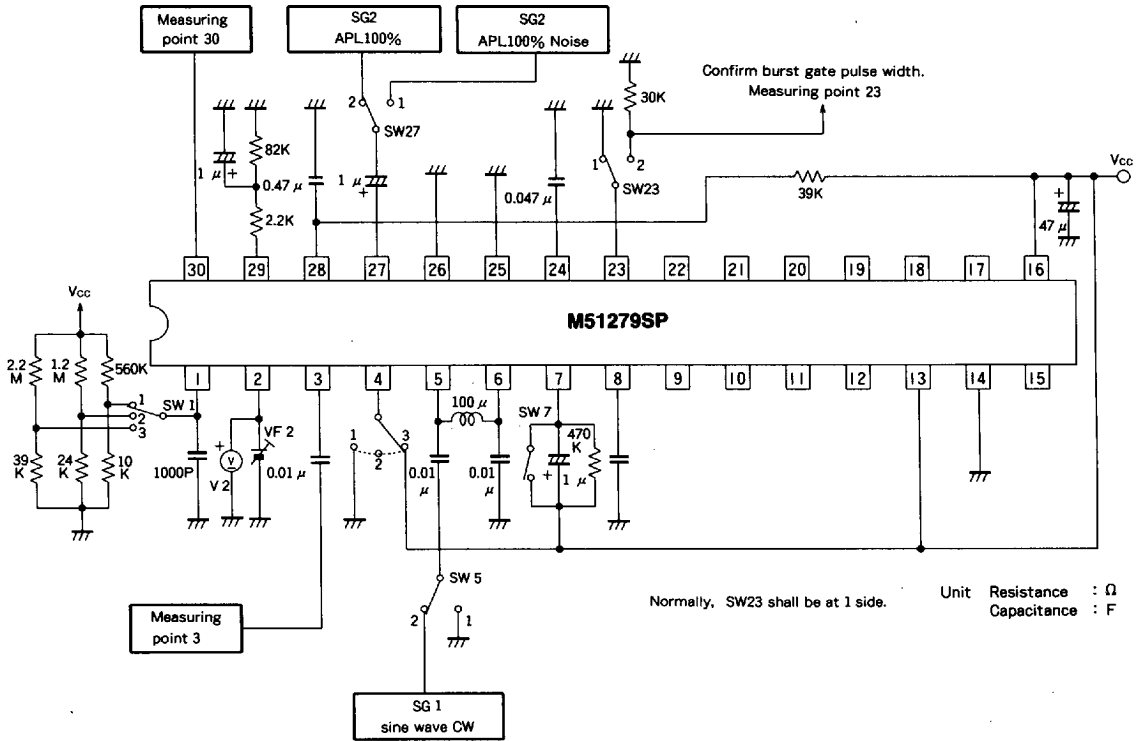


At each measuring point, the measured value is the value read from an ammeter or voltmeter.

Unit Resistance : Ω
Capacitance : F

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TEST CIRCUIT B



ACCI and ACCII

Set SW1, 5 and 27 to 2; SW4 to 3, and turn off SW7. Input 3.57954MHz, 100mVp-p (odB) from SG1. Adjust VF2 (to approximately 3V) so that burst gate pulse width will be set in 2.8μs (burst, is approximately 10 cycles). (Check the burst gate pulse generator section to confirm burst gate pulse width).

In the following equations, V_A (mVp-p) represents the output value at the measuring point under the above conditions. V_b (mVp-p) and V_c (mVp-p) represent output values at measuring point 3: the former, when the output from SG1 is 6dB; and the latter, when the same output is -20dB.

$$ACCI = 20 \log V_b/V_A \text{ (dB)} \quad ACCII = 20 \log V_c/V_A \text{ (dB)}$$

Gca

Turn SW7 on. Set the other SWs to the same conditions specified in 1).

Set the output of SG1 to 3.579545MHz, 5mVp-p. In the following equation, V_D (mVp-p) represents the output value at measuring

point 3.

$$G_{CA} = 20 \log V_D/5 \text{ (dB)} \text{ (Burst gate pulse } 2.8\mu\text{s)}$$

Vcmax, Vctyp and Vcmin

Set the SWs to the same conditions specified in 1).

Set the output of SG1 to 3.579545MHz, 100mVp-p. V_{cmax} , V_{ctyp} and C (mVp-p) represent the output amplitude values at measuring point 3 when SW4 is set to 3, 2 and 1 respectively. V_{cmin} is obtained by the following equation.

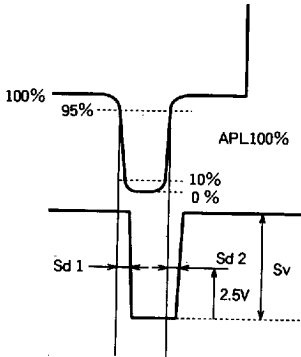
$$V_{cmin} = 20 \log C/V_{cmax} \text{ (dB)} \text{ (Burst gate pulse } 2.8\mu\text{s)}$$

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Sd1, Sd2 and Sv

Set SW27 to 2. The other SWs can be set to any position. Input an APL 100% standard signal from SG2 (500mVp-p). Determine Sd1, Sd2 and Sv, shown in the right-hand figure, by observing the input signal and synchronizing pulse output at measuring point 30.

**Smin**

Under the same conditions specified in 4), reduce the output of SG2. Smin (mVp-p) represents the output value of SG2 just before the output values at measuring point 30 begin to deviate from the standard values for Sd1, Sd2 and Sv

NC

Set SW27 to 1. Set other SWs to the same conditions specified in 4). Vary the noise pulse level of SG3. NC(V) represents the potential difference between the input synchronizing tip and the noise pulse tip when the noise pulse at measuring point 30 begins to fall away.

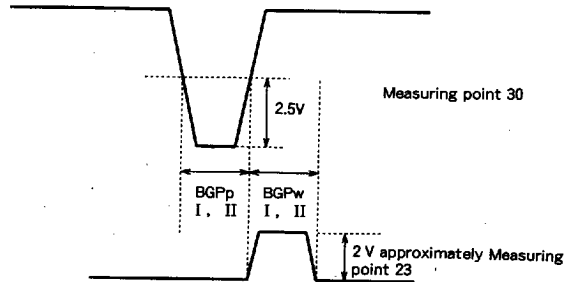
BGPp I and BGPp II

Set SW7 to 2. Input an APL 100% standard signal from SG2. Set SW23 to 2 and observe measuring point 23 and 30. Set SW1 to 1 then to 3 and measure BGPp I and BGPp II. ($V_2=3V$)

BGPw I and BGPw II

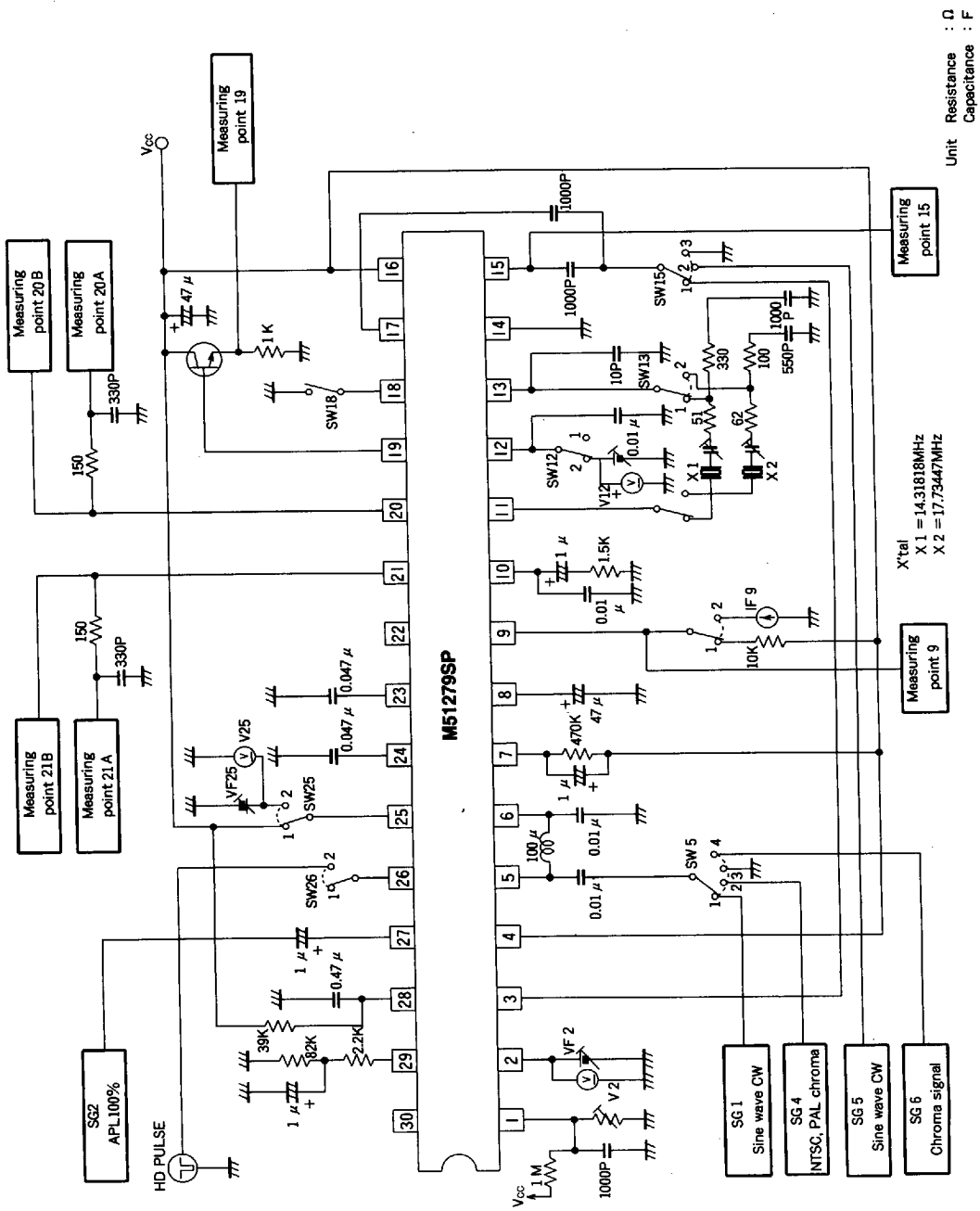
Set SW1 to 2; and the other SWs to the same conditions specified in 7).

Set V2 to 2.0V then to 4.0V and measure BGPwI and BGPw II at measuring point 23.



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TEST CIRCUIT C



Unit Resistance : Ω
Capacitance : F

X^{Tal}
X1 = 14.31818MHz
X2 = 17.73447MHz

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ADJUSTMENT OF BURST PULSE POSITION AND WIDTH

On inputting NTSC/PAL standard chroma signals, adjust the resistance value at terminal 1 and the voltage value at terminal 2 in order to locate the burst gate pulse at the burst position and observe measuring point 3.

In other cases, set the resistance value at terminal 1 to 24k Ω . Vary the burst gate width in 2.8 μ s when setting conditions for NTSC, in 2.3 μ s when setting conditions for PAL by adjusting the voltage at terminal 2.

(Observation has already occurred in 10-2) with SW23 set to 2).

VCXO TO ADJUSTMENT

Set SW5 to 3, SW25 and 26 to 1, and turn SW18 on (for PAL). Apply an APL100% standard signal from SG2. Adjust the VCXO external trimmer to set output frequency at measuring point 19 to :

3.579545MHz (NTSC, set SW13 to 1)

4.433618MHz (PAL, set SW13 to 2).

Gdb-y and Gdr-y

Set SW5, 12, 13, 25 and 26 to 1; SW15 to 2, and turn off SW18. Input 3.579545MHz, 100mVp-p from SG1, an APL100% standard signal from SG2, and 3.589545MHz, 100mVp-p from SG3. In the following equation, DB (mVp-p) and DR (mVp-p) represent output (f(beat)=10kHz) at measuring points 20A and 21A respectively.

$$Gdb - y = 20 \log DB / 100 \text{ (dB)}$$

$$Gdr - y = 20 \log DR / 100 \text{ (dB)}$$

Δ Eb-y and Δ Er-y

Set SW15 to 3, and other SWs and SG1 and 2 to the same conditions specified in 1). Δ Eb-y (mVp-p) and Δ Er-y (mVp-p) represent carrier leakage output values (3.58MHz component) at measuring points 20B and 21B respectively.

Vmb-y and Vmr-y

Set each SW, and SG1 and 2 to the same conditions specified in 1). Set the output of SG3 to 600mVp-p and measure output values (f(beat)=10kHz) at measuring points 20A and 21A. The values are represented by Vmb-y and Vmr-y (Vp-p) respectively.

BWb-y and BWr-y

Set each SW, and SG1 and 2 to the same conditions specified in 1). Vary the output frequency of SG3 from 3.58 to 5MHz with its voltage set to 100mVp-p. BWb-y and BWr-y (MHz) represent output frequency at measuring points 20A and 21A respectively when the output voltage at both measuring points is -3dB (reference is DB or DR).

BLK Δ vb and BLK Δ vr

Set SW15 to 3, SW25 to 2, and other SWs and SG1 to the same conditions specified in 1). BLK Δ vb represents DC voltage fluctuation at measuring point 20B when VF25 is set to 5.0V and then 0V. Measure BLK Δ vr similarly at measuring point 2NB.

R-Y, B-Y demodulation gain ratio

From DB and DR obtained by measurement of Gdb-y and Gdr-y, we obtain the following equation.

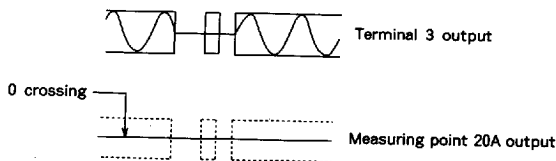
$$(R-Y) / (B-Y) = DR / DB$$

Δ V

Δ V represents the potential difference between measuring points 20A and 21A obtained by measurement of BLK Δ vb and BLK Δ vr when VF25 is set to 5.0V.

Tcp and Tcn

Set SW15, 25 and 26 to 1, SW12 and 13 to 2, SW5 to 4, and turn off SW18. Input 4.433618MHz from SG6. Vary the voltage of VF12. Tcp represents the voltage of V12(V) when the output at measuring point 12A passes 0. Set SW13 to 1 and input 3.579545MHz from SG6. Measure Tcn similarly.



Twp and TwN

Set SW5, 15, 25 and 26 to 1; SW12 and 13 to 2, and turn off SW18. Input 4.433618MHz, 100mVp-p from SG1. Twp (deg) represents the amount of phase shift of the output at measuring point 19 compared with that at measuring point 15 when VF12 is set at 5.0 and then 0V. Set SW13 to 1 and input 3.579545MHz, 100mVp-p from SG1. Measure TwN (deg) similarly.

KthP and KthN

Set SW5, 13 and 26 to 2; SW12, 15 and 25 to 1, and turn SW18 on. Input the PAL chroma standard signal from SG4. Start reducing the output from SG4. In the following equation, Vkp (mVp-p) represents the burst width of the SG4 output when the color difference signal output at measuring point 20A begins to muted.

$$KthP = 20 \log Vkd / 100 \text{ (dB)}$$

Set SW13 and 26 to 1 and turn off SW18. Input the NTSC chroma standard signal from SG4. Vkn is determined similarly, and we obtain the following equation.

$$KthN = 20 \log Vkn / 100 \text{ (dB)}$$

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ID operation

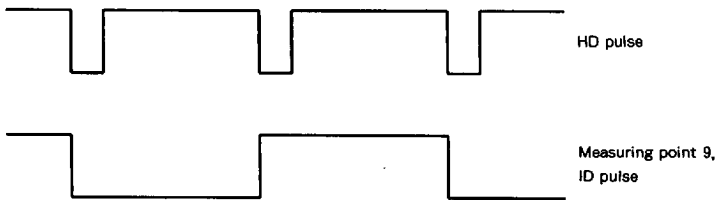
Under the same measuring conditions as specified for the measurement of Kthp, input the PAL chroma standard signal from SG4. Confirm that the color difference signal is not reversed every 1H at measuring point 21A for R-Y output.

BLKth

Set SW25 to 2 and other SWs and SGs to the same conditions specified for the measurement of Kthp. Slowly reduce the VF25 voltage from 5.0V. BLKth represents the voltage of V25 (V) when color difference output at measuring points 20A and 21A begins to be muted.

ID pulse

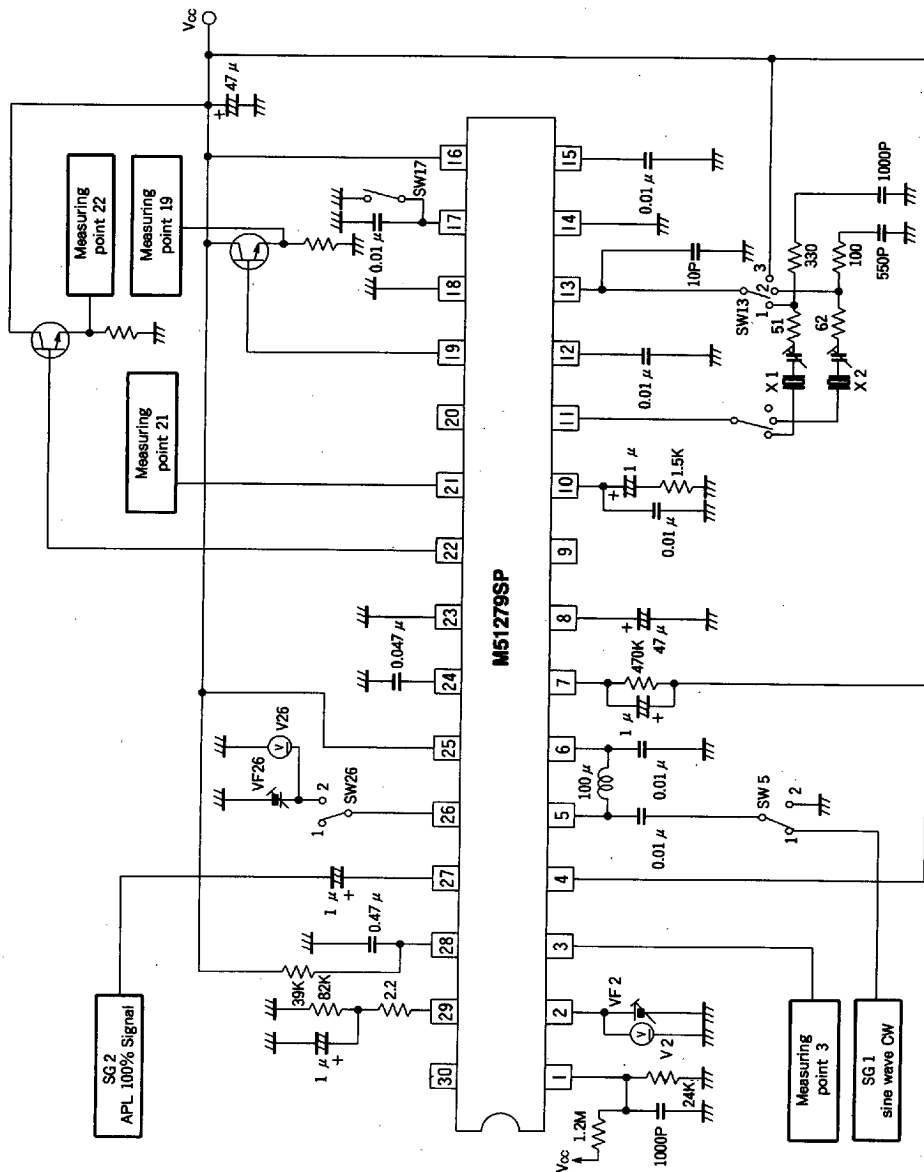
Under the same measuring conditions specified for the measurement of Kthp, input the PAL chroma standard signal from SG4. Set SW9 to 1. Observe the pulse output at measuring point 9. Confirm that the leading edge of the HD pulse is reversed and has 1/2 dividing.

**IDvsat**

Under the same measuring conditions specified for the measurement of KthN, set SW9 to 2. IDvsat (mV) represents the DC voltage at measuring point 9 when 5mA is applied from IF9.

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TEST CIRCUIT D



X'tal
 X1 = 14.31818MHz
 X2 = 17.73447MHz

Unit Resistance : Ω
 Capacitance : F

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HDth

Set SW5 and 26 to 2, SW13 to 3, and turn SW17 on. Start reducing the voltage at VF25 slowly from 5.0V. HDth (V) represents VF26 voltage when DC voltage at measuring point 21 changes either from High (4V approximately) to Low (0V approximately) or similarly but in the opposite direction.

obtain the following equation.

$$F_{cPN} = f_3 - f_4 \text{ (Hz)}$$

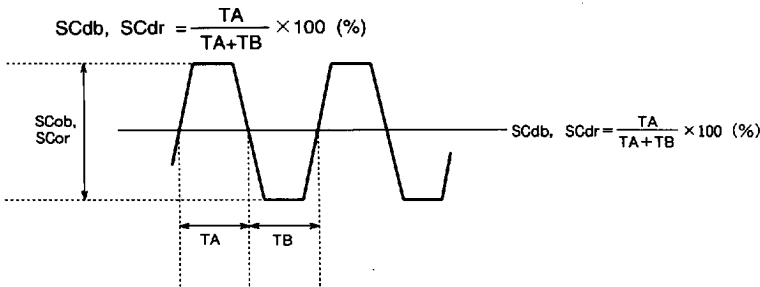
*Please refer to Application note in M51271SP/FP

SCob and SCor

Set SW5 and 26 to 1, SW13 to 2, and turn off SW17. Input 4.433618MHz, 100mVp-p from SG1. SCob (mVp-p) represents the output voltage at measuring point 19. SCor (mVp-p) represents the output voltage at measuring point 22 under the same conditions.

SCdb and SCdr

Under the same measuring conditions specified in 2), measure SCdb and SCdr at measuring points 19 and 22, respectively, as follows.



Or-y · b-y

Under the same conditions specified in 2), measure the phase difference between the output at measuring point 19 and that at 22, which is represented by Or-y · b-y.

FcPP and FcPN

Under the same measuring conditions specified in 2), estimate the frequency of the output from SG1 by starting at 4.435MHz (asynchronous) and moving toward the center frequency (4.433618MHz), with output voltage of 100mVp-p. Determine the lock-in frequency f1. Also, estimate the frequency by starting at 4.432MHz (asynchronous state) and moving toward the center frequency to determine the lock-in frequency f2. We then obtain the following equation.

$$F_{cPP} = f_1 - f_2 \text{ (Hz)}$$

Set SW13 to 1. Estimate the frequency of SG1 by starting at 3.581MHz (asynchronous state) and moving toward the center frequency (3.579545MHz). Determine the lock-in frequency f3. Also, estimate the frequency by starting at 3.578MHz (asynchronous state) and moving toward the center frequency to determine the lock-in frequency f4. We then

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