MITSUBISHI INTEGRATED CIRCUIT

M56760FP

540MHz PLL FREQUENCY SYNTHESIZER

DESCRIPTION

M56760FP is a PLL frequency synthesizer for wirelessphone. Two modulus prescalers of 1/128 and 1/129 are incorporated, and direct input of maximum 540MHz is available.

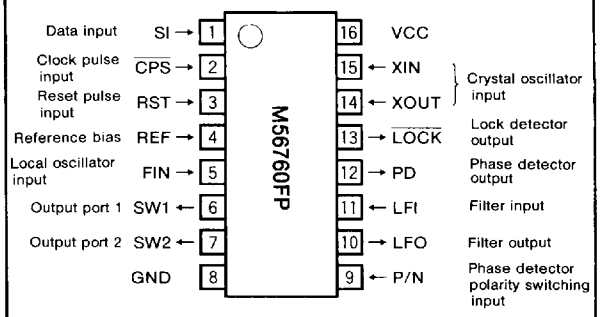
FEATURES

- Two modulus prescalers of 1/128 and 1/129 are incorporated. (fmax=540MHz)
- Large range of operating supply voltage (V_{CC} = 3.0 ~ 5.5V)
- Low current consumption (I_{CC}=14mA at V_{CC}=3V)
- Divider for reference frequency is also programmable. Setting range of dividing ratio N (f_{REF}) = 128 ~ 16,376 (can be set by multiples of 8)
- Programmable divider for local oscillator
  Setting range of dividing ratio N (V. C. O) = 16,384 ~ 131,071 (can be set by multiples of integer)
- Serial data input system
- PLL lock/unlock status indication function
- PLL power on/off can be controlled by transmitted data from controller (Standby current at off is 4mA.)
- Output port whose status can be set by transmitted data from controller
- Transistor for LPF is incorporated.

APPLICATION

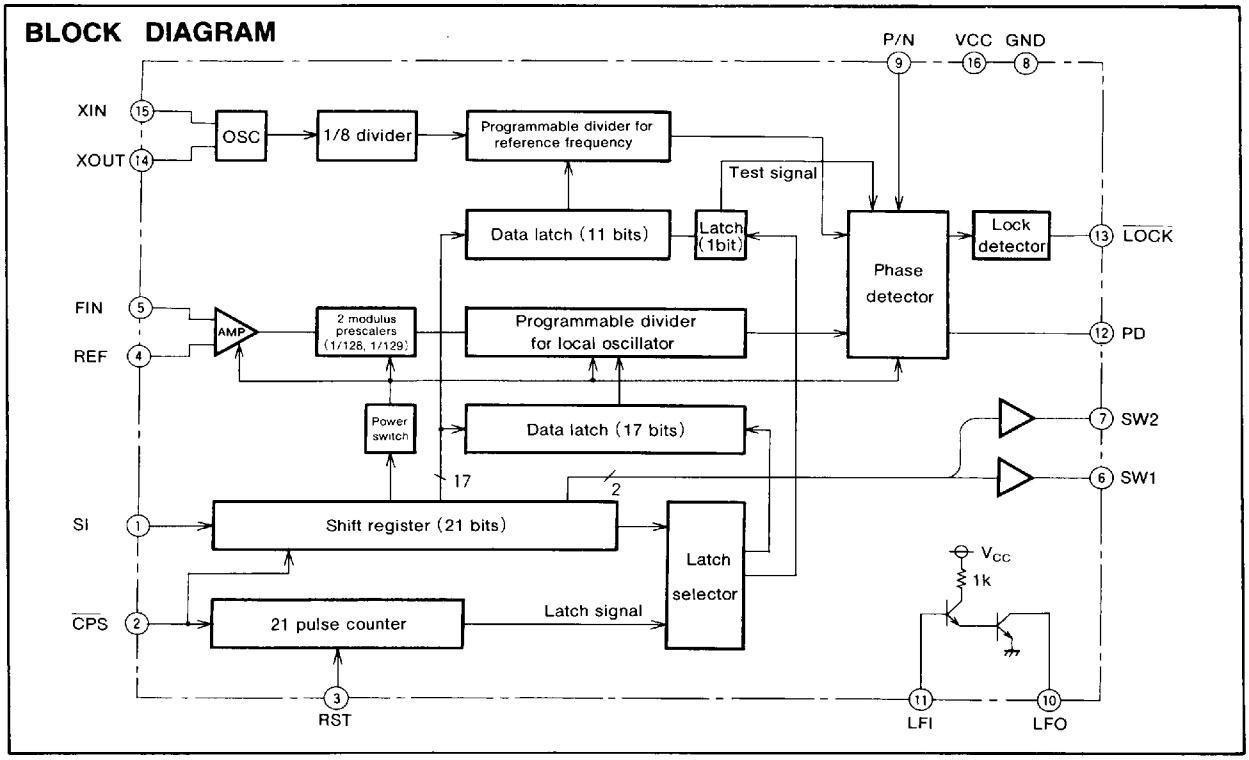
Wirelessphone

PIN CONFIGURATION (TOP VIEW)



Outline 16P2N

BLOCK DIAGRAM

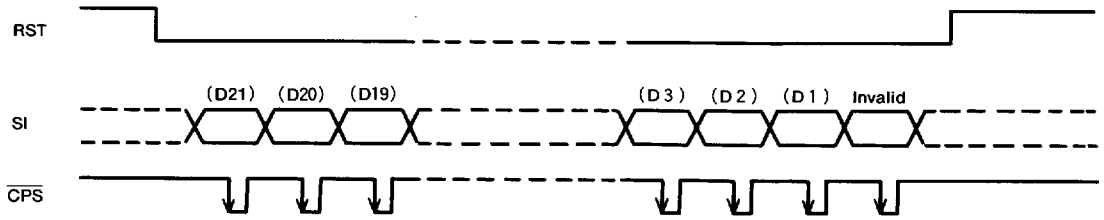


PIN DESCRIPTION

Pin no	Symbol	Pin name	Description
1	SI	Data input	Data input terminal of shift register
2	$\overline{CPS}$	Clock pulse input	Clock pulse input terminal of shift register
3	RST	Reset pulse input	Reset pulse input terminal of 21 pulse counter
4	REF	Reference bias	Grounded with 1000pF condenser.
5	FIN	Local oscillator input	Local oscillator frequency (V. C. O) input.
6	SW1	Output port1	Output port whose status can be set by transmitted data from controller. Open collector
7	SW2	Output port2	
8	GND	Ground	0 V
9	P/N	Phase detector polarity switching input	When this terminal is at "H", PD terminal becomes "H" for phase lead, and "L" for phase lag. When this terminal is at "L", PD terminal becomes "L" for phase lead, and "H" for phase lag.
10	LFO	Filter output	Collector output of transistor for LPF
11	LFI	Filter input	Base input of transistor for LPF
12	PD	Phase detector output	Tristate output
13	$\overline{LOCK}$	Lock detector output	When PLL system is locked ····· "L" When PLL system is unlocked ····· "H" Open collector
14	X_{OUT}	Crystal oscillator input	Output from 12.8MHz reference oscillator is input to XIN. Oscillator by external crystal resonator is available.
15	X_{IN}		
16	V_{CC}	Power terminal	

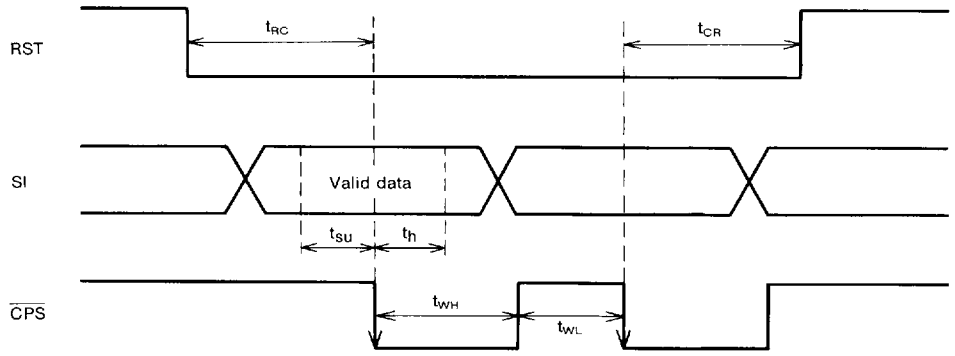
FUNCTION

1. DATA INPUT



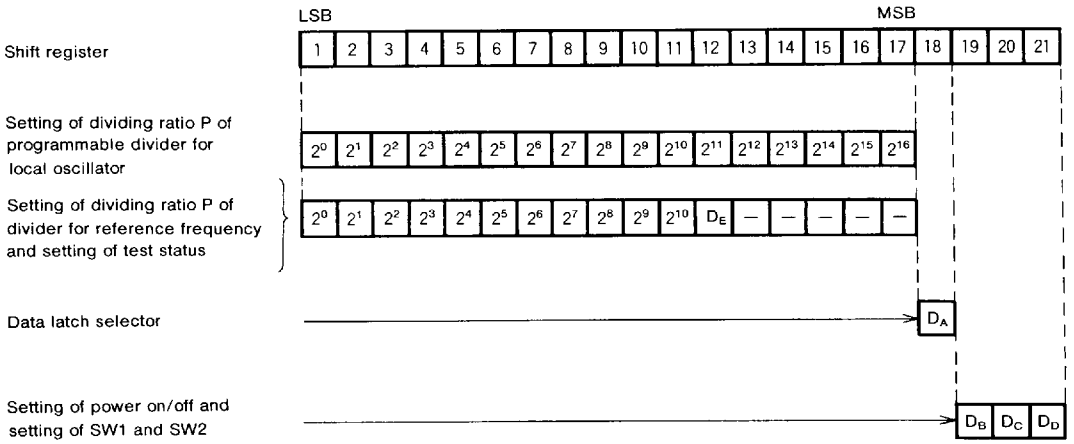
Note 1 : SI input status is read into the shift register in sequence at the trailing edge of CPS input.
2 : All the data(power on/off, latch selection, Nvalue, SW on/off)is set at the CPS trailing edge of the 21st pulse, and later CPS is invalid.
3 : Neither CPS nor SI is accepted while RST is at "H".

2. TIMING OF INPUT SIGNAL



$t_{SU}=t_h=t_{WH}=t_{WL}=10\mu$Smin.
$t_{RC}=t_{CR}=20\mu$Smin.

3. BIT CONFIGURATION OF SHIFT REGISTER



Note 4 : Dividing ratio P of programmable divider is given in 17 bits for divider for local oscillator and in 11 bits for divider for reference frequency.

- Total dividing ratio of local oscillator frequency N(V. C. O)is;
  N(V.C.O)=P, where P=16,384~131,071
- Total dividing ratio of reference frequency N(f_{REF})is;
  N(f_{REF})=8 · P, where P=16~2,047
  12nd bit data De is for test mode. Always set to "L" in normal operation.
  Input "H" or "L" to the 13rd through 17th bits as dummy data.

Data D_E	Status
L	Nomal
H	Test mode

Note 5 : Data latch to be updated is selected by Da.

Data D_A	Explanation
H	Data of latch for reference frequency is updated.
L	Data of latch for local oscillator is updated.

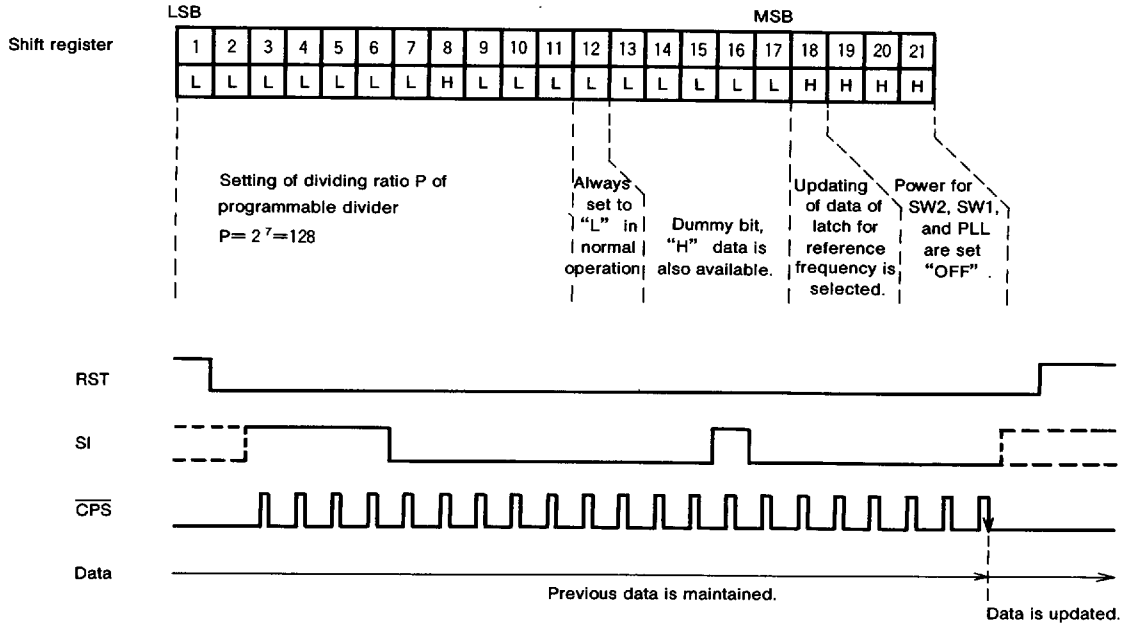
Note 6 : Power on/off of SW1, SW2, and PLL system is set by Db, Dc, and Dd.

Data		Output port	
D_3	D_C	SW2	SW1
L	L	ON	ON
H	L	OFF	ON
L	H	ON	OFF
H	H	OFF	OFF

Data	PLL
D_D	Power switch
L	ON
H	OFF

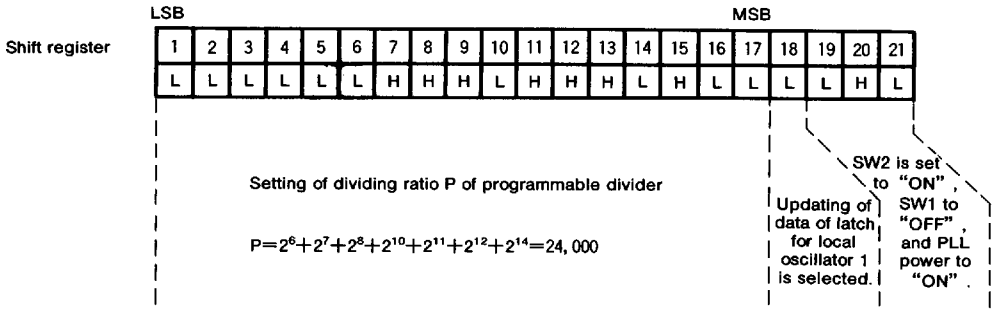
4. DATA CODING EXAMPLE

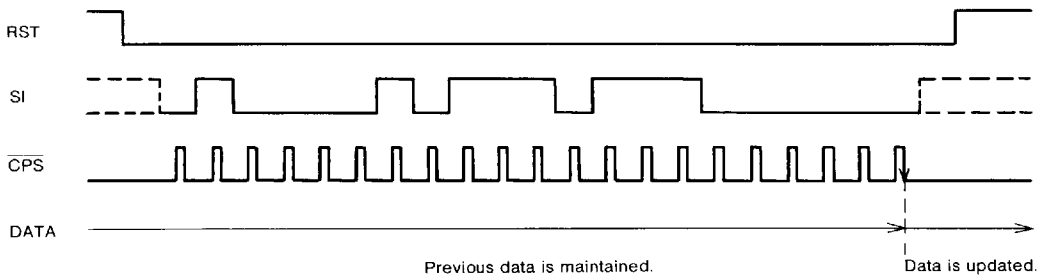
(1) Setting : Reference frequency 12.5kHz, PLL power off, SW1 off, and SW2 off.



Note 7 : Total dividing ratio of reference frequency N(f_{REF}) is set as follows:
N(f_{REF})=8 · P=8x128=1024
when 12.8MHz crystal oscillator is used,
f_{REF}=12,800/1024=12.5kHz

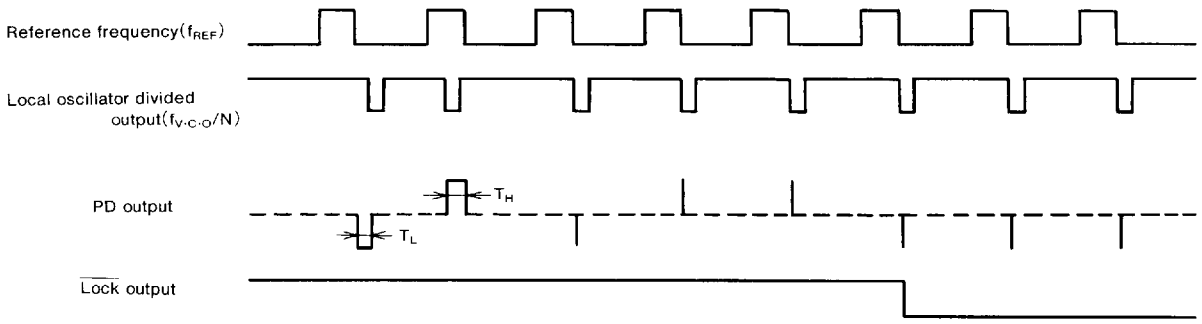
(2) Setting : Dividing ratio for local oscillator 24,000, PLL power on, SW1 off, and SW2 on





Note 8 : If PLL is locked when the reference frequency is set to 12.5kHz;
fv.c.o=12.5x24,000=300,000kHz=300MHz

5. PD, Lock SIGNAL OUTPUT WAVEFORM



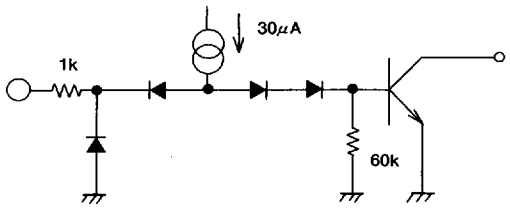
Note 9 : PD output becomes "L" status when the phase of local oscillator divided output ($f_{V\cdot C\cdot O}/N$) is faster than that of reference frequency (f_{REF}) and "H" status when it is behind.
10 : ····· indicates high impedance status.
11 : Lock output becomes "L" status when the phase differences T_L and T_H are kept at below 625nS** for more than three cycles of reference frequency (fr).

* : The above explanation is the case when P/N input (11 pin) is at "H" status.
In the case that P/N input is at "L" status, polarity of PD output is reversed.
** : This is the case when 12.8MHz oscillator is used for reference oscillator frequency.

INPUT/OUTPUT CIRCUIT DRAWING

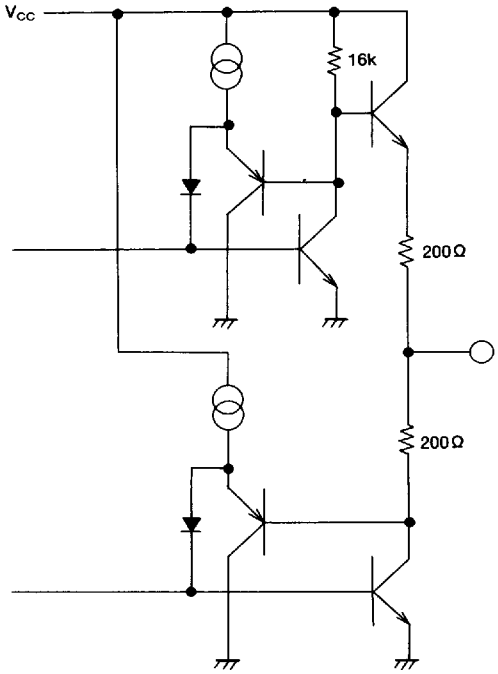
1

Each input of RST, $\overline{CPS}$, SI, and P/N



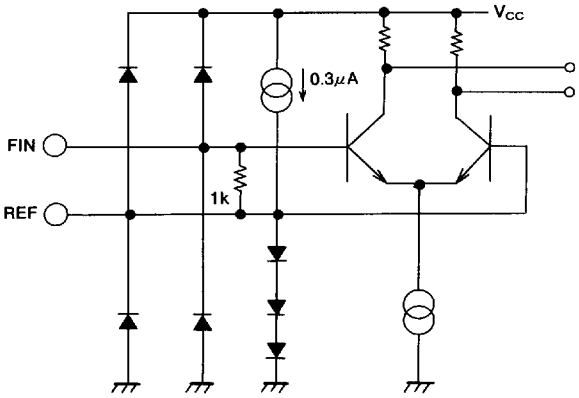
2

PD output



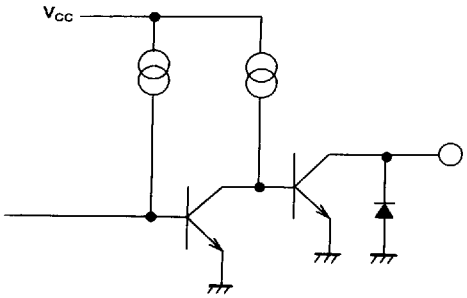
3

Each input of FIN and REF



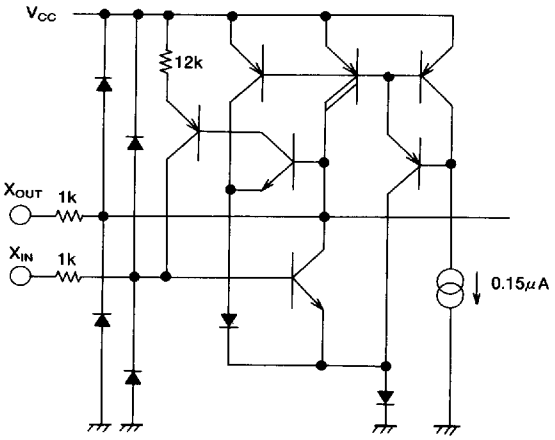
4

$\overline{Lock}$ output Vcc



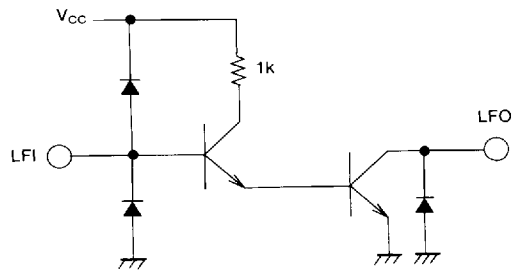
5

OSC circuit



6

Circuit drawing of transistor for LPF



Note12 : Resistance and power source are standard values when V_{CC}=3V and T_a=25℃.

ABSOLUTE MAXIMUM RATINGS (T_a=−20℃～75℃, unless otherwise noted)

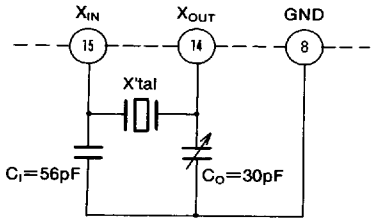
Symbol	Parameter	Conditions	Ratings		Unit	Remarks
			Min.	Max.		
V_{CC}	Supply voltage		−0.5	6.0	V	
V_I	Input voltage	Each input	−0.5	6.0	V	
V_O	Output voltage	Each output	−0.5	6.0	V	
P_d	Power dissipation	T_a=75℃		300	mW	Allowable power dissipation of package
Topr	Operating ambient temperature		−20	75	℃	
Tstg	Storing ambient temperature		−40	125	℃	

RECOMMENDED OPERATING CONDITIONS (T_a =−20～75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit	Remarks
			Min.	Typ.	Max.		
V_{CC}	Supply voltage	F_{IN}=100～540MHz	3.0		5.5	V	
V_{IN}	Input amplitude	F_{IN}=100～540MHz	160		640	mVp-p	
F_{IN}	Input frequency	V_{CC}=3.0～5.5V	100		540	MHz	
I_{OL}	Low-level output current	Each output of $\overline{LOCK}$ and LFO			1	mA	
V_{XIN}	XIN input amplitude	V_{CC}=3.0～5.5V f_{osc}=10～15MHz sine wave	0.5		2	Vp-p	15.2
f_{osc}	Reference oscillator frequency	V_{CC}=3.0～5.5V V_{XIN}=0.5～2Vp-p	10	12.8	15	MHz	15.1～2

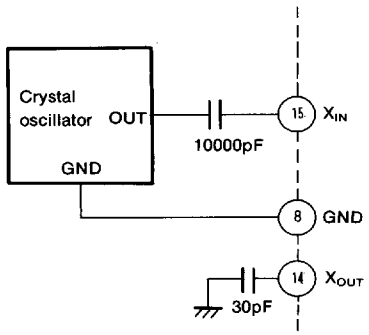
540MHz PLL FREQUENCY SYNTHESIZER

Connection of crystal resonator



X'tal load capacity 20pF effective resistance 100Ω or less

Connection of crystal oscillator

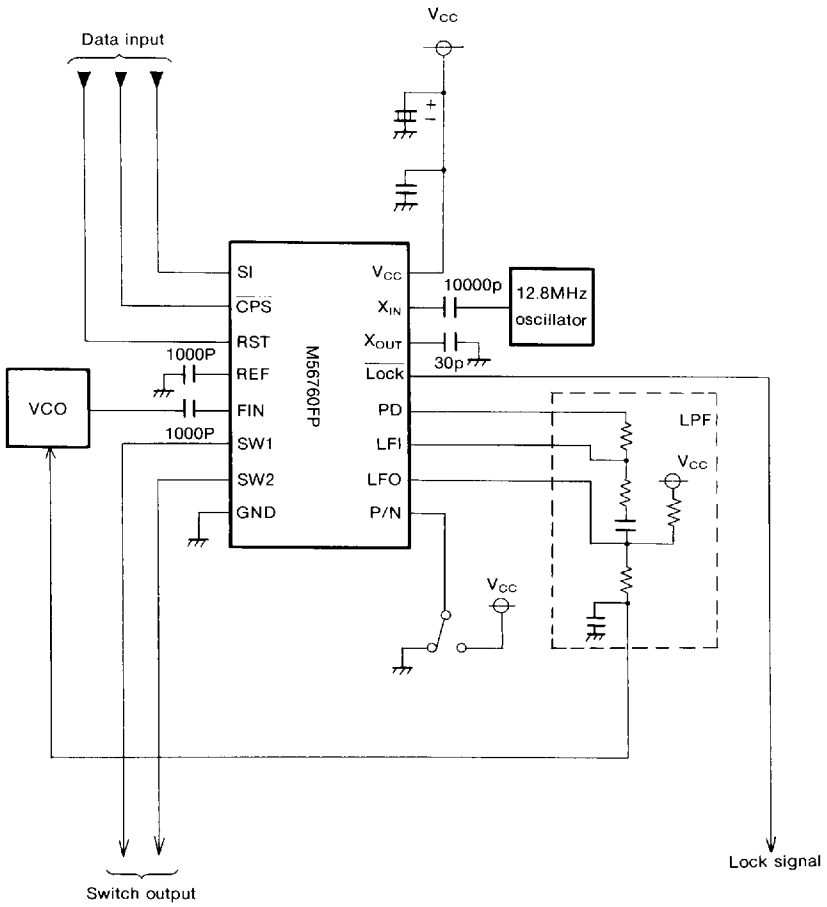


ELECTRICAL CHARACTERISTICS (T_a=−20~75℃, unless otherwise noted)

Symbol	Parameter	Terminal	Test Conditions	Limits			Unit
				Min.	Typ.	Max.	
V_{IH}	High-level input voltage	SI, $\overline{CPS}$, RST, P/N	V_{CC}=3.0~5.5V	2		5.5	V
V_{IL}	Low-level input voltage	SI, $\overline{CPS}$, RST, P/N	V_{CC}=3.0~5.5V	0		0.6	V
I_{IH}	High-level input current	SI, $\overline{CPS}$, RST, P/N	V_{CC}=5.5V V_{IH}=5.5V			10	μA
I_{IL}	Low-level input current	SI, $\overline{CPS}$, RST, P/N	V_{CC}=5.5V V_{IL}=0V		−30	−60	μA
V_{OL}	Low-level output voltage	$\overline{LOCK}$	V_{CC}=3.0V I_{OL}=1mA			0.4	V
V_{OHP1}	PD High-level output voltage	PD	V_{CC}=5V I_{OH}=−1mA	3.5			V
V_{OHP2}	PD High-level output voltage	PD	V_{CC}=3.0V I_{OH}=−0.1mA	2			V
V_{OLP1}	PD Low-level output voltage	PD	V_{CC}=5V I_{OL}=1mA			1.5	V
V_{OLP2}	PD Low-level output voltage	PD	V_{CC}=3.0V I_{OL}=0.1mA			1	V
I_{PD1}	PD leak current	PD	V_{CC}=5.5V V_O=0.8~4.7V			±1	μA
I_{PD2}	PD leak current	PD	V_{CC}=5V V_O=2.5V			±100	μA
I_{CC1}	Supply current	V_{CC}	V_{CC}=5.5V, PLL power "OFF"		4	8	mA
I_{CC2}			V_{CC}=5.5V, PLL power "ON"		14	25	mA
I_{OLK}	Output leak current	$\overline{LOCK}$, LFO	V_{CC}=5.5V V_{OH}=5.5V			5	μA
I_{SIOS}	Input bias current	LFI	V_{CC}=5V I_C=1mA, V_C=2.5V			±1	μA
V_{OL}		SW1 SW2	V_{CC}=3.0V I_{OL}=2mA			0.5	V

Note 13 : GND terminal (8 pin) of this circuit is the reference (0V) for all the voltages.
14 : Current flowing into the circuit is positive (no symbol) and that flowing out is negative (−symbol), and maximum and minimum values are indicated in absolute values.
15 : Typical value is that when V_{CC}=3V and T_a=25℃.

APPLICATION EXAMPLE



16P2N — Plastic 16pin 300mil(200mil body)SOP

Dimension in mm