M66200AP/AFP

DRAM CONTROLLER

DESCRIPTION

The M66200AP/AFP is a semiconductor integrated circuit for 256K- and 1M-bit CMOS-process DRAM controllers. The device can control all necessary DRAM signals, including MPU, RAS and CAS memory control signals of signals and the signals to adjust the memory access and refresh.

The M66200AP/AFP can be used in combination with one of the address selectors of the M66210, M66211, M66212 and M66213.

The device supports almost all the 16-bit MPUs available in the market and supports 256K×1, 1M×1, 64K×1, 64K×4, 256K×4bit DRAMs.

FEATURES

- No-wait read/write access is possible if DRAM is less than 120ns when MPU is 8MHz or 10MHz.
- "Early write" feature
- Refresh
  - Automatic refresh: CAS before RAS method
  - External refresh: RAS only method
- Usable on either $\overline{RAS0}$ bank or $\overline{RAS1}$ bank
- Byte switching capability between $\overline{CAS0}$ and $\overline{CAS1}$
- Memory space:
  - When 1M-bit DRAMs are used: 4M bytes maximum
  - When 256K-bit DRAMs are used: 1M byte maximum
- Drive capability: $I_O = \pm 24$ mA
- TTL input level
- 5V single power supply
- The following types are available as an address selector IC
  - 10-line data latch (24-pin)
    - M66210P/FP (non-inverted output)
    - M66211P/FP (inverted output)
  - 2→1 line (×5) data selector (20 pins)
    - M66212P/FP (non-inverted output)
    - M66213P/FG (inverted output)

APPLICATION

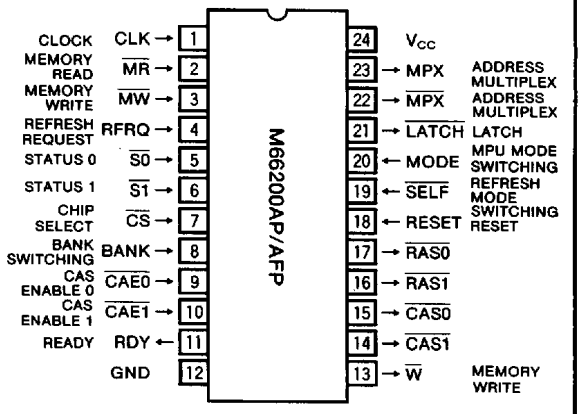
General-purpose 16-bit microprocessor and all systems using DRAM

FUNCTIONAL DESCRIPTION

The M66200A is an integrated circuit for a CMOS-process 256K- and 1M-bit DRAM controller which suppresses its noise caused by high output current switching by circuit configuration. The device supports general-purpose 16-bit microprocessors available in the market.

The chip select $\overline{CS}$, memory read ($\overline{MR}$), memory write ($\overline{MW}$), status ($\overline{SO}$ and $\overline{SI}$) as input as the MPU memory control signal, the system clock is input to CLK, and then $\overline{RAS}$, $\overline{CAS}$, memory write ($\overline{W}$), ready ($\overline{RDY}$), address multiplex (MPX, $\overline{MPX}$ and $\overline{LATCH}$) signals are output according to the memory access operation (memory read, memory write). Refresh operation is synchronized with the clock.

PIN CONFIGURATION (TOP VIEW)



Outline 24P4D
24P2N-B

No-wait memory access is possible when a general-purpose 16-bit microprocessor is an 8MHz or 10MHz version and 256K- or 1M-bit DRAM is a high-speed version of 120ns or less.

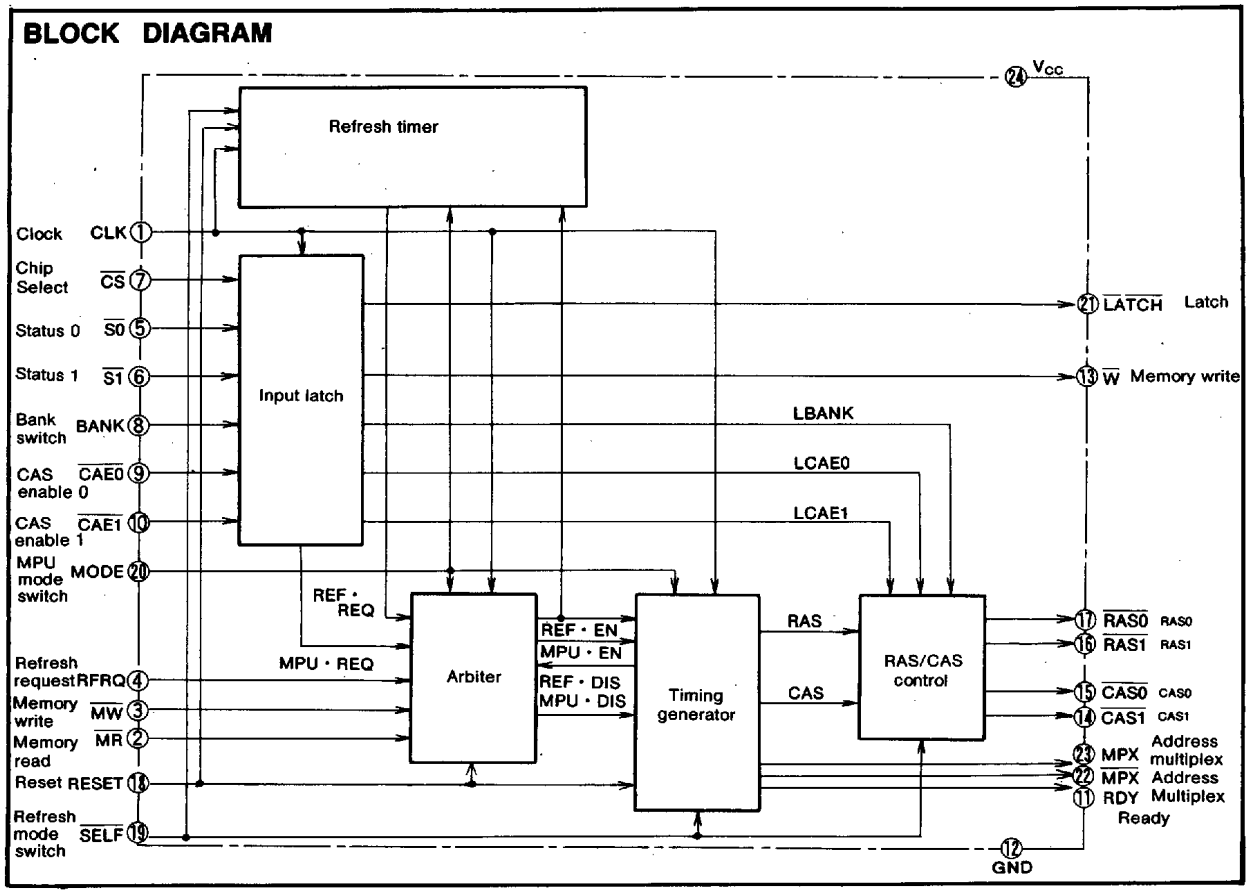
The built-in refresh timer controls refresh rate, (which is 14μs when the system clock is set to 8MHz).

The management of memory access and refresh requests are made by the built-in arbiter. The arbiter gives priority to the request that comes first. If a refresh request comes during a memory access, the refresh operation is started after the memory access is completed. On the other hand, if a memory access comes from the MPU during a refresh operation, the memory access request is not accepted until the refresh cycle is completed (RDY output is not made). And, a wait cycle is entered in the MPU (four-wait maximum).

Automatic refresh by the built-in refresh timer follows the "CAS before RAS" method. External refresh using the refresh request input RFRQ is also possible. In this case, the refresh is made by "RAS only" method.

The M66200A has a pair of RAS and CAS. Bank switching and byte switching is possible. This control mode uses bank switching input (BANK), and CAS enable inputs ($\overline{CAE0}$ and $\overline{CAE1}$).

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION OF INTERNAL BLOCKS

Block name	Function
Refresh timer	When $\overline{SELF}$ is low, the refresh request signal is generated at a fixed interval. • When MODE is low, the refresh request signal is generated at an interval of 116 CLK pulses • When MODE is high, the refresh request signal is generated at an interval of 230 CLK pulses.
Input latch	$\overline{CS}$, $\overline{S0}$, $\overline{S1}$, BANK, $\overline{CAE0}$ and $\overline{CAE1}$ signals from MPU are latched.
Arbiter	Determines and adjusts memory access cycle priority and refresh cycle priority. The arbiter gives priority to whichever comes first; memory access request or refresh request.
Timing generator	RAS, CAS or W signals are generated according to the cycle that the arbiter determines. The write cycle uses "early write method" and the refresh cycle use "CAS before RAS" (when $\overline{SELF}$ is low).
RAS, CAS control	Choice between RAS and CAS is determined by the combination of three inputs of BANK, $\overline{CAE0}$ and $\overline{CAE1}$.

FUNCTIONAL DESCRIPTION OF PINS

<table>
<tr><th>I/O</th><th>Symbol</th><th>Function</th></tr>
<tr><td rowspan="11">Input</td><td>RESET</td><td>Reset input
Reset input is set to "high" by built-in flip-flop reset input.(Refresh operation is not executed as the refresh counter is reset during the reset period.)</td></tr>
<tr><td>CLK</td><td>Clock input</td></tr>
<tr><td>$\overline{CS}$
$\overline{S0}$, $\overline{S1}$</td><td>MPU address decoder signal
Status signal from MPU
(Memory access cycle is started by the $\overline{CS}$, $\overline{S0}$ and $\overline{S1}$ signals.
CLK falling edge-sampling.)
<table>
<tr><th>$\overline{S0}$</th><th>$\overline{S1}$</th><th>A mode</th><th>B mode</th></tr>
<tr><td>L</td><td>L</td><td>Read</td><td>No access</td></tr>
<tr><td>L</td><td>H</td><td>Write</td><td>Write</td></tr>
<tr><td>H</td><td>L</td><td>Read</td><td>Read</td></tr>
<tr><td>H</td><td>H</td><td>No access</td><td>No access</td></tr>
</table></td></tr>
<tr><td>$\overline{MR}$</td><td>Read signal from MPU (Detects end of read cycle.)</td></tr>
<tr><td>$\overline{MW}$</td><td>Write signal from MPU (Detects end of write cycle.)</td></tr>
<tr><td>MODE</td><td>MPU select input
<table>
<tr><th>MODE</th><th>MPU mode</th><th>MPU</th></tr>
<tr><td>L</td><td>A mode</td><td>4-bus cycle MPU</td></tr>
<tr><td>H</td><td>B mode</td><td>2-bus cycle MPU</td></tr>
</table></td></tr>
<tr><td>$\overline{SELF}$</td><td>Refresh mode select input
<table>
<tr><th>$\overline{SELF}$</th><th>Refresh mode</th></tr>
<tr><td>L</td><td>Automatic refresh (CAS before RAS refresh)</td></tr>
<tr><td>H</td><td>External refresh (RAS only refresh)</td></tr>
</table></td></tr>
<tr><td>RFRQ</td><td>Refresh signal
Used when $\overline{SELF}$ is high (external refresh),
RFRQ becomes $\overline{RAS}$. Inputting the timing of $\overline{RAS}$ only refresh to this pin sets refresh to "$\overline{RAS}$ only refresh".
When $\overline{SELF}$ is low, this is set low (automatic refresh).</td></tr>
<tr><td>BANK
$\overline{CAE0}$
$\overline{CAE1}$</td><td>RAS and CAS which become valid by the combination of three inputs are determined.
<table>
<tr><th>BANK</th><th>$\overline{CAE0}$</th><th>$\overline{CAE1}$</th><th>$\overline{RAS0}$</th><th>$\overline{RAS1}$</th><th>$\overline{CAS0}$</th><th>$\overline{CAS1}$</th></tr>
<tr><td>L</td><td>L</td><td>L</td><td>Valid</td><td>H</td><td>Valid</td><td>Valid</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>Valid</td><td>H</td><td>Valid</td><td>H</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>Valid</td><td>H</td><td>H</td><td>Valid</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>Valid</td><td>H</td><td>H</td><td>H</td></tr>
<tr><td>H</td><td>L</td><td>L</td><td>H</td><td>Valid</td><td>Valid</td><td>Valid</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>H</td><td>Valid</td><td>Valid</td><td>H</td></tr>
<tr><td>H</td><td>H</td><td>L</td><td>H</td><td>Valid</td><td>H</td><td>Valid</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>H</td><td>Valid</td><td>H</td><td>H</td></tr>
</table></td></tr>
<tr><td rowspan="6">Output</td><td>$\overline{RAS0}$
$\overline{RAS1}$</td><td>Row address strobe signal</td></tr>
<tr><td>$\overline{CAS0}$
$\overline{CAS1}$</td><td>Column address strobe signal</td></tr>
<tr><td>$\overline{W}$</td><td>Write signal to DRAM</td></tr>
<tr><td>MPX
$\overline{MPX}$</td><td>Multiplex signal to external data selector</td></tr>
<tr><td>$\overline{LATCH}$</td><td>Latch signal to external data selector</td></tr>
<tr><td>RDY</td><td>Ready signal to MPU</td></tr>
</table>

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Conditions	Ratings	Unit
V_{CC}	Supply voltage			−0.5～+7.0	V
V_I	Input voltage			−0.5～V_{CC}+0.5	V
V_O	Output voltage			−0.5～V_{CC}+0.5	V
I_{IK}	Input protection diode current		$V_I < 0V$	−20	mA
			$V_I > V_{CC}$	+20	
I_{OK}	Input parasitic diode current		$V_O < 0V$	−20	mA
			$V_O > V_{CC}$	+20	
I_O	Output current	$\overline{RAS0}$, $\overline{RAS1}$, $\overline{CAS0}$, $\overline{CAS1}$, $\overline{W}$		±50	mA
		MPX, $\overline{MPX}$, RDY, $\overline{LATCH}$		±20	
I_{CC}	Supply/GND current		V_{CC}, GND	±200	mA
P_d	Power dissipation			500	mW
Tstg	Storage temperature			−65～+150	℃
T_{opr}	Operating temperature			0～70	℃

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5		5.5	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V

ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits 25℃ Min	Limits 25℃ Max	Limits 0～70℃ Min	Limits 0～70℃ Max	Unit
V_{T+}	Positive threshold voltage	RESET	V_O=0.1, V_{CC}−0.1V, I_O=20μA			2.4		2.4	V
V_{T-}	Negative threshold voltage	RESET	V_O=0.1, V_{CC}−0.1V, I_O=20μA		0.6		0.6		V
V_H	Hysteresis voltage	RESET	V_O=0.1, V_{CC}−0.1V, I_O=20μA		0.2	1.8	0.2	1.8	V
V_{IH}	High-level input voltage	($\overline{SELF}$, MODE)	V_O=0.1, V_{CC}−0.1V, I_O=20μA		2.4		2.4		V
V_{IL}	Low-level input voltage	($\overline{SELF}$, MODE)	V_O=0.1, V_{CC}−0.1V, I_O=20μA			0.6		0.6	V
V_{IH}	High-level input voltage	(Other input)	V_O=0.1, V_{CC}−0.1V, I_O=20μA		2.0		2.0		V
V_{IL}	Low-level input voltage	(Other input)	V_O=0.1, V_{CC}−0.1V, I_O=20μA			0.8		0.8	V
V_{OH}	High-level output voltage	$\overline{RAS0}$, $\overline{RAS1}$, $\overline{CAS0}$, $\overline{CAS1}$, $\overline{W}$	$V_I = V_{IH}$, V_{IL}	I_{OH} = −20μA	V_{CC}−0.1		V_{CC}−0.1		V
				I_{OL} = −24mA, V_{CC}=4.5V	3.83		3.70		
V_{OL}	Low-level output voltage	$\overline{RAS0}$, $\overline{RAS1}$, $\overline{CAS0}$, $\overline{CAS1}$, $\overline{W}$	$V_I = V_{IH}$, V_{IL}	I_{OH} = 20μA		0.1		0.1	V
				I_{OL} = 24mA, V_{CC}=4.5V		0.44		0.53	
V_{OH}	High-level output voltage	MPX, $\overline{MPX}$, RDY, $\overline{LATCH}$	$V_I = V_{IH}$, V_{IL}	I_{OH} = −20μA	V_{CC}−0.1		V_{CC}−0.1		V
				I_{OL} = −8mA, V_{CC}=4.5V	3.83		3.70		
V_{OL}	Low-level output voltage	MPX, $\overline{MPX}$, RDY, $\overline{LATCH}$	$V_I = V_{IH}$, V_{IL}	I_{OL} = 20μA		0.1		0.1	V
				I_{OL} = 8mA, V_{CC}=4.5V		0.44		0.53	
I_{IH}	High-level input current		$V_I = V_{CC}$			0.1		1.0	μA
I_{IL}	Low-level input current		V_I = GND			−0.1		−1.0	μA
I_{CC}	Static power dissipation current		$V_I = V_{CC}$, GND, I_O = 0μA			10.0		100	μA
ΔI_{CC}	Maximum static power dissipation		V_I = 2.4V, 0.4V (Note)			2.7		2.9	mA
C_I	Input capacitance					10		10	pF

Note : This value is set to one input and all other inputs are fixed to V_{CC} or GND.

SWITCHING CHARACTERISTICS (V_{CC}=5V±10%, T_a=0~70°C)

This standard assumes the use of the address data selectors M66210P/FP~M66213P/FP

MEMORY ACCESS (A MODE)

Number	Symbol	Parameter	Test conditions	Limits		Unit
				Min	Max	
—	f_{max}	Maximum repetitive frequency		20		MHz
1	t_{TLH}	Output transition time	C_L=50pF (RDY, $\overline{LATCH}$, MPX, $\overline{MPX}$)		15	ns
	t_{THL}				15	
2	t_{TLH}		C_L=50pF ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$)		10	ns
	t_{THL}				10	
	t_{TLH}		C_L=200pF ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$)		20	ns
	t_{THL}				20	
3	t_{PLH}	CLK—$\overline{RAS}$ propagation time	C_L=50pF		34	ns
	t_{PHL}				36	
4	t_{PLH}		C_L=150pF	10	36	ns
	t_{PHL}			13	40	
5	t_{PLH}	$\overline{MR}$, $\overline{MW}$—$\overline{CAS}$ propagation time	C_L=50pF		41	ns
	t_{PHL}				36	
6	t_{PLH}	CLK—$\overline{CAS}$	C_L=150pF	14	43	ns
	t_{PHL}			13	40	
7	t_{PLH}	CLK—MPX, $\overline{MPX}$ propagation time	C_L=50pF	21	62	ns
	t_{PHL}			21	62	
8	t_{PLH}	CLK—MPX, $\overline{MPX}$ propagation time	C_L=50pF	18	74	ns
	t_{PHL}			18	74	
9	t_{PLH}	$\overline{MW}$—$\overline{W}$ propagation time	C_L=50pF		48	ns
	t_{PHL}				25	
10	t_{PLH}	$\overline{S0}$—$\overline{W}$ propagation time (when $\overline{S0}$ and $\overline{S1}$ are used)	C_L=200pF		52	ns
	t_{PHL}				34	
11	t_{PLH}	$\overline{MW}$—$\overline{W}$ propagation time (when $\overline{S0}$ and $\overline{S1}$ are not used)	C_L=50pF		20	ns
	t_{PHL}				20	
12	t_{PLH}		C_L=200pF		24	ns
	t_{PHL}				28	
13	t_{PLH}	CLK—RDY propagation time	C_L=50pF		36	ns
14	t_{PHL}	$\overline{MR}$, $\overline{MW}$—RDY			36	
15	t_{PLH}	$\overline{MR}$, $\overline{MW}$—$\overline{LATCH}$ propagation time	C_L=50pF		32	ns
16	t_{PHL}	CLK—$\overline{LATCH}$			32	

MEMORY ACCESS (B MODE)

Number	Symbol	Parameter	Test conditions	Limits Min	Limits Max	Unit
—	f_{max}	Maximum repetitive frequency		20		MHz
17	t_{TLH}	Output transition time	C_L=50pF (RDY, $\overline{LATCH}$, MPX, $\overline{MPX}$)		15	ns
	t_{THL}				15	
18	t_{TLH}		C_L=50pF ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$)		10	ns
	t_{THL}				10	
	t_{TLH}		C_L=200pF ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$)		20	ns
	t_{THL}				20	
19	t_{PLH}	CLK—$\overline{RAS}$ propagation time	C_L=50pF		34	ns
	t_{PHL}				36	
20	t_{PLH}		C_L=150pF	10	36	ns
	t_{PHL}			13	40	
21	t_{PLH}	$\overline{MR}$, $\overline{MW}$—$\overline{CAS}$ propagation time	C_L=50pF		41	ns
	t_{PHL}				36	
22	t_{PLH}	CLK—$\overline{CAS}$	C_L=150pF	14	43	ns
	t_{PHL}			13	40	
23	t_{PLH}	CLK—MPX, $\overline{MPX}$ propagation time	C_L=50pF	21	62	ns
	t_{PHL}			21	62	
24	t_{PLH}	CLK—MPX, $\overline{MPX}$ propagation time	C_L=50pF	18	74	ns
	t_{PHL}			18	74	
25	t_{PLH}	$\overline{MW}$—$\overline{W}$ propagation time	C_L=50pF		48	ns
	t_{PHL}				25	
26	t_{PLH}	$\overline{S0}$—$\overline{W}$	C_L=200pF		52	ns
	t_{PHL}				34	
27	t_{PLH}	CLK—RDY propagation time	C_L=50pF		36	ns
28	t_{PHL}	$\overline{MR}$, $\overline{MW}$—RDY			36	
29	t_{PLH}	$\overline{MR}$, $\overline{MW}$—$\overline{LATCH}$ propagation time	C_L=50pF		32	ns
30	t_{PHL}	CLK—$\overline{LATCH}$			32	

INTERNAL REFRESH (CAS BEFORE RAS) (A MODE)

Number	Symbol	Parameter	Test conditions	Limits Min	Limits Max	Unit
31	t_{PLH}	CLK—$\overline{RAS}$ propagation time	C_L=50pF		38	ns
	t_{PHL}				38	
32	t_{PLH}		C_L=150pF		41	ns
	t_{PHL}				41	
33	t_{PLH}	CLK—$\overline{CAS}$ propagation time	C_L=50pF		31	ns
	t_{PHL}				41	
34	t_{PLH}		C_L=150pF		33	ns
	t_{PHL}				45	

INTERNAL REFRESH (CAS BEFORE RAS) (B MODE)

Number	Symbol	Parameter	Test conditions	Limits Min	Limits Max	Unit
35	t_{PLH}	CLK—$\overline{RAS}$ propagation time	C_L=50pF		38	ns
	t_{PHL}				38	
36	t_{PLH}		C_L=150pF		41	ns
	t_{PHL}				41	
37	t_{PLH}	CLK—$\overline{CAS}$ propagation time	C_L=50pF		31	ns
	t_{PHL}				33	
38	t_{PLH}		C_L=150pF		33	ns
	t_{PHL}				37	

EXTERNAL REFRESH (RAS ONLY)

Number	Symbol	Parameter	Test conditions	Limits		Unit
				Min	Max	
39	t_{PLH}	RFRQ—$\overline{RAS}$ propagation time	C_L=50pF		23	ns
	t_{PHL}				23	
40	t_{PLH}		C_L=150pF		27	ns
	t_{PHL}				27	

TIMING REQUIREMENTS (V_{CC}=5V±10%, T_a=0~70℃)
MEMORY ACCESS (A MODE)

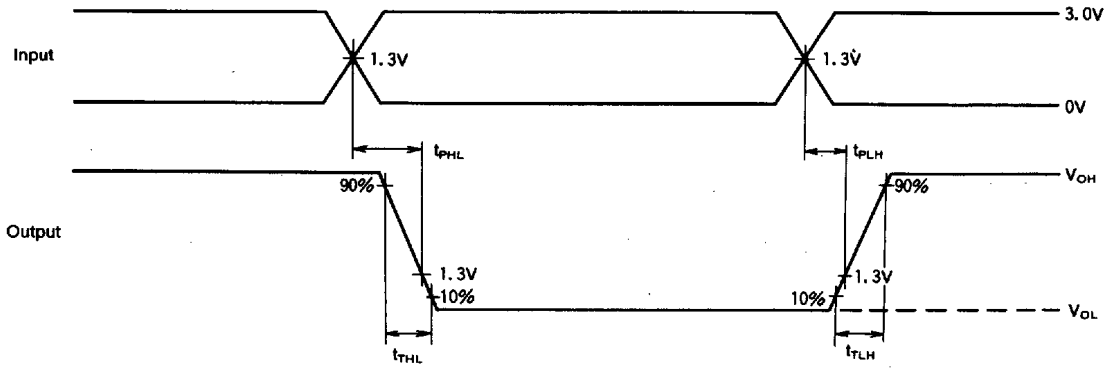
Number	Symbol	Parameter	Test conditions	Limits		Unit
				Min	Max	
41	t_{WH}	Clock pulse width (high level)		20		ns
42	t_{WL}	Clock pulse width (low level)		20		ns
43	t_{su}	CLK—$\overline{CS}$ setup time		20		ns
44	t_h	CLK—$\overline{CS}$ hold time		20		ns
45	t_{su}	CLK—$\overline{S0}$ setup time		20		ns
46	t_h	CLK—$\overline{S0}$ hold time		20		ns
47	t_{su}	CLK—$\overline{S1}$ setup time		20		ns
48	t_h	CLK—$\overline{S1}$ hold time		20		ns
49	t_{su}	CLK—$\overline{MR}$ setup time		20		ns
50	t_h	CLK—$\overline{MR}$ hold time		1.5CK+10	2.5CK−20	ns
51	t_{su}	CLK—$\overline{MW}$ setup time		20		ns
52	t_h	CLK—$\overline{MW}$ hold time		1.0CK+10	2.0CK−20	ns
53	t_{su}	CLK—BANK setup time		20		ns
54	t_h	CLK—BANK hold time		20		ns
55	t_{su}	CLK—$\overline{CAE0}$, $\overline{CAE1}$ setup time		20		ns
56	t_h	$\overline{MR}$, $\overline{MW}$—$\overline{CAE0}$, $\overline{CAE1}$ hold time		20		ns
57	t_{WH}	Reset pulse width (high level)		20		ns
58	t_{rec}	CLK—RESET recovery time		20		ns

MEMORY ACCESS (B MODE)

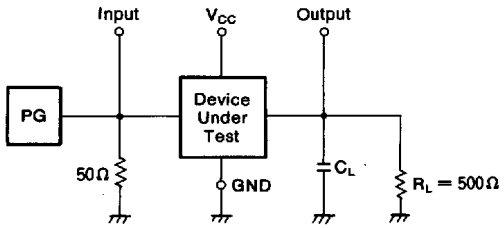
Number	Symbol	Parameter	Test conditions	Limits		Unit
				Min	Max	
59	t_{WH}	Clock pulse width (high level)		20		ns
60	t_{WL}	Clock pulse width (low level)		20		ns
61	t_{su}	CLK—$\overline{CS}$ setup time		20		ns
62	t_h	CLK—$\overline{CS}$ hold time		20		ns
63	t_{su}	CLK—$\overline{S0}$ setup time		20		ns
64	t_h	CLK—$\overline{S0}$ hold time		20		ns
65	t_{su}	CLK—$\overline{S1}$ setup time		20		ns
66	t_h	CLK—$\overline{S1}$ hold time		20		ns
67	t_{su}	CLK—$\overline{MR}$ setup time		20		ns
68	t_h	CLK—$\overline{MR}$ hold time		2.0CK	2.5CK	ns
69	t_{su}	CLK—$\overline{MW}$ setup time		20		ns
70	t_h	CLK—$\overline{MW}$ hold time		1.5CK	2.0CK	ns
71	t_{su}	CLK—BANK setup time		20		ns
72	t_h	CLK—BANK hold time		20		ns
73	t_{su}	CLK—$\overline{CAE0}$, $\overline{CAE1}$ setup time		20		ns
74	t_h	CLK—$\overline{CAE0}$, $\overline{CAE1}$ hold time		20		ns
75	t_{WH}	Reset pulse width (high level)		20		ns
76	t_{rec}	CLK—RESET recovery time		20		ns

Note : The limits of 50, 52, 68 and 70 (max) assume the continuous access from MPU and do not show the limits of operation.

SWITCHING WAVEFORM



TEST CIRCUIT



(1) The pulse generator (PG) has the following characteristics (10%~90%): t_r=3ns, t_f=3ns.
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.