

MITSUBISHI <DIGITAL ASSP>
M66200AP/AFP

DRAM CONTROLLER

DESCRIPTION

The M66200AP/AFP is a semiconductor integrated circuit for 256K- and 1M-bit CMOS-process DRAM controllers. The device can control all necessary DRAM signals, including MPU, RAS and CAS memory control signals of signals and the signals to adjust the memory access and refresh.

The M66200AP/AFP can be used in combination with one of the address selectors of the M66210, M66211, M66212 and M66213.

The device supports almost all the 16-bit MPUs available in the market and supports 256K×1, 1M×1, 64K×1, 64K×4, 256K×4bit DRAMs.

FEATURES

- No-wait read/write access is possible if DRAM is less than 120ns when MPU is 8MHz or 10MHz.
- "Early write" feature
- Refresh
 - Automatic refresh: CAS before RAS method
 - External refresh: RAS only method
- Usable on either RAS0 bank or RAS1 bank
- Byte switching capability between CAS0 and CAS1
- Memory space:
 - When 1M-bit DRAMs are used: 4M bytes maximum
 - When 256K-bit DRAMs are used: 1M byte maximum
- Drive capability: $I_o = \pm 24$ mA
- TTL input level
- 5V single power supply
- The following types are available as an address selector IC
 - 10-line data latch (24-pin)
 - { M66210P/FP (non-inverted output)
 - { M66211P/FP (inverted output)
 - 2→1 line (×5) data selector (20 pins)
 - { M66212P/FP (non-inverted output)
 - { M66213P/FG (inverted output)

APPLICATION

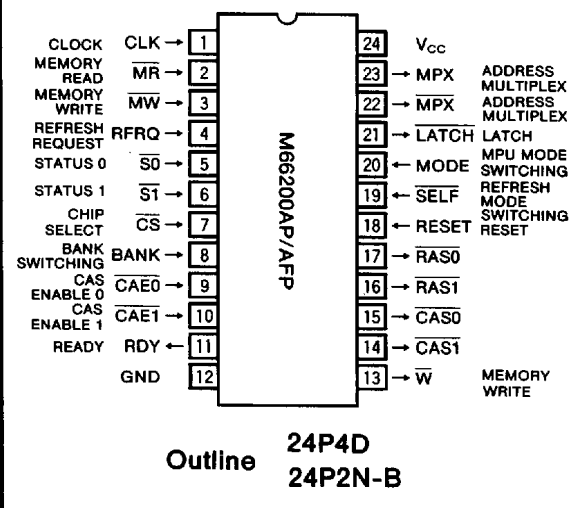
General-purpose 16-bit microprocessor and all systems using DRAM

FUNCTIONAL DESCRIPTION

The M66200A is an integrated circuit for a CMOS-process 256K- and 1M-bit DRAM controller which suppresses its noise caused by high output current switching by circuit configuration. The device supports general-purpose 16-bit microprocessors available in the market.

The chip select \overline{CS} , memory read (\overline{MR}), memory write (\overline{MW}), status (\overline{SO} and \overline{SI}) as input as the MPU memory control signal, the system clock is input to CLK, and then RAS, CAS, memory write (\overline{W}), ready (\overline{RDY}), address multiplex (MPX, MPX and LATCH) signals are output according to the memory access operation (memory read, memory write). Refresh operation is synchronized with the clock.

PIN CONFIGURATION (TOP VIEW)



No-wait memory access is possible when a general-purpose 16-bit microprocessor is an 8MHz or 10MHz version and 256K- or 1M-bit DRAM is a high-speed version of 120ns or less.

The built-in refresh timer controls refresh rate, (which is 14μs when the system clock is set to 8MHz).

The management of memory access and refresh requests are made by the built-in arbiter. The arbiter gives priority to the request that comes first. If a refresh request comes during a memory access, the refresh operation is started after the memory access is completed. On the other hand, if a memory access comes from the MPU during a refresh operation, the memory access request is not accepted until the refresh cycle is completed (RDY output is not made). And, a wait cycle is entered in the MPU (four-wait maximum).

Automatic refresh by the built-in refresh timer follows the "CAS before RAS" method. External refresh using the refresh request input RFRQ is also possible. In this case, the refresh is made by "RAS only" method.

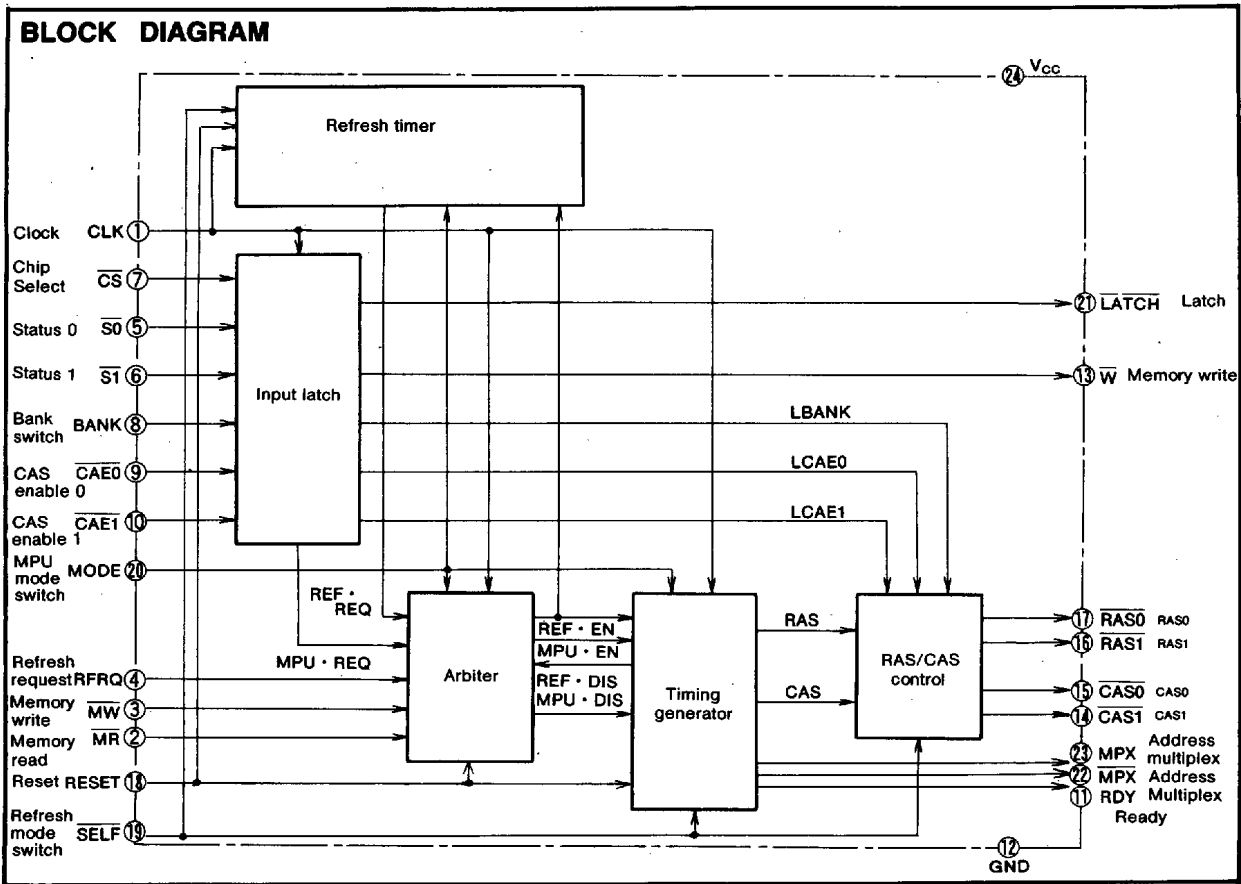
The M66200A has a pair of RAS and CAS. Bank switching and byte switching is possible. This control mode uses bank switching input (BANK), and CAS enable inputs (CAE0 and CAE1).

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FUNCTIONAL DESCRIPTION OF INTERNAL BLOCKS

Block name	Function
Refresh timer	When $\overline{\text{SELF}}$ is low, the refresh request signal is generated at a fixed interval. • When $\overline{\text{MODE}}$ is low, the refresh request signal is generated at an interval of 116 CLK pulses • When $\overline{\text{MODE}}$ is high, the refresh request signal is generated at an interval of 230 CLK pulses.
Input latch	$\overline{\text{CS}}$, $\overline{\text{S0}}$, $\overline{\text{S1}}$, $\overline{\text{BANK}}$, $\overline{\text{CAE0}}$ and $\overline{\text{CAE1}}$ signals from MPU are latched.
Arbiter	Determines and adjusts memory access cycle priority and refresh cycle priority. The arbiter gives priority to whichever comes first; memory access request or refresh request.
Timing generator	RAS, CAS or W signals are generated according to the cycle that the arbiter determines. The write cycle uses "early write method" and the refresh cycle use "CAS before RAS" (when $\overline{\text{SELF}}$ is low).
RAS, CAS control	Choice between RAS and CAS is determined by the combination of three inputs of $\overline{\text{BANK}}$, $\overline{\text{CAE0}}$ and $\overline{\text{CAE1}}$.

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FUNCTIONAL DESCRIPTION OF PINS

I/O	Symbol	Function																																																														
Input	RESET	Reset input Reset input is set to "high" by built-in flip-flop reset input. (Refresh operation is not executed as the refresh counter is reset during the reset period.)																																																														
	CLK	Clock input																																																														
	\overline{CS} S0, S1	MPU address decoder signal Status signal from MPU (Memory access cycle is started by the \overline{CS} , S0 and S1 signals.) (CLK falling edge-sampling.)																																																														
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RFRQ	Refresh signal Used when SELF is high (external refresh), RFRQ becomes RAS. Inputting the timing of RAS only refresh to this pin sets refresh to "RAS only refresh". When SELF is low, this is set low (automatic refresh).																																																															
BANK CAE0 CAE1	RAS and CAS which become valid by the combination of three inputs are determined. <table border="1"> <thead> <tr> <th>BANK</th> <th>CAE0</th> <th>CAE1</th> <th>RAS0</th> <th>RAS1</th> <th>CAS0</th> <th>CAS1</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> <td>L</td> <td>Valid</td> <td>H</td> <td>Valid</td> <td>Valid</td> </tr> <tr> <td>L</td> <td>L</td> <td>H</td> <td>Valid</td> <td>H</td> <td>Valid</td> <td>H</td> </tr> <tr> <td>L</td> <td>H</td> <td>L</td> <td>Valid</td> <td>H</td> <td>H</td> <td>Valid</td> </tr> <tr> <td>L</td> <td>H</td> <td>H</td> <td>Valid</td> <td>H</td> <td>H</td> <td>H</td> </tr> <tr> <td>H</td> <td>L</td> <td>L</td> <td>H</td> <td>Valid</td> <td>Valid</td> <td>Valid</td> </tr> <tr> <td>H</td> <td>L</td> <td>H</td> <td>H</td> <td>Valid</td> <td>Valid</td> <td>H</td> </tr> <tr> <td>H</td> <td>H</td> <td>L</td> <td>H</td> <td>Valid</td> <td>H</td> <td>Valid</td> </tr> <tr> <td>H</td> <td>H</td> <td>H</td> <td>H</td> <td>Valid</td> <td>H</td> <td>H</td> </tr> </tbody> </table>	BANK	CAE0	CAE1	RAS0	RAS1	CAS0	CAS1	L	L	L	Valid	H	Valid	Valid	L	L	H	Valid	H	Valid	H	L	H	L	Valid	H	H	Valid	L	H	H	Valid	H	H	H	H	L	L	H	Valid	Valid	Valid	H	L	H	H	Valid	Valid	H	H	H	L	H	Valid	H	Valid	H	H	H	H	Valid	H	H
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Output	RAS0 RAS1	Row address strobe signal																																																														
	CAS0 CAS1	Column address strobe signal																																																														
	W	Write signal to DRAM																																																														
	MPX MPX	Multiplex signal to external data selector																																																														
	LATCH	Latch signal to external data selector																																																														
	RDY	Ready signal to MPU																																																														

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		-0.5~+7.0	V
V_I	Input voltage		-0.5~ $V_{CC}+0.5$	V
V_O	Output voltage		-0.5~ $V_{CC}+0.5$	V
I_{IK}	Input protection diode current	$V_I < 0V$	-20	mA
		$V_I > V_{CC}$	+20	
I_{OK}	Input parasitic diode current	$V_O < 0V$	-20	mA
		$V_O > V_{CC}$	+20	
I_O	Output current	RAS0, RAS1, CAS0, CAS1, W	±50	mA
		MPX, MPX, RDY, LATCH	±20	
I_{CC}	Supply/GND current	V_{CC} , GND	±200	mA
P_d	Power dissipation		500	mW
T_{stg}	Storage temperature		-65~+150	°C
T_{opr}	Operating temperature		0~70	°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5		5.5	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V

ELECTRICAL CHARACTERISTICS ($V_{CC}=5V\pm 10\%$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits				Unit
			25°C		0~70°C		
			Min	Max	Min	Max	
V_{T+}	Positive threshold voltage	RESET $V_O=0.1, V_{CC}=0.1V, I_O=20\mu A$		2.4		2.4	V
V_{T-}	Negative threshold voltage		0.6		0.6		V
V_H	Hysteresis voltage		0.2	1.8	0.2	1.8	V
V_{IH}	High-level input voltage	(SELF, MODE) $V_O=0.1, V_{CC}=0.1V, I_O=20\mu A$	2.4		2.4		V
V_{IL}	Low-level input voltage			0.6		0.6	V
V_{IH}	High-level input voltage	(Other input) $V_O=0.1, V_{CC}=0.1V, I_O=20\mu A$	2.0		2.0		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_{OH}	High-level output voltage	RAS0, RAS1 CAS0, CAS1, W $V_I = V_{IH}, V_{IL}$	$I_{OH} = -20\mu A$ $I_{OL} = -24mA, V_{CC}=4.5V$	$V_{CC}-0.1$ 3.83	$V_{CC}-0.1$ 3.70		V
V_{OL}	Low-level output voltage		$I_{OH} = 20\mu A$ $I_{OL} = 24mA, V_{CC}=4.5V$		0.1 0.44	0.1 0.53	V
V_{OH}	High-level output voltage	MPX, MPX RDY, LATCH $V_I = V_{IH}, V_{IL}$	$I_{OH} = -20\mu A$ $I_{OL} = -8mA, V_{CC}=4.5V$	$V_{CC}-0.1$ 3.83	$V_{CC}-0.1$ 3.70		V
V_{OL}	Low-level output voltage		$I_{OH} = 20\mu A$ $I_{OL} = 8mA, V_{CC}=4.5V$		0.1 0.44	0.1 0.53	V
I_{IH}	High-level input current	$V_I = V_{CC}$		0.1		1.0	μA
I_{IL}	Low-level input current	$V_I = GND$		-0.1		-1.0	μA
I_{CC}	Static power dissipation current	$V_I = V_{CC}, GND, I_O = 0\mu A$		10.0		100	μA
ΔI_{CC}	Maximum static power dissipation	$V_I = 2.4V, 0.4V$ (Note)		2.7		2.9	mA
C_I	Input capacitance			10		10	pF

Note : This value is set to one input and all other inputs are fixed to V_{CC} or GND.

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SWITCHING CHARACTERISTICS ($V_{CC}=5V\pm 10\%$, $T_a=0\sim 70^\circ C$)

This standard assumes the use of the address data selectors M66210P/FP~M66213P/FP

MEMORY ACCESS (A MODE)

Number	Symbol	Parameter	Test conditions	Limits		Unit	
				Min	Max		
—	f_{max}	Maximum repetitive frequency		20		MHz	
1	t_{TLH}	Output transition time	$C_L=50pF$ (\overline{RDY} , \overline{LATCH} , \overline{MPX} , \overline{MPX})		15	ns	
	t_{THL}				15		
2	t_{TLH}		$C_L=50pF$ (\overline{RAS} , \overline{CAS} , \overline{W})		10	ns	
	t_{THL}				10		
3	t_{PLH}	CLK— \overline{RAS} propagation time	$C_L=50pF$		34	ns	
	t_{PHL}				36		
4	t_{PLH}		$C_L=150pF$	10	36	ns	
	t_{PHL}			13	40		
5	t_{PLH}	MR, MW—CAS propagation time	$C_L=50pF$		41	ns	
	t_{PHL}				36		
6	t_{PLH}		CLK—CAS	$C_L=150pF$	14	43	ns
	t_{PHL}				13	40	
7	t_{PLH}	CLK— \overline{MPX} , \overline{MPX} propagation time	$C_L=50pF$	21	62	ns	
	t_{PHL}			21	62		
8	t_{PLH}		CLK— \overline{MPX} , \overline{MPX} propagation time	$C_L=50pF$	18	74	ns
	t_{PHL}				18	74	
9	t_{PLH}	MW— \overline{W} propagation time	$C_L=50pF$		48	ns	
	t_{PHL}				25		
10	t_{PLH}		$\overline{S0}$ — \overline{W} propagation time (when $\overline{S0}$ and $\overline{S1}$ are used)	$C_L=200pF$		52	ns
	t_{PHL}					34	
11	t_{PLH}	MW— \overline{W} propagation time (when $\overline{S0}$ and $\overline{S1}$ are not used)	$C_L=50pF$		20	ns	
	t_{PHL}				20		
12	t_{PLH}		$C_L=200pF$		24	ns	
	t_{PHL}				28		
13	t_{PLH}	CLK—RDY propagation time	$C_L=50pF$		36	ns	
14	t_{PHL}	MR, MW—RDY propagation time	$C_L=50pF$		36	ns	
15	t_{PLH}	MR, MW—LATCH propagation time	$C_L=50pF$		32	ns	
16	t_{PHL}	CLK—LATCH propagation time	$C_L=50pF$		32	ns	

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MEMORY ACCESS (B MODE)

Number	Symbol	Parameter	Test conditions	Limits		Unit	
				Min	Max		
—	f_{max}	Maximum repetitive frequency		20		MHz	
17	t_{TLH}	Output transition time	$C_L=50pF$ (RDY, \overline{LATCH} , MPX, \overline{MPX})		15	ns	
	t_{THL}				15		
18	t_{TLH}		$C_L=50pF$ (\overline{RAS} , \overline{CAS} , \overline{W})		10	ns	
	t_{THL}				10		
19	t_{PLH}	CLK- \overline{RAS} propagation time	$C_L=50pF$		34	ns	
	t_{PHL}				36		
20	t_{PLH}		$C_L=150pF$	10	36	ns	
	t_{PHL}			13	40		
21	t_{PLH}	propagation time	$C_L=50pF$		41	ns	
	t_{PHL}				36		
22	t_{PLH}		CLK- \overline{CAS}	$C_L=150pF$	14	43	ns
	t_{PHL}				13	40	
23	t_{PLH}	CLK- \overline{MPX} , \overline{MPX} propagation time	$C_L=50pF$	21	62	ns	
	t_{PHL}			21	62		
24	t_{PLH}	CLK- \overline{MPX} , \overline{MPX} propagation time	$C_L=50pF$	18	74	ns	
	t_{PHL}			18	74		
25	t_{PLH}	propagation time	$C_L=50pF$		48	ns	
	t_{PHL}				25		
26	t_{PLH}		$\overline{S0}-\overline{W}$	$C_L=200pF$		52	ns
	t_{PHL}					34	
27	t_{PLH}	CLK-RDY propagation time	$C_L=50pF$		36	ns	
28	t_{PHL}	MR, MW-RDY propagation time	$C_L=50pF$		36	ns	
29	t_{PLH}	MR, MW-LATCH propagation time	$C_L=50pF$		32	ns	
30	t_{PHL}	CLK-LATCH propagation time	$C_L=50pF$		32	ns	

INTERNAL REFRESH (CAS BEFORE RAS) (A MODE)

Number	Symbol	Parameter	Test conditions	Limits		Unit
				Min	Max	
31	t_{PLH}	CLK- \overline{RAS} propagation time	$C_L=50pF$		38	ns
	t_{PHL}				38	
32	t_{PLH}		$C_L=150pF$		41	ns
	t_{PHL}				41	
33	t_{PLH}	CLK- \overline{CAS} propagation time	$C_L=50pF$		31	ns
	t_{PHL}				41	
34	t_{PLH}		$C_L=150pF$		33	ns
	t_{PHL}				45	

INTERNAL REFRESH (CAS BEFORE RAS) (B MODE)

Number	Symbol	Parameter	Test conditions	Limits		Unit
				Min	Max	
35	t_{PLH}	CLK- \overline{RAS} propagation time	$C_L=50pF$		38	ns
	t_{PHL}				38	
36	t_{PLH}		$C_L=150pF$		41	ns
	t_{PHL}				41	
37	t_{PLH}	CLK- \overline{CAS} propagation time	$C_L=50pF$		31	ns
	t_{PHL}				33	
38	t_{PLH}		$C_L=150pF$		33	ns
	t_{PHL}				37	

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EXTERNAL REFRESH (RAS ONLY)

Number	Symbol	Parameter	Test conditions	Limits		Unit
				Min	Max	
39	t_{PLH}	RFRQ—RAS propagation time	$C_L=50pF$		23	ns
	t_{PHL}				23	
40	t_{PLH}		$C_L=150pF$		27	ns
	t_{PHL}				27	

TIMING REQUIREMENTS ($V_{CC}=5V\pm 10\%$, $T_a=0\sim 70^\circ C$)
MEMORY ACCESS (A MODE)

Number	Symbol	Parameter	Test conditions	Limits		Unit
				Min	Max	
41	t_{WH}	Clock pulse width (high level)		20		ns
42	t_{WL}	Clock pulse width (low level)		20		ns
43	t_{SU}	CLK—CS setup time		20		ns
44	t_h	CLK—CS hold time		20		ns
45	t_{SU}	CLK—S0 setup time		20		ns
46	t_h	CLK—S0 hold time		20		ns
47	t_{SU}	CLK—S1 setup time		20		ns
48	t_h	CLK—S1 hold time		20		ns
49	t_{SU}	CLK—MR setup time		20		ns
50	t_h	CLK—MR hold time		1.5CK+10	2.5CK-20	ns
51	t_{SU}	CLK—MW setup time		20		ns
52	t_h	CLK—MW hold time		1.0CK+10	2.0CK-20	ns
53	t_{SU}	CLK—BANK setup time		20		ns
54	t_h	CLK—BANK hold time		20		ns
55	t_{SU}	CLK—CAE0, CAE1 setup time		20		ns
56	t_h	MR, MW—CAE0, CAE1 hold time		20		ns
57	t_{WH}	Reset pulse width (high level)		20		ns
58	t_{rec}	CLK—RESET recovery time		20		ns

MEMORY ACCESS (B MODE)

Number	Symbol	Parameter	Test conditions	Limits		Unit
				Min	Max	
59	t_{WH}	Clock pulse width (high level)		20		ns
60	t_{WL}	Clock pulse width (low level)		20		ns
61	t_{SU}	CLK—CS setup time		20		ns
62	t_h	CLK—CS hold time		20		ns
63	t_{SU}	CLK—S0 setup time		20		ns
64	t_h	CLK—S0 hold time		20		ns
65	t_{SU}	CLK—S1 setup time		20		ns
66	t_h	CLK—S1 hold time		20		ns
67	t_{SU}	CLK—MR setup time		20		ns
68	t_h	CLK—MR hold time		2.0CK	2.5CK	ns
69	t_{SU}	CLK—MW setup time		20		ns
70	t_h	CLK—MW hold time		1.5CK	2.0CK	ns
71	t_{SU}	CLK—BANK setup time		20		ns
72	t_h	CLK—BANK hold time		20		ns
73	t_{SU}	CLK—CAE0, CAE1 setup time		20		ns
74	t_h	CLK—CAE0, CAE1 hold time		20		ns
75	t_{WH}	Reset pulse width (high level)		20		ns
76	t_{rec}	CLK—RESET recovery time		20		ns

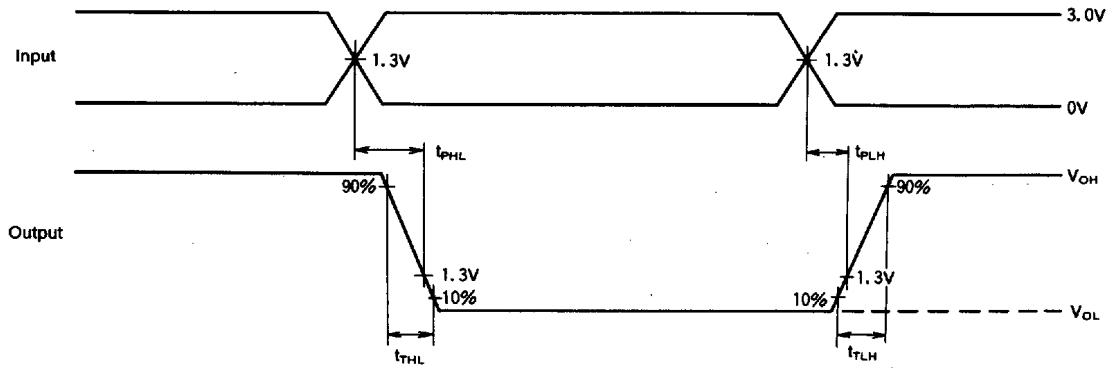
Note : The limits of 50, 52, 68 and 70 (max) assume the continuous access from MPU and do not show the limits of operation.

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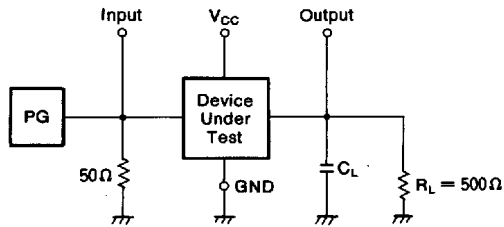


DRAM CONTROLLER

SWITCHING WAVEFORM



TEST CIRCUIT



- (1) The pulse generator (PG) has the following characteristics (10%~90%): $t_r=3\text{ns}$, $t_f=3\text{ns}$.
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

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