

M66212P/FP
M66213P/FP

2→1-LINE(×5)DATA SELECTOR

DESCRIPTION

The M66212P/FP and M66213P/FP are semiconductor integrated circuits consisting of five 2-line to 1-line data selectors/multiplexers.

FEATURES

- TTL level input $V_{IL}=0.8V$ max., $V_{IH}=2.0V$ min.
- High fan-out output ($I_{OL}=24mA$, $I_{OH}=-24mA$)
- High-speed 9 ns typ. ($C_L=50pF$, $V_{CC}=5V$)
- Low power dissipation $50\mu W$ /package maximum ($V_{CC}=5V$, $T_a=25^{\circ}C$, quiescent state)
- Suitable for 256K-or 1M-bit DRAM address drivers

APPLICATION

Data selector for microcomputer systems

FUNCTION

Use of the silicon gate process allows for high speed processing while maintaining low power dissipation and a high noise margin on the M66212/M66213. The circuit configuration is designed to suppress the switching noise due to increases in output current.

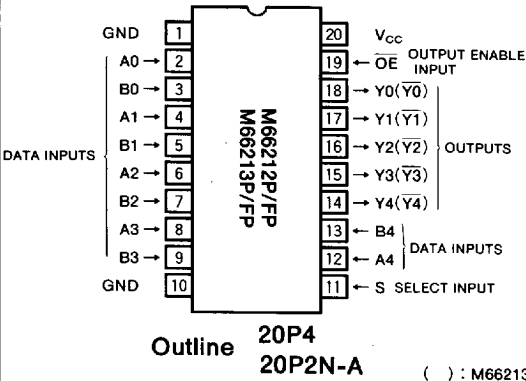
The M66212 is a data selector for non-inverted output while the M66213 is for inverted output.

The M66212/M66213 has five built-in data selector circuits, making the device suitable for an address driver for 256K-or 1M-bit dynamic RAMs.

The 2-line signals are applied to data inputs A and B, and after one of the data inputs has been selected by select input S, it is output at pin Y.

By applying 2-bit parallel data to A and B, and connecting the output of a binary counter to S, A and B data will be output at Y synchronous with the clock pulse in the order A-

PIN CONFIGURATION (TOP VIEW)



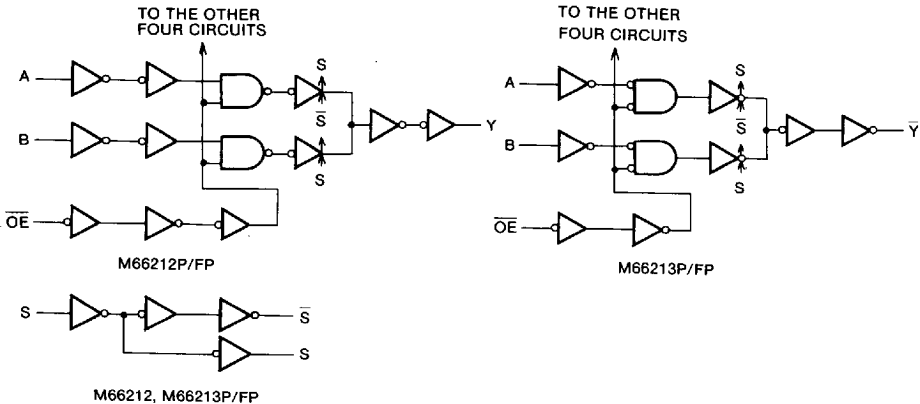
B. Both S and output-enable input $\overline{OE}$ are common to all five circuits. When $\overline{OE}$ is high, all outputs of the M66212 become low and those of the M66213 become high, irrespective of the data on the inputs.

FUNCTION TABLE

OE	Inputs			Output
	S	A	B	
H	X	X	X	Y(Y)
L	L	L	X	L(H)
L	L	H	X	H(L)
L	H	X	L	L(H)
L	H	X	H	H(L)

Note 1 : X : Don't care.
() : M66213P/FP

LOGIC DIAGRAM



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2→1-LINE(×5)DATA SELECTOR

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage		−0.5~+7.0	V
V _I	Input voltage		−0.5~V _{CC} +0.5	V
V _O	Output voltage		−0.5~V _{CC} +0.5	V
I _{IK}	Input protection diode current	V _I < 0V	−20	mA
		V _I > V _{CC}	+20	
I _{OK}	Output parasitic diode current	V _O < 0V	−20	mA
		V _O > V _{CC}	+20	
I _O	Output current		±50	mA
I _{CC}	Power supply/GND current	V _{CC} , GND	±200	mA
P _d	Power dissipation		500	mW
T _{stg}	Storage temperature		−65~+150	°C

RECOMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V _{CC}	Supply voltage	4.5		5.5	V
V _I	Input voltage	0		V _{CC}	V
V _O	Output voltage	0		V _{CC}	V
T _{opr}	Storage temperature	0		70	°C

ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits					Unit
			25°C			0~70°C		
			Min	Typ	Max	Min	Max	
V _{IH}	High-level input voltage	V _O =0.1, V _{CC} =0.1V, I _O =20μA	2.0			2.0		V
V _{IL}	Low-level input voltage	V _O =0.1, V _{CC} =0.1V, I _O =20μA			0.8		0.8	V
V _{OH}	High-level output voltage	V _I = V _{IH} , V _{IL} I _{OH} = -20μA	V _{CC} -0.1			V _{CC} -0.1		V
		I _{OH} = -24mA, V _{CC} =4.5V	3.83			3.70		
V _{OL}	Low-level output voltage	V _I = V _{IH} , V _{IL} I _{OL} = 20μA			0.1		0.1	V
		I _{OL} = 24mA, V _{CC} =4.5V			0.44		0.53	
I _{IH}	High-level input current	V _I = V _{CC}			0.1		1.0	μA
I _{IL}	Low-level input current	V _I = GND			0.1		1.0	μA
I _{CC}	Quiescent supply current	V _I = V _{CC} , GND, I _O = 0μA			10.0		100	μA
ΔI _{CC}	Maximum quiescent supply current	V _I = 2.4V, 0.4V (Note 2)			2.7		2.9	mA

Note 2 : Only one input is set to this value and other inputs are tied to V_{CC} or GND.

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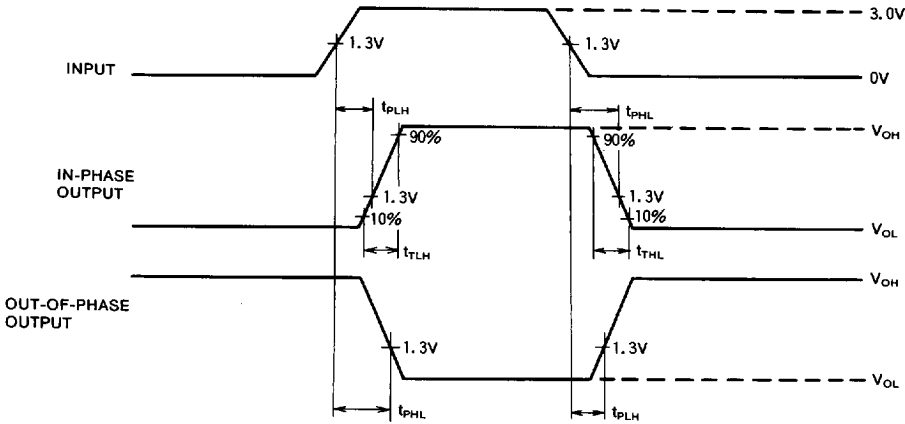
SWITCHING CHARACTERISTICS (V_{CC} = 5V±10%, T_a = 0~70°C)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t _{TLH}	Output transition time	C _L =50pF		5	10	ns
t _{THL}				3	10	
t _{TLH}		C _L =200pF		11	20	ns
t _{THL}				8	20	
t _{PLH}	A, B—Y, $\bar{Y}$ propagation time	C _L =50pF		9	21	ns
t _{PHL}				11	21	
t _{PLH}		C _L =200pF		11	27	ns
t _{PHL}				15	27	
t _{PLH}	S—Y, $\bar{Y}$ propagation time	C _L =50pF		12	23	ns
t _{PHL}				14	23	
t _{PLH}		C _L =200pF	7	13	28	ns
t _{PHL}			7	17	28	
t _{PLH}	$\overline{OE}$ —Y, $\bar{Y}$ propagation time	C _L =50pF		12	21	ns
t _{PHL}				12	21	
t _{PLH}		C _L =200pF		13	26	ns
t _{PHL}				15	26	
C _I	Input capacitance				10	pF
C _{PD}	Power dissipation capacitance (Note 3)			40		pF

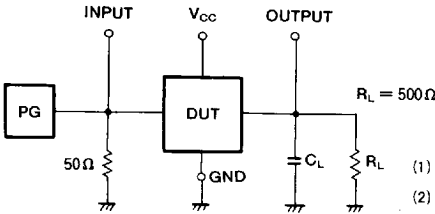
Note 3 : C_{PD} is an internal equivalent capacitance calculated according to the operating dissipation current with no load (per selector). The dynamic dissipation current can be calculated from the following equation under a no load condition.

$$P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$$

TIMING DIAGRAM



TEST CIRCUIT



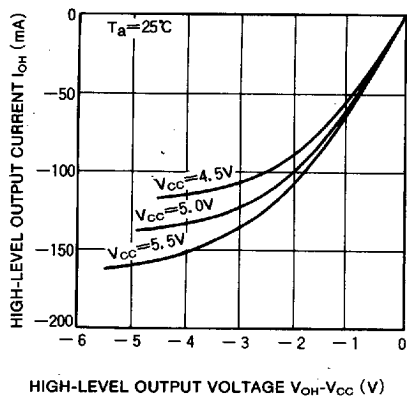
- (1) Characteristics of pulse generator (PG) (10%—90%) $t_r = 3\text{ns}$, $t_f = 3\text{ns}$
- (2) C_L includes stray probe and wiring capacitance.

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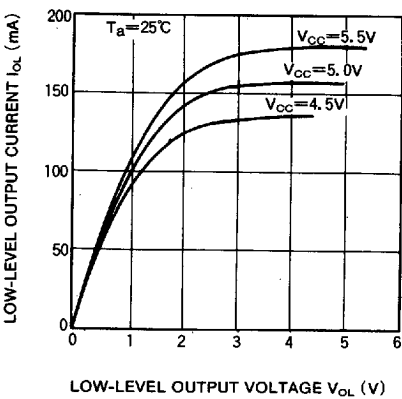


TYPICAL CHARACTERISTICS

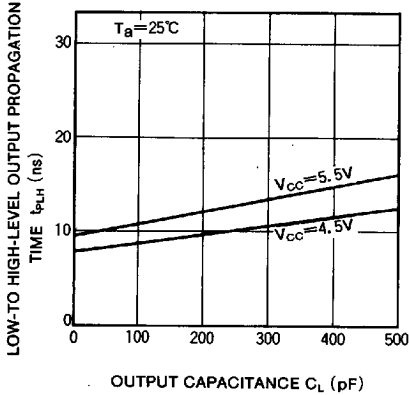
HIGH-LEVEL OUTPUT CURRENT VS
HIGH-LEVEL OUTPUT VOLTAGE



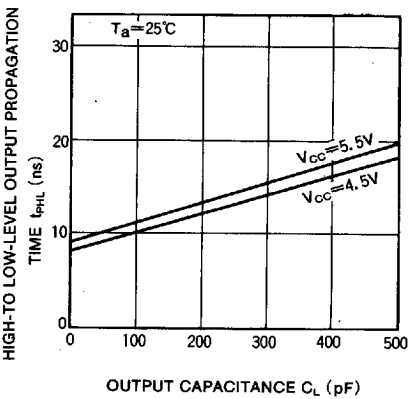
LOW-LEVEL OUTPUT CURRENT VS
LOW-LEVEL OUTPUT VOLTAGE



LOW-TO-HIGH-LEVEL OUTPUT PROPAGATION
TIME VS LOAD CAPACITANCE



HIGH-TO-LOW-LEVEL OUTPUT PROPAGATION
TIME VS LOAD CAPACITANCE



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