

M66310P/FP

16-BIT LED DRIVER WITH SHIFT REGISTER AND LATCH

DESCRIPTION

M66310P/FP is a LED array driver having a 16bit serial-input and parallel output shiftregister function with direct coupled reset input and output latch function.

This product guarantees the output electric current of 24mA which is sufficient for cathode common LED drive, capable of flowing 16bits continuously at the same time.

Parallel output is open drain output.

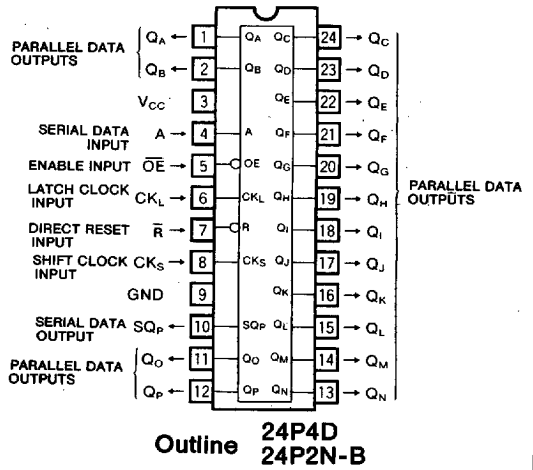
In addition, as this product has been designed in complete CMOS, power consumption can be greatly reduced when compared with conventional BIPOLAR or Bi-CMOS products.

Furthermore, pin lay-out ensures the realization of an easy printed circuit.

FEATURES

- Cathode common LED drive
- High output current
all parallel output $I_{OH} = -24\text{mA}$
simultaneous lighting available
- Low power dissipation : 100 μ W/package (max)
($V_{CC} = 5\text{V}$, $T_a = 25^\circ\text{C}$, quiescent state)
- High noise margin
schmitt input circuit provides responsiveness to a long line length.
- Equipped with direct-coupled reset
- Open drain output
(except serial data output)
- Wide operating temperature range
: $T_a = -40 \sim +85^\circ\text{C}$
- Pin lay-out facilitates printed circuit wiring. (This lay-out facilitates cascade connection and LED connection.)

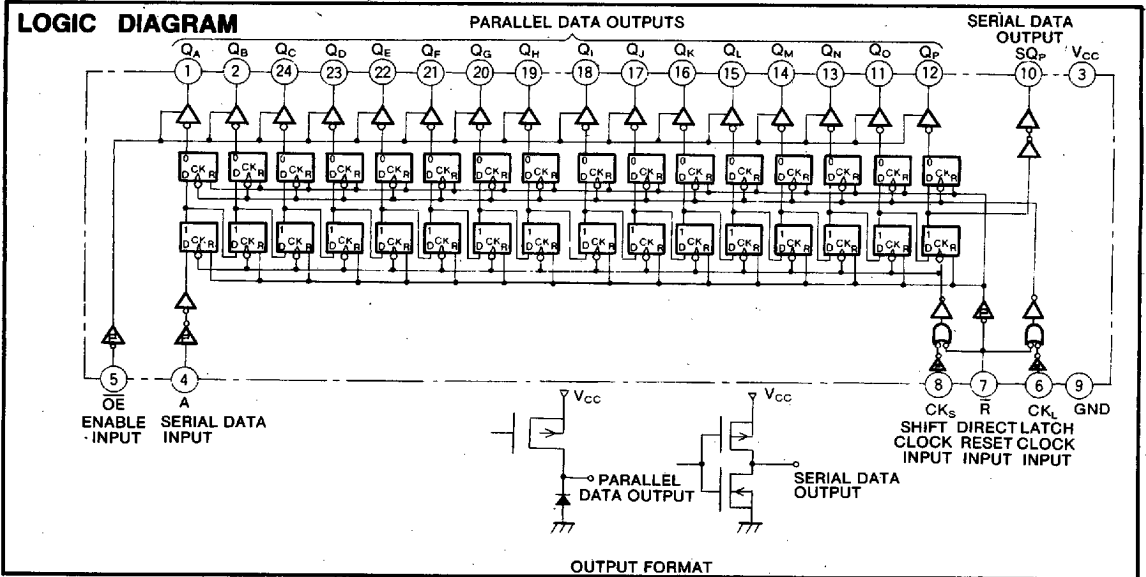
PIN CONFIGURATION (TOP VIEW)



APPLICATION

- LED array drive of BUTTON TELEPHONE
- LED array drive of ERASER of a PPC copier
- Other various LED modules

LOGIC DIAGRAM



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16-BIT LED DRIVER WITH SHIFT REGISTER AND LATCH

FUNCTIONAL DESCRIPTION

As M66310P/FP uses silicon gate CMOS process, it realizes high-speed and high-output currents sufficient for LED drive while maintaining low power consumption and allowance for high noises.

Each bit of a shiftregister consists of two flip-flops having independent clocks for shifting and latching.

As for clock input, shift clock input CK_S and latch clock input CK_L are independent from each other, shift and latch operations being made when "L" changes to "H".

Serial data input A is the data input of the first-step shiftregister and the signal of A shifts shifting registers one by one when a pulse is impressed to CK_S. When A is "L", the signal of "L" shifts.

When the pulse is impressed to CK_L, the contents of the

shifting register at that time are stored in a latching register, and they appear in the outputs from Q_A~Q_P.

Outputs from Q_A~Q_P are open drain outputs.

To extend the number of bits, use the serial data output SQ_P which shows the output of the shifting register of the 16th bit.

If CK_S and CK_L are connected, the state of the shifting register with one clock delay is outputted to Q_A~Q_P.

When reset input \bar{R} is changed to "L", Q_A~Q_P and SQ_P are reset. In this case, shifting and latching registers are reset.

If "H" is impressed to output enable input OE, Q_A~Q_P reaches the high impedance state, but SQ_P does not reach the high impedance state. Furthermore, change in OE does not affect shift operation.

FUNCTION TABLE (Note : 1)

Operation mode	Input					PARALLEL DATA Output																Serial data output SQ _P	Remarks		
	R	CK _S	CK _L	A	OE	Q _A	Q _B	Q _C	Q _D	Q _E	Q _F	Q _G	Q _H	Q _I	Q _J	Q _K	Q _L	Q _M	Q _N	Q _O	Q _P				
Reset	L	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	L	—	
Shift latch operation	Shift t ₁	H	↑	X	H	L	Q _A ⁰	Q _B ⁰	Q _C ⁰	Q _D ⁰	Q _E ⁰	Q _F ⁰	Q _G ⁰	Q _H ⁰	Q _I ⁰	Q _J ⁰	Q _K ⁰	Q _L ⁰	Q _M ⁰	Q _N ⁰	Q _O ⁰	Q _P ⁰	q _O ⁰	Output lighting "H"	
	Latch t ₂	H	X	↑	X	L	H	q _A ⁰	q _B ⁰	q _C ⁰	q _D ⁰	q _E ⁰	q _F ⁰	q _G ⁰	q _H ⁰	q _I ⁰	q _J ⁰	q _K ⁰	q _L ⁰	q _M ⁰	q _N ⁰	q _O ⁰	q _P ⁰	q _O ⁰	—
	Shift t ₁	H	↑	X	L	L	Q _A ⁰	Q _B ⁰	Q _C ⁰	Q _D ⁰	Q _E ⁰	Q _F ⁰	Q _G ⁰	Q _H ⁰	Q _I ⁰	Q _J ⁰	Q _K ⁰	Q _L ⁰	Q _M ⁰	Q _N ⁰	Q _O ⁰	Q _P ⁰	q _O ⁰	q _O ⁰	Output lights-out "L"
Output disable	X	X	X	X	H	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	q _P	—

- Note 1 : ↑ : Change from low-level to high-level
 Q⁰ : Output state Q before CK_L changed
 X : Irrelevant
 q⁰ : Contents of shift register before CK_S changed
 q : Contents of shift register
 t₁, t₂ : t₂ is set after t₁ is set
 Z : High impedance

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16-BIT LED DRIVER WITH SHIFT REGISTER AND LATCH

ABSOLUTE MAXIMUM RATINGS (T_a=-40~+85°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage		-0.5~+7.0	V
V _I	Input voltage		-0.5~V _{CC} +0.5	V
V _O	Output voltage		-0.5~V _{CC} +0.5	V
I _{IK}	Input protection diode current	V _I < 0V	-20	mA
		V _I > V _{CC}	20	
I _{OK}	Output parasitic diode current	V _O < 0V	-20	mA
		V _O > V _{CC}	20	
I _O	Output current per output pin	Q _A ~Q _P	-50	mA
		SQ _P	±25	
I _{CC}	Supply/GND current	V _{CC} , GND	-410, +20	mA
P _d	Power dissipation	(Note 2)	500	mW
T _{stg}	Storage temperature range		-65~+150	°C

Note 2 : M66310FP ; T_a=-40~+70°C, T_a=70~85°C are derated at -6mW/°C.

RECOMMENDED OPERATING CONDITIONS (T_a=-40~+85°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V _{CC}	Supply voltage	4.5	5	5.5	V
V _I	Input voltage	0		V _{CC}	V
V _O	Output voltage	0		V _{CC}	V
Topr	Operating temperature range	-40		+85	°C

ELECTRICAL CHARACTERISTICS (V_{CC}=4.5~5.5V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits				Unit	
			T _a =25°C			T _a =-40~+85°C		
			Min	Typ	Max	Min		Max
V _{T+}	Positive-going threshold voltage	V _O = 0.1V, V _{CC} = 0.1V I _O = 20μA	0.35XV _{CC}		0.7XV _{CC}	0.35XV _{CC}	0.7XV _{CC}	V
V _{T-}	Negative-going threshold voltage	V _O = 0.1V, V _{CC} = 0.1V I _O = 20μA	0.2XV _{CC}		0.55XV _{CC}	0.2XV _{CC}	0.55XV _{CC}	V
V _{OH}	High-level output voltage Q _A ~Q _P	V _I = V _{T+} , V _{T-} V _{CC} = 4.5V	I _{OH} = -20μA	V _{CC} - 0.1		V _{CC} - 0.1		V
			I _{OH} = -24mA	3.83		3.66		
V _{OH}	High-level output voltage SQ _P	V _I = V _{T+} , V _{T-} V _{CC} = 4.5V	Note3 I _{OH} = -40mA	3.50		3.25		V
			I _{OH} = -20μA	V _{CC} - 0.1		V _{CC} - 0.1		
V _{OL}	Low-level output voltage SQ _P	V _I = V _{T+} , V _{T-} V _{CC} = 4.5V	I _{OL} = -4mA	3.83		3.66		V
			I _{OL} = 20μA			0.1	0.1	
I _{IH}	High-level input current	V _I = V _{CC} , V _{CC} = 5.5V			0.5		5.0	μA
I _{IL}	Low-level input current	V _I = GND, V _{CC} = 5.5V			-0.5		-5.0	μA
I _O	Maximum output leakage current Q _A ~Q _P	V _I = V _{T+} , V _{T-} V _{CC} = 5.5V	V _O = V _{CC}		1.0		10.0	μA
			V _O = GND		-1.0		-10.0	
I _{CC}	Quiescent supply current	V _I = V _{CC} , GND, V _{CC} = 5.5V			20.0		200.0	μA

Note 3 : M66310 is used under the condition of an output current I_{OH} = -40mA, the number of simultaneous drive outputs is restricted as shown in the Duty Cycle - I_{OH} of Standard characteristics.

6249826 0020680 287

16-BIT LED DRIVER WITH SHIFT REGISTER AND LATCH

SWITCHING CHARACTERISTICS (V_{CC}=5V)

Symbol	Parameter	Test conditions	Limits					Unit
			T _a =25°C			T _a =-40~+85°C		
			Min	Typ	Max	Min	Max	
f _{max}	Maximum clock frequency	C _L =50pF R _L =1kΩ (Note 5)	5			4		MHz
t _{PLH}	Low-level to high-level and high-level to low-level				100		130	ns
t _{PHL}	output propagation time (CK _S -SQ _P)				100		130	ns
t _{PHL}	High-level to low-level output propagation time (R-SQ _P)				100		130	ns
t _{PHZ}	High-level to low-level output propagation time (R-Q _A ~Q _P)				150		200	ns
t _{PZH}	Low-level to high-level and high-level to low-level				100		130	ns
t _{PHZ}	output propagation time (CK _L -Q _A ~Q _P)				150		200	ns
t _{PZH}	Output enable time to low-level and high-level				100		130	ns
t _{PHZ}	(OE-Q _A ~Q _P)				150		200	ns
C _I	Input Capacitance				10		10	pF
C _O	Output Capacitance	OE=V _{CC}		15		15	pF	
C _{PD}	Power dissipation Capacitance (Note 4)		11				pF	

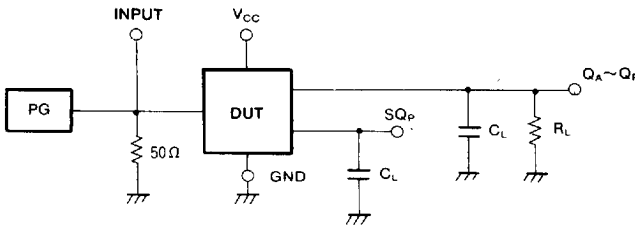
Note 4 : C_{PD} is the internal capacitance of the IC calculated from operation supply current under no-load conditions. (per latch)
 The power dissipated during operation under no-load conditions is calculated using the following formula:
 $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_l + I_{CC} \cdot V_{CC}$

TIMING REQUIREMENTS (V_{CC}=5V)

Symbol	Parameter	Test conditions	Limits					Unit
			T _a =25°C			T _a =-40~+85°C		
			Min	Typ	Max	Min	Max	
t _w	CK _S , CK _L , R pulse width	(Note 5)	100			130		ns
t _{su}	A setup time with respect to CK _S		100			130		ns
t _{su}	CK _S setup time with respect to CK _L		100			130		ns
t _h	A hold time with respect to CK _S		10			15		ns
t _{rec}	R, recovery time with respect to CK _S , CK _L		50			70		ns

Note 5 : Test Circuit

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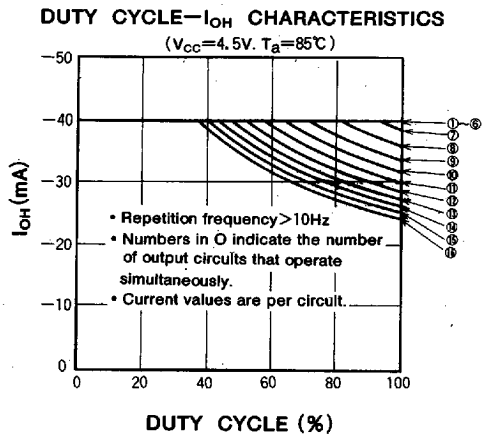
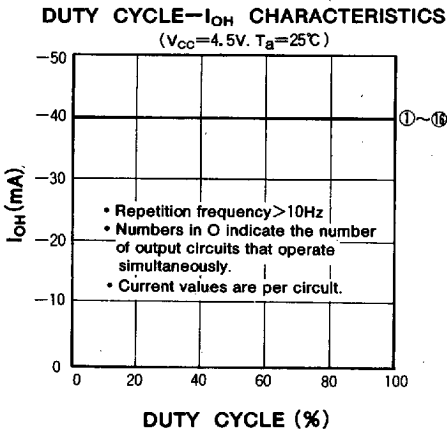
- (1) The pulse generator (PG) has the following characteristics (10%~90%) : t_r=6ns, t_f=6ns
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

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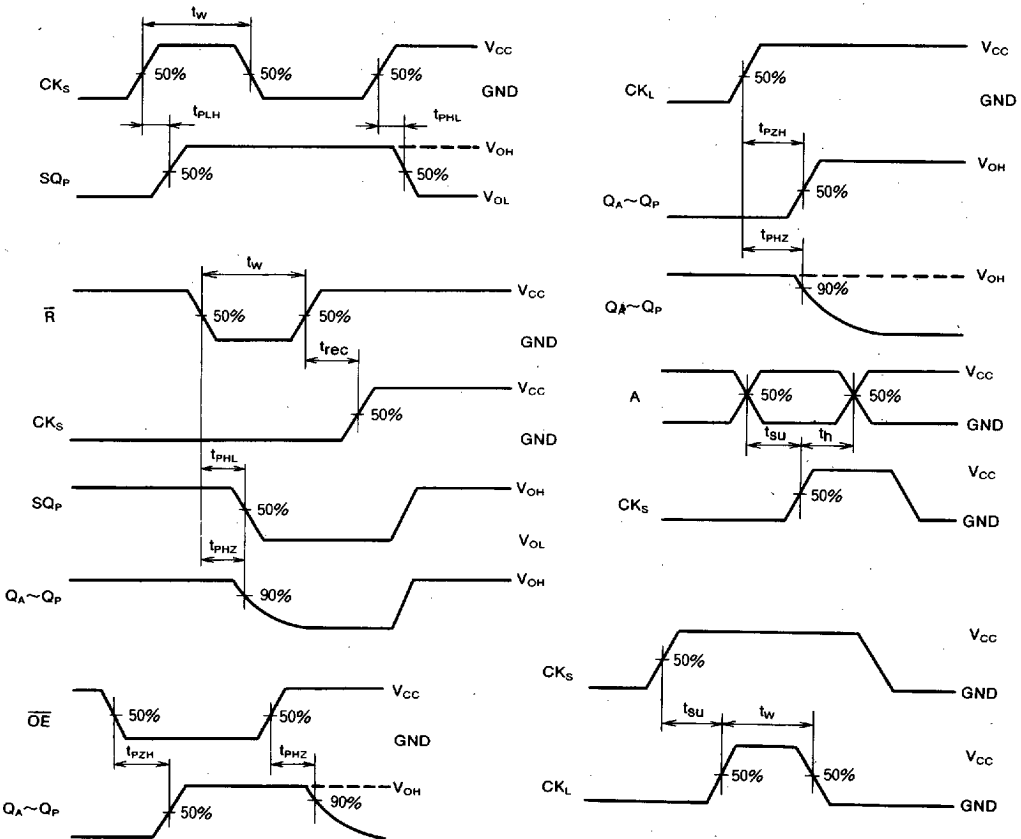


16-BIT LED DRIVER WITH SHIFT REGISTER AND LATCH

TYPICAL CHARACTERISTICS



TIMING DIAGRAM



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