

M66500SP/FP

PROGRAMMABLE BUFFERED I/O EXPANDER

DESCRIPTION

The M66500SP/FP is a large-scale integrated circuit chip for programmable high-speed I/O interface, manufactured using a Bi-CMOS process and is suitable for 8- and 16-bit high-speed CPU I/O ports. The device is operated by a single 5V power supply and consists of three sets of 8-bit I/O ports, two sets of 8-bit high-withstand voltage output-only ports, and one 4-bit input-only port.

FEATURES

- I/O expandable up to 44 bits
- No-wait direct connection with 12MHz CPU
- Output pattern write in the input mode
- Output pin state read from CPU
- Transistor array drive
- 16-bit high-withstand voltage output-only port, 35V and 48mA*
- TTL input level at CPU-side pin
- CMOS-level Schmitt trigger input for I/O pin

APPLICATION

I/O port expander for microprocessors M37450, M37700 and M5L8085.

FUNCTIONAL DESCRIPTION

The M66500P/FP is a high-speed general-purpose programmable I/O expander that can be directly connected to high-speed CPUs with 0 wait states. The device consists of three sets of 8-bit I/O ports (ports A, B and C), two sets of 8-bit high-withstand voltage output-only ports (ports E and F), and a 4 bit input-only port G. These I/O ports can be programmed as input or output ports.

Ports A, B and C consist of CMOS circuits and are capable of driving transistor arrays with $I_{OH} = -2.5mA$ and $I_{OL} = 2.5mA$.

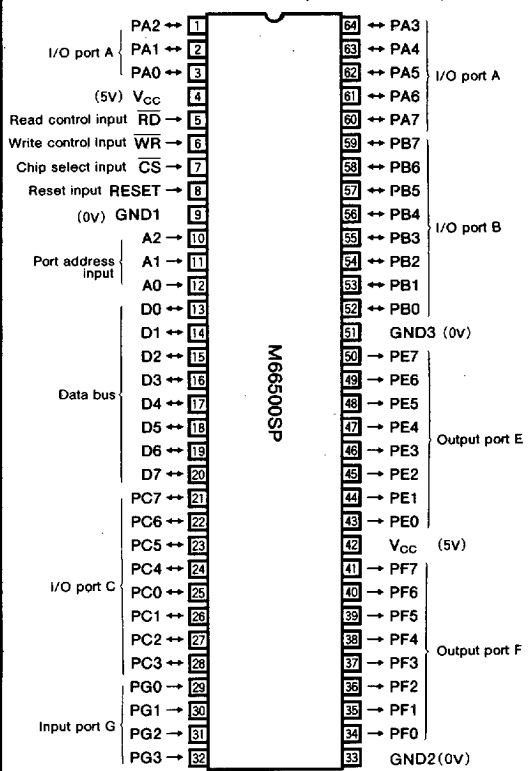
Ports E and F are high-withstand voltage, high-current-drive, bipolar open collector outputs. Ports G is an input-only port with hysteresis input.

Port C can be divided into a pair of 4-bit I/O ports. Any bit can be set or reset if the port is originally set for output.

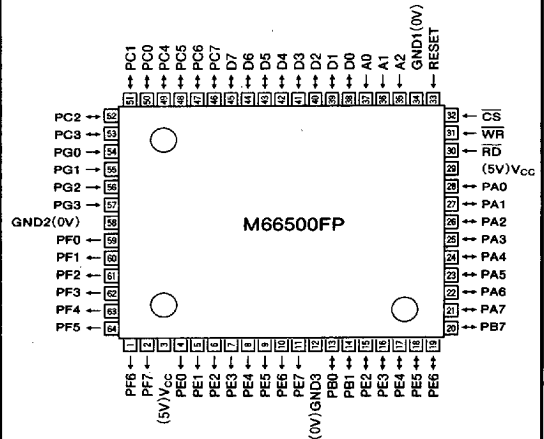
If the reset input (RESET) becomes high-level, output-only ports E and F enters a high-level output disable status, I/O ports are set to input mode, and all other ports enter the high-impedance state.

* : I_{OL} of the M66500FP is 24mA.

PIN CONFIGURATION (TOP VIEW)



Outline 64P4B



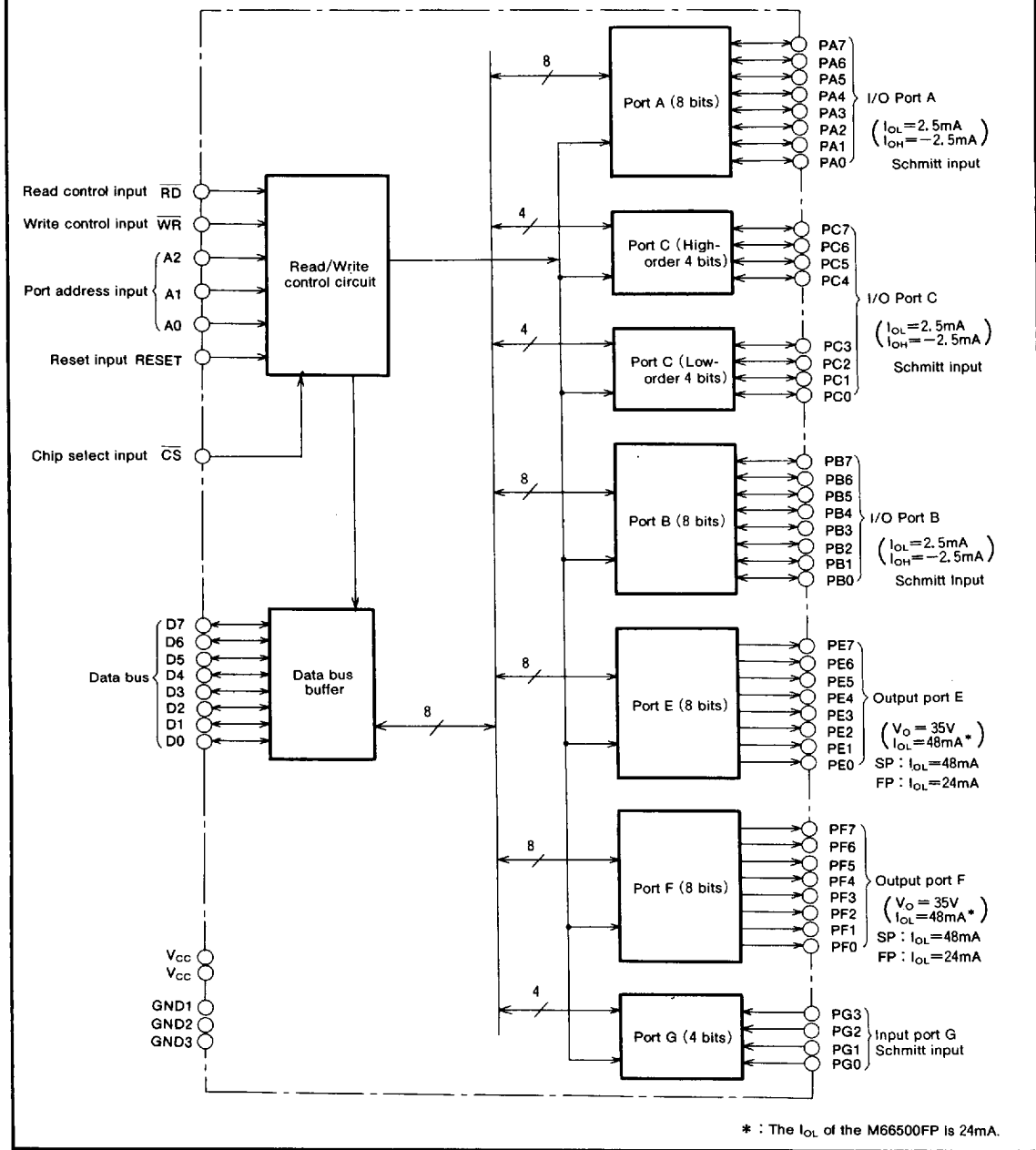
Outline 64P6W-B

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PROGRAMMABLE BUFFERED I/O EXPANDER

BLOCK DIAGRAM



GND1 (SP: 9-pin, FP: 34-pin) : For data bus, port C, port G and internal logic unit.
 GND2 (SP: 33-pin, FP: 58-pin) : For output unit of port F
 GND3 (SP: 51-pin, FP: 12-pin) : For I/O buffer of port A and port B, and port E output.

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FUNCTION (Reference Bloon Diagram)

RD (read) Input

If the input is low-level, the port input data or port latch contents appear at the data bus.

WR (write) Input

The data on the data bus is written to the control register or to the port latch on the leading edge transition from low-level to high-level.

A0, A1, A2 (Port Selection) Input

The low-order three bits of the address bus are used for selection of each port and control register. See Table 1 for the basic functions.

RESET Input

Clears the control register with high level input. In this case, I/O ports A, B and C enter the input mode (high-impedance state) and output-only ports E and F enter the disable state (high-level output status). The data in the port latch is maintained.

CS (Chip Select) Input

Communication with CPU becomes possible with low-level input. If the input is high-level, the data bus maintains the high-impedance state and control from MPU is ignored. The status of each port and the content of the port latch are not affected.

Read/Write Control Circuit

Control signals from the MPU sets the status of each port and enables data transfer between the data bus and ports.

Data bus buffer

8-bit bi-directional bus buffer to transfer data of a data bus.

Port A and Port B

Ports A and B are 8-bit I/O ports with an input buffer and an output latch buffer and are set to input or output ports by the control command from the MPU. The output circuit consists of a CMOS 3-state totem pole circuit. The output sink current I_{OL} is 2.5mA, the output source current I_{OH} is -2.5mA and transistor array drive is possible. The device has CMOS-level Schmitt trigger inputs.

If the port is set for output, the data on the data bus is written to the port latch on \overline{WR} rise and the data is output to the port. If the port is set for output and \overline{RD} is low-level, the port output data appears on the data bus.

If the port is set for input and \overline{RD} is low-level, the data input to the port appears on the data bus. If the port is set for input and \overline{WR} is low-level, the data in the data bus is written to the port latch on \overline{WR} rise. Therefore port output data is available after the port is set for output.

The content of port latch is not fixed at power on.

Port C

Port C can be divided into a pair of 4-bit I/O ports in addition to the functions provided by ports A and B. If the port is set for output, each bit can be set/reset individually.

Port E and Port F

Port E and F are 8-bit output-only ports with output withstand voltage $V_0 = 35V$, output sink current I_{OL} is 48mA*. The output circuit is an open-collector using bipolar transistors.

If the port is selected, the data in the data bus is written to the port latch at \overline{WR} rise and if the port is set to enable status, the latch data is output at the port. If the port is set to disable status, the port output is high-level, irrespective of latch data.

If $\overline{RD} =$ low-level, the content of port latch appears at the data bus.

* : The I_{OL} of the M66500FP is 24mA.

Port G

Port G is a 4-bit input-only port with a Schmitt trigger circuit. If \overline{RD} is low-level, the data of the port appears in the low-order 4 bits of the data bus.

NOTE : Data from the data bus is available only to the selected port including the control register, or both the port output data and port status will not change unless the port is selected and \overline{WR} rises.

Table 1 Basic functions.

A2	A1	A0	CS	RD	WR	Function
0	0	0	0	0	1	Data bus ← Port A
0	0	1	0	0	1	Data bus ← Port B
0	1	0	0	0	1	Data bus ← Port C
0	1	1	0	0	1	Data bus ← Port G
1	0	0	0	0	1	Data bus ← Port E latch data
1	0	1	0	0	1	Data bus ← Port F latch data
0	0	0	0	1	$\overline{\mathcal{J}}$	Port A ← Data bus
0	0	1	0	1	$\overline{\mathcal{J}}$	Port B ← Data bus
0	1	0	0	1	$\overline{\mathcal{J}}$	Port C ← Data bus
1	0	0	0	1	$\overline{\mathcal{J}}$	Port E ← Data bus
1	0	1	0	1	$\overline{\mathcal{J}}$	Port F ← Data bus
1	1	1	0	1	$\overline{\mathcal{J}}$	Control register ← Data bus
X	X	X	1	X	X	Data bus is in the high-impedance state.

0 indicates low-level and 1 indicates high-level.

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Control Word

When (A0, A1, A2, WR, D7) = (1, 1, 1, \bar{x} , 1), the data in the data bus is regarded as the control word and the port status is set, or when (1, 1, 1, \bar{x} , 0), a Port C bit is set/reset. See Figure 1 and 2.

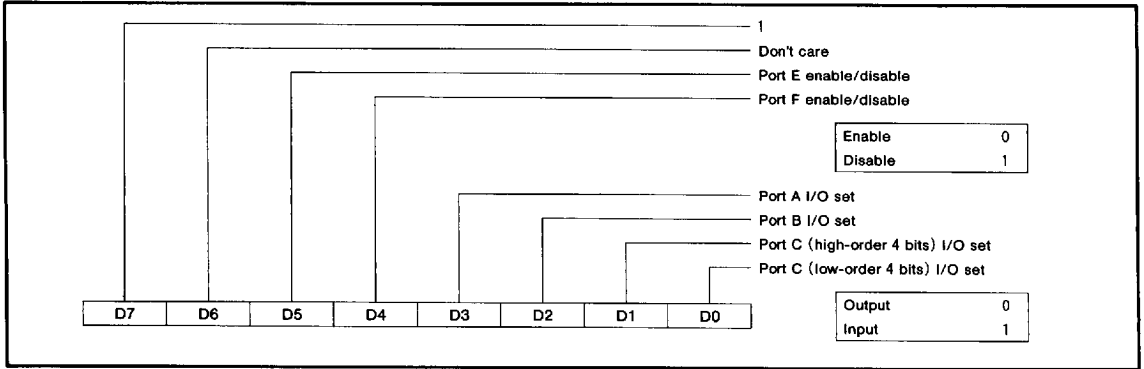


Fig. 1 Port status set control word

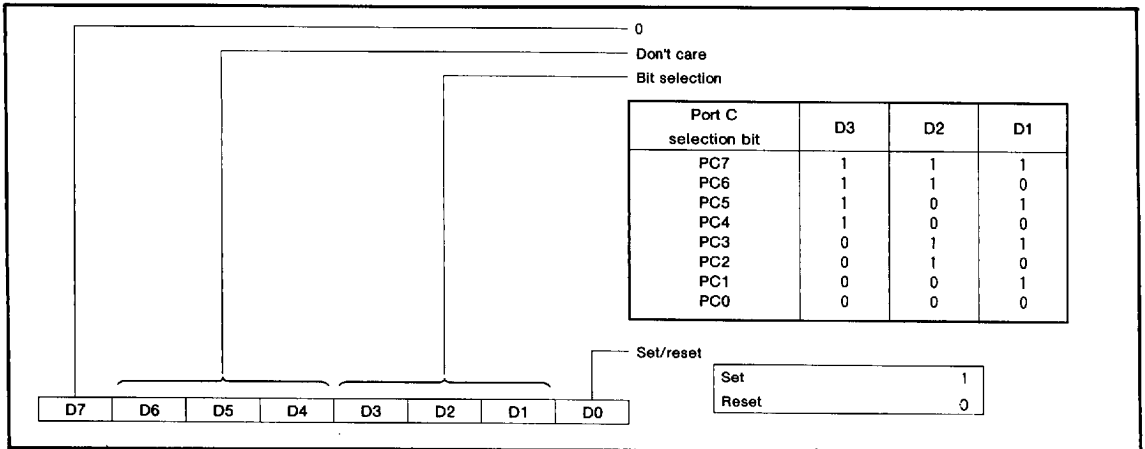


Fig. 2 Port C bit set/reset control word

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ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit	
V_{CC}	Supply voltage		-0.3~+7	V	
V_I	Input voltage		-0.3~ $V_{CC}+0.3$	V	
V_O	Output voltage		-0.3~ $V_{CC}+0.3$	V	
P_d	Power dissipation	M66500SP	$T_a=25^\circ\text{C}$ when a single IC is used (Note 1)	1.9	W
		M66500FP	$T_a=25^\circ\text{C}$ when a single IC is used. (Note 2)	1.4	
T_{stg}	Storage temperature		-65~+150	$^\circ\text{C}$	

Note 1 : $T_a \geq 25^\circ\text{C}$ is derated at 15.4mW/ $^\circ\text{C}$.

2 : $T_a \geq 25^\circ\text{C}$ is derated at 11mW/ $^\circ\text{C}$.

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit	
			Min.	Typ.	Max.		
V_{CC}	Supply voltage		4.5	5	5.5	V	
V_O	High-level output voltage	$I_{OH} \leq 250\mu\text{A}$ $V_{OL} \leq 0.6\text{V}$ (M66500SP) $V_{OL} \leq 0.5\text{V}$ (M66500FP)	0		35	V	
I_{OL}	Low-level output current		Ports E, F	0		48	mA
				0		24	
T_{opr}	Operating temperature		-20		+75	$^\circ\text{C}$	

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, $T_a = -20 \sim +75^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.*	Max.	
V_{IH}	High-level input voltage	Control pin	2			V
V_{IL}	Low-level input voltage	Data bus (Note 3)			0.8	V
V_{T+}	Upper threshold voltage	Ports A, B, C		2.0	2.8	V
		Port G		2.7	3.5	
V_{T-}	Lower threshold voltage	Ports A, B, C	0.8	1.3		V
		Port G	1.1	1.9		
V_{OH}	High-level output voltage	Data bus	$I_{OH} = -2.5\text{mA}$			V
V_{OL}	Low-level output voltage	Ports A, B, C	$I_{OL} = 2.5\text{mA}$		0.45	V
V_{OL}	Low-level output voltage	Port E, F	$I_{OL} = 48\text{mA}$ (M66500SP)		0.6	V
			$I_{OL} = 24\text{mA}$ (M66500FP)		0.5	
I_{OH}	High-level output current	Port E, F	$V_O = 35\text{V}$		250	μA
I_I	Input leakage current		$V_I = 0 \sim V_{CC}$		± 10	μA
I_{OZ}	Off-state output current		$V_O = 0 \sim V_{CC}$		± 10	μA
I_{CC}	Supply current	All ports high-level output			5	mA
		All ports low-level output	M66500SP	80	110	
C_I	Input pin capacitance	$f = 1\text{MHz}$			10	pF
$C_{I/O}$	I/O pin capacitance	0V except measuring pins			20	pF

Note 3 : The control pins are \overline{RD} , \overline{WR} , \overline{RESET} , \overline{CS} , A2, A1 and A0 pins.

* : Typical values are at $T_a = 25^\circ\text{C}$, $V_{CC} = 5\text{V}$.

TIMING REQUIREMENTS ($T_a = -20 \sim +75^\circ\text{C}$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits		Unit
			Min.	Max.	
$t_{W(R)}$	Read pulse width	$t_{SU(A-R)} = 0\text{ns}$ $t_{SU(A-R)} \geq 40\text{ns}$	160		ns
			120		
$t_{SU(PE-R)}$	Peripheral setup time before read		0		ns
$t_{H(R-PE)}$	Peripheral hold time after read		0		ns
$t_{SU(A-R)}$	Address setup time before read		0		ns
$t_{H(R-A)}$	Address hold time after read		0		ns
$t_{W(W)}$	Write pulse width		120		ns
$t_{SU(DQ-W)}$	Data setup time before write		40		ns
$t_{H(W-DQ)}$	Data hold time after write		0		ns
$t_{SU(A-W)}$	Address setup time before write		0		ns
$t_{H(W-A)}$	Address hold time after write		0		ns

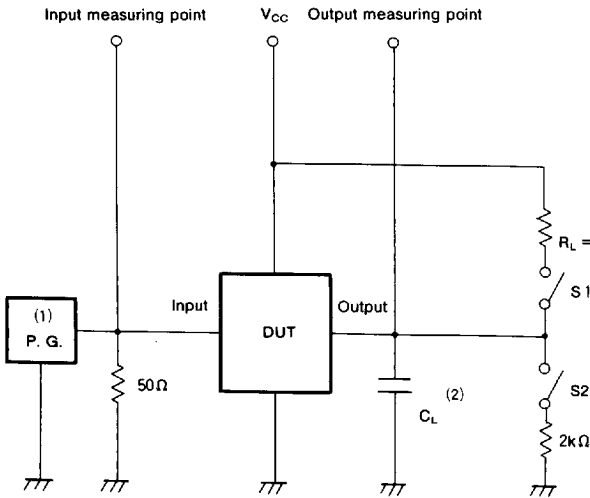
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SWITCHING CHARACTERISTICS (T_a = -20 ~ +75°C, V_{CC} = 5V ± 10%, unless otherwise noted)

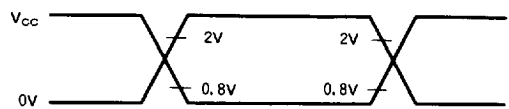
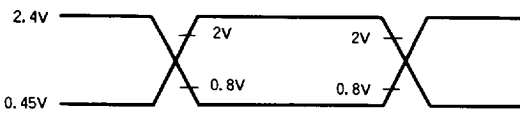
Symbol	Parameter	Test conditions	Limits		Unit
			Min.	Max.	
t _{PZH(R-DQ)}	Propagation time from read to data output	t _{SU(A-R)} = 0 ns C _L = 150pF (Note 4)		120	ns
t _{PZL(R-DQ)}				85	
t _{PHZ(R-DQ)}	Propagation time from read to data floating	C _L = 150pF (Note 4)	10	85	ns
t _{PLZ(R-DQ)}					
t _{PHL(W-PE)}	Propagation time from write to output	Ports A, B, C		200	ns
t _{PLH(W-PE)}		Ports E, F		250	
		C _L = 150pF, R _L = 110Ω (Note 4)			

Note 4: Test Circuit

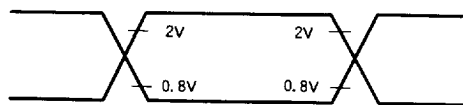


- (1) The pulse generator (PG) has the following characteristics: t_r = 6ns, t_f = 6ns, Z₀ = 50Ω
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

Symbol	Output pin	S 1	S 2
t _{PHL(W-PE)}	Ports A,B,C	Open	Open
t _{PLH(W-PE)}	Ports E,F	Closed	Open
t _{PZH(R-DQ)}	Data bus	Open	Closed
t _{PHZ(R-DQ)}	Data bus	Open	Closed
t _{PZL(R-DQ)}	Data bus	Closed	Open
t _{PLZ(R-DQ)}	Data bus	Closed	Open



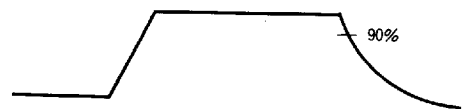
V_{IH} = 2V, V_{IL} = 0.8V
Input pulse levels and input reference levels



V_{OH} = 2V, V_{OL} = 0.8V (Data bus, ports A, B, C)

V_{OH} = V_{OL} = 1.5V (Ports E, F)

t_{PHL(W-PE)} t_{PZH(R-DQ)}
t_{PLH(W-PE)} t_{PZL(R-DQ)}



Output reference levels

t_{PHZ(R-DQ)}

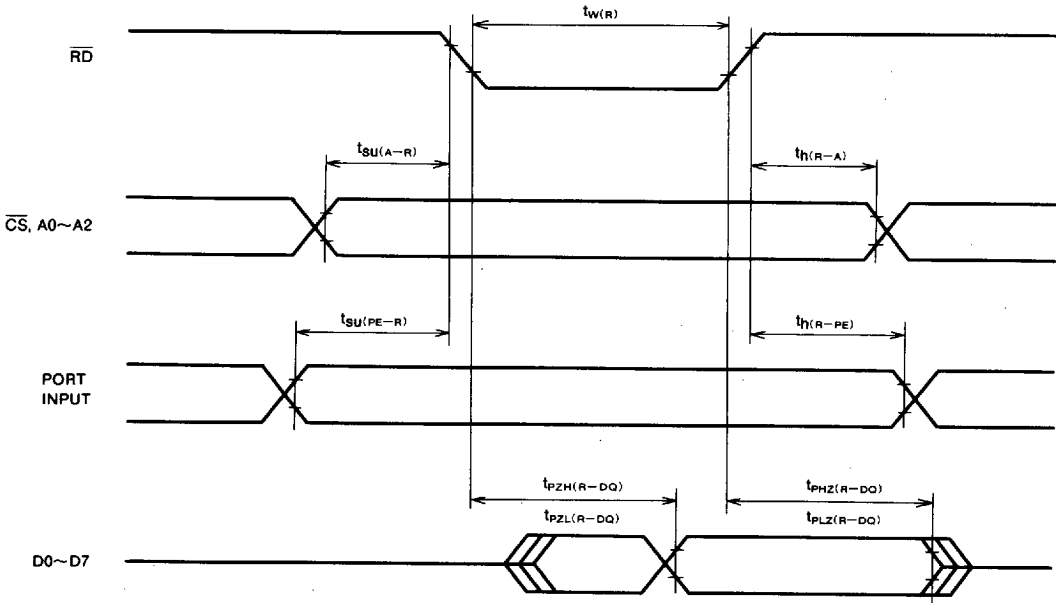
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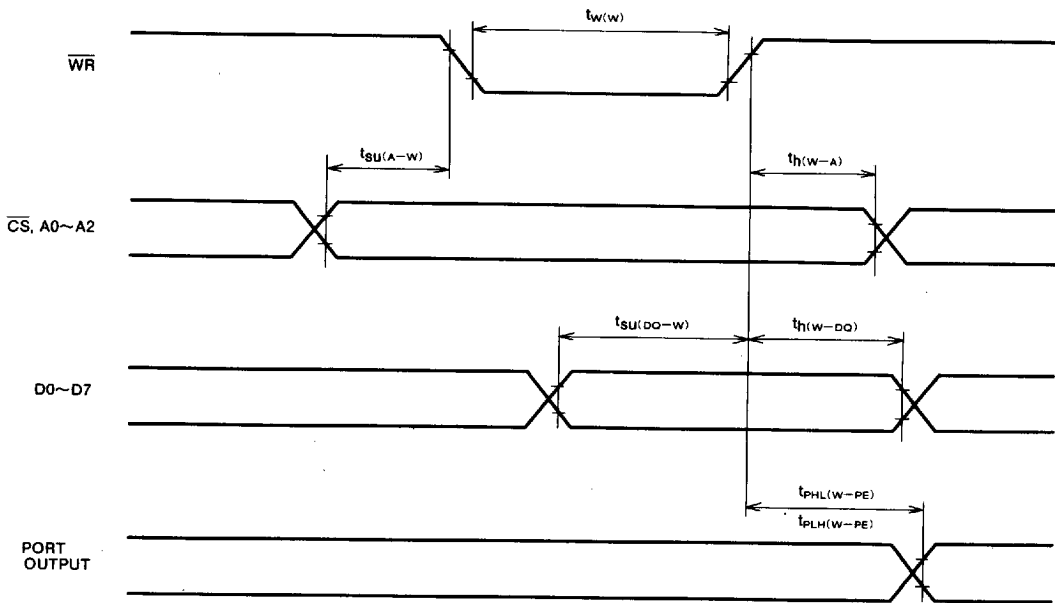
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TIMING DIAGRAM

Read operation timing



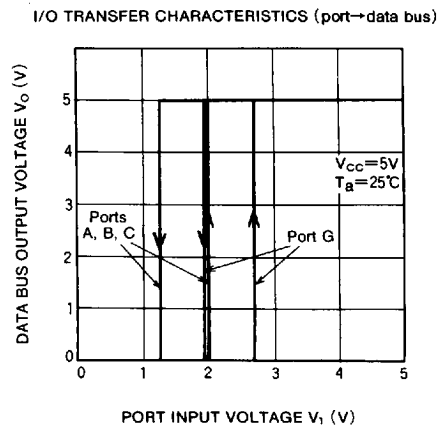
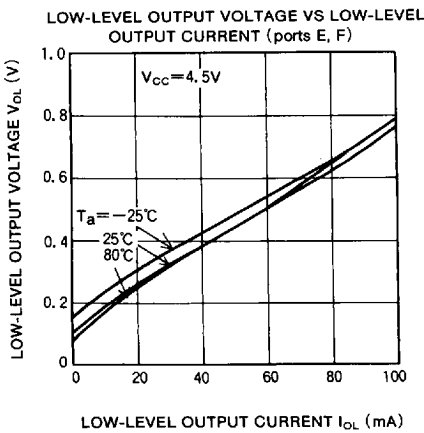
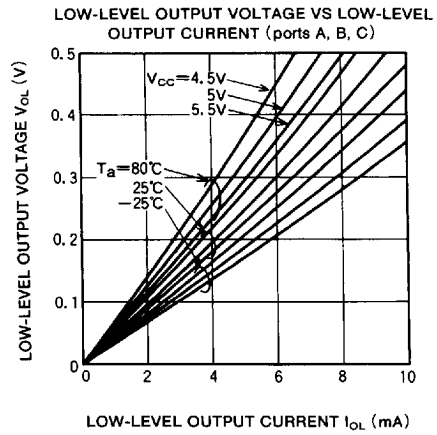
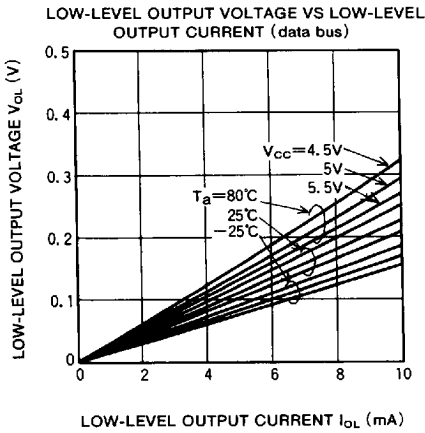
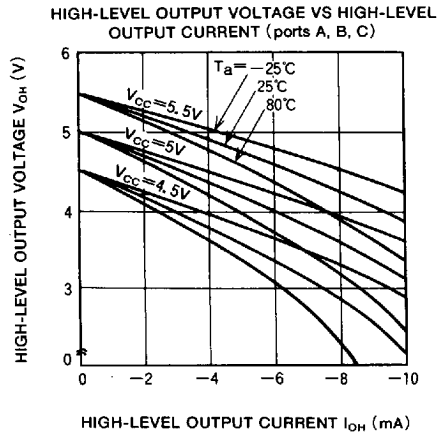
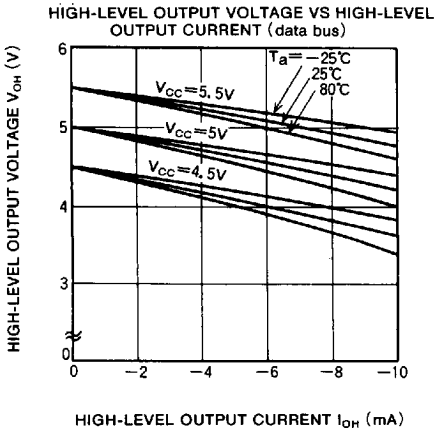
Write operation timing (includes control register write)



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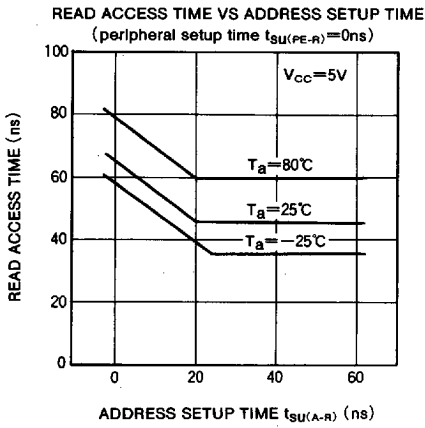
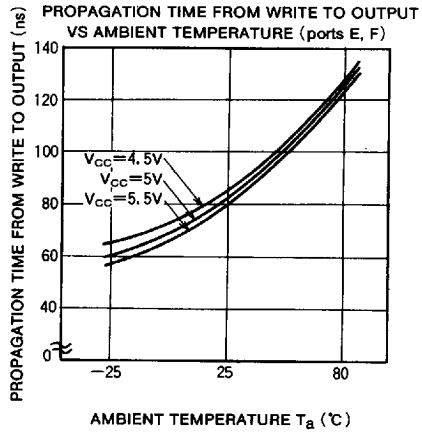
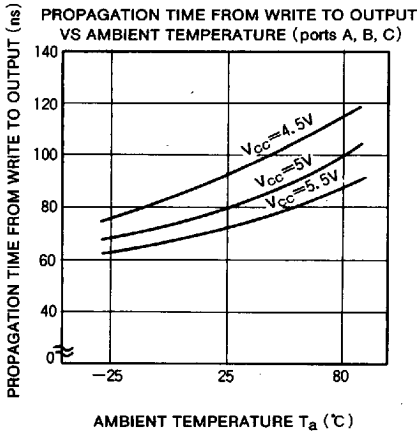
TYPICAL CHARACTERISTICS



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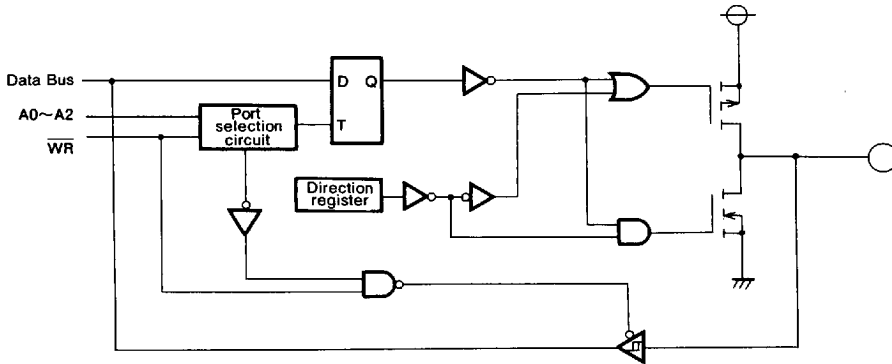


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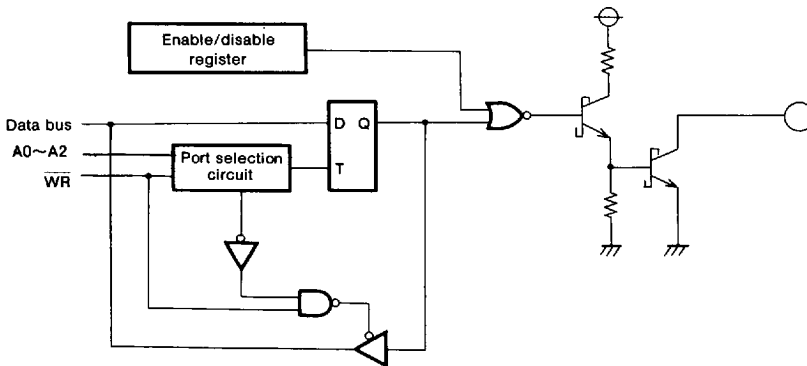
PORT BLOCK DIAGRAM

(Ports A, B, C*)

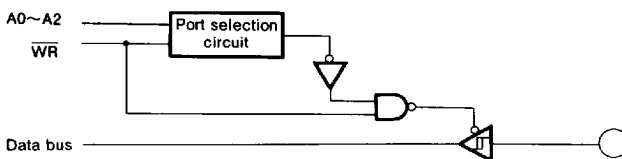


* : The bit set/reset circuit is added to port C.

(Ports E, F)



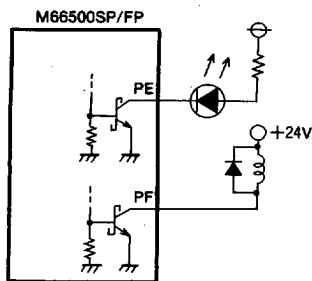
(Port G)



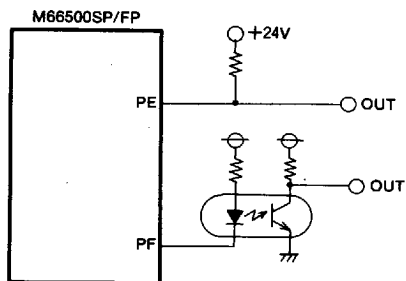
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PROGRAMMABLE BUFFERED I/O EXPANDER

APPLICATION EXAMPLE



1. LED, relay drive



2. Level shift, photo-coupler drive

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