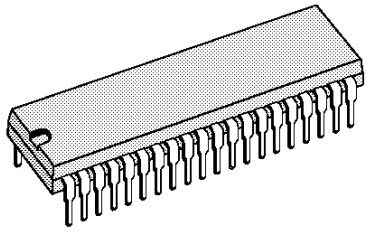
SGS-THOMSON MICROELECTRONICS

STV5342

TELETEXT DECODER WITH 4 INTEGRATED PAGES

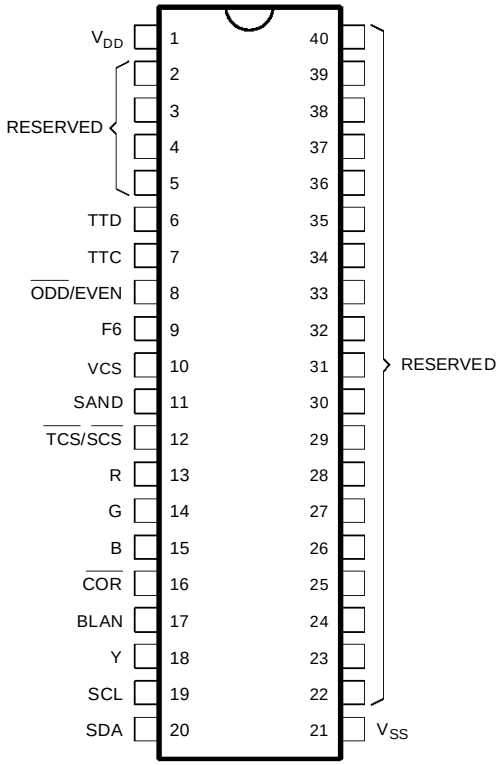
- COMPLETE TELETEXT DECODER INCLUDING ON-CHIP 4 PAGES MEMORY, REDUCING EMC RADIATIONS
- UPWARD SOFTWARE AND HARDWARE COMPATIBLE WITH PREVIOUS SGS-THOMSON's DECODER SDA5243
- AUTOMATIC SELECTION OF UP TO SIX NATIONAL LANGUAGES
- 4 SIMULTANEOUS PAGE REQUESTS
- DISPLAY OF THE 25TH STATUS ROW
- MICROPROCESSOR CONTROL VIA AN I^2C BUS (SLAVE ADDRESS 0010001 R/W)
- DATA ACQUISITION AVAILABLE FROM LINES 2 TO 22 OR FROM A COMPLETE FIELD
- HIGH QUALITY DISPLAY USING A CHARACTER MATRIX OF 12 x 10 DOTS
- SINGLE + 5V SUPPLY VOLTAGE
- ON-CHIP MASK PROGRAMMABLE ROM CHARACTER GENERATORS
- HCMOS PROCESS



DIP40
(Plastic Package)

ORDER CODE : STV5342

PIN CONNECTIONS



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DESCRIPTION

The STV5342 is a HCMOS integrated circuit which performs all the processing of logical data within a 625 lines system teletext decoder. It is designed to operate in conjunction with one-chip : the SAA5231 integrated chip which extracts Teletext information embedded in a composite video signal. Up to 4 pages of display data can be stored in internal memory. A complete system also comprises a microprocessor controlling the STV5342 via a 2-wires serial bus. An on-chip ROM memory contains the character sets. The STV5342 performs automatic selection of one of up to six natural languages. Data bytes may be decoded in either 7-Bit plus parity or in full 8-Bit formats. The chip set also supports facilities for reception and display of higher-level protocol data.

PIN DESCRIPTION

Pin	Symbol	Function	Description
1	V_{DD}	+5V	Positive supply voltage
2 to 5 22 to 40	RESERVED		Not used
6	TTD	Teletext data input	An A.C. coupled teletext data input supplied by the SAA5231 chip is latched to V_{SS} between 4 and 8µs after each TV line.
7	TTC	Teletext clock input	A 6.9375MHz clock signal, supplied by the SAA5231 chip, is internally A.C. coupled, clamped and buffered.
8	$\overline{ODD}$/EVEN	Interlaced mode state output	High for even numbered and low for odd numbered frames. The value is valid 2µs before the end of lines 311 and 624.
9	F6	Character display clock signal	The 6MHz clock signal, supplied by the SAA5231 chip is internally A.C. coupled, clamped and buffered.
10	VCS	Video composite synchronization input signal	Active high VCS input.
11	SAND	Sandcastle	Three level output pulse to the SAA5231 device. Phase lock, blanking signal, and color burst components are contained in this signal.
12	$\overline{TCS}$/$\overline{SCS}$	Input / output composite synchronization signal	Scan composite input signal ($\overline{SCS}$) for the display synchronization or Text composite sync. ($\overline{TCS}$) output signal to the SAA5231. Both signals are active low.
13,14,15	R G B	Red, green, blue	Character and background colors active-high open-drain outputs.
16	$\overline{COR}$	Contrast reduction	Open-drain active-low output supporting optimal display of characters in "mixed mode" operation.
17	BLAN	Blanking signal output	Open-drain active high output for TV-image blanking in normal and mixed-mode operation.
18	Y	Foreground output	Open-drain active-high output with foreground information. Can be used for printer command.
19	SCL	Serial clock	Microprocessor clock input via serial bus.
20	SDA	Serial data input / output	Open-drain microprocessor serial data input/output via serial bus.
21	V_{SS}	0 Volt	Ground

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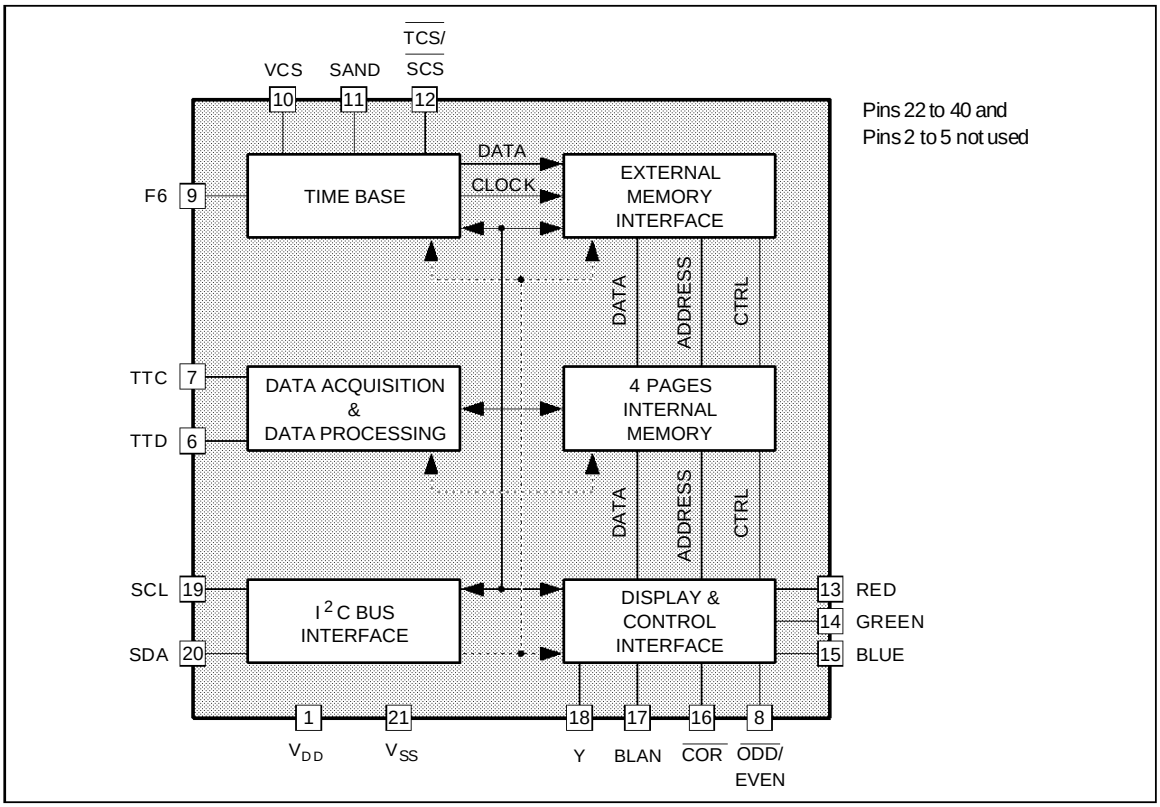
BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Power Supply Range	-0.3, +6.0	V

INPUT VOLTAGE RANGE :

V_I	VCS,SDA,SCL,D0-D7	-0.3, V_{DD} + 0.5	V
V_I	TTD,F6,$\overline{TCS}$/$\overline{SCS}$,TTC	-0.3, +10	V

OUTPUT VOLTAGE RANGE :

V_O	SAND,SDA,$\overline{ODD}$/EVEN,R,G,B	-0.3 , V_{DD}	V
V_O	BLAN,$\overline{COR}$, Y, $\overline{TCS}$/$\overline{SCS}$	-0.3 , V_{DD}	V
T_{stg}	Storage Temperature Range	-20, +125	^oC
T_A	Operating Ambient Temperature Range	-20, +70	^oC

5342-02.TBL

ELECTRICAL CHARACTERISTICS

V_{DD} = 5V, V_{SS} = 0V, T_A = - 20 to + 70^oC

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply Voltage (Pin 1)	4.5	5	5.5	V
I_{DD}	Supply Current (operating mode)		15	40	mA

5342-03.TBL

ELECTRICAL CHARACTERISTICS (continued)
V_{DD} = 5V, V_{SS} = 0V, T_A = - 20 to + 70°C

Symbol	Parameter	Min	Typ	Max	Unit
INPUTS					
	TTD (Pin 6)				
C_{EXT}	Ext. Coupling Capacitor			50	nF
$V_{I(p-p)}$	Input Voltage p-p	2		7	V
t_r , t_f	Input Rise / Fall Times	10		80	ns
t_{DS}	Input Set-up Time	40			ns
t_{DH}	Input Hold Time	40			ns
$I_{I(L)}$	Input Leakage Current (V_I = 0 to V_{DD})	-10		+10	µA
C_I	Input capacitance			7	pF
	TTC, F6 (Pins 7,9)				
V_I	DC Input Voltage	- 0.3		+10	V
$V_{I(p-p)}$	AC Input Voltage F6 AC Input Voltage TTC	1 1.5		7 7	V V
$\pm V_P$	Input Peak Rel. 50 % Duty	0.2		3.5	V
f_{TTC}	TTC Clock Frequency		6.9375		MHz
f_{F6}	F6 Clock Frequency		6		MHz
t_r , t_f	Clock Rise / Fall Times	10		80	ns
$I_{I(L)}$	Input Leakage Current (V_I = 0 to 10V)	-10		+10	µA
C_I	Input Capacitance			10	pF
	VCS (Pin 10)				
V_{IL}	Low Level Input Voltage	0		0.8	V
V_{IH}	High Level Input Voltage	2		V_{DD}	V
t_r , t_f	Input Rise / Fall Times			500	ns
$I_{I(L)}$	Input Leakage Current (V_I = 0 to V_{DD})	-10		+10	µA
C_I	Input Capacitance			7	pF
	SCL (Pin 19)				
V_{IL}	Low Level Input Voltage	0		1.5	V
V_{IH}	High Level Input Voltage	3		V_{DD}	V
f_{SCL}	SCL Clock Frequency			100	kHz
t_r , t_f	Input Rise / Fall Times			2	µs
$I_{I(L)}$	Input Leakage Current (V_I = 0 to V_{DD})	-10		+10	µA
C_I	Input Capacitance			7	pF
INPUT/OUTPUTS					
	$\overline{TCS}$(output), $\overline{SCS}$(input) (Pin12)				
V_{IL}	Low Level Input Voltage	0		1.5	V
V_{IH}	High Level Input Voltage	3		8	V
t_r , t_f	Input Rise / Fall Times			500	ns
$I_{I(L)}$	Input Leakage Current (V_I = 0 to V_{DD} and output in high impedance state)	-10		+10	µA
C_I	Input Capacitance			7	pF
V_{OL}	Low Level Output Voltage (I_{OL} = 0.4mA)	0		0.4	V
V_{OH}	High Level Output Voltage (-I_{OH} = 0.2mA)	2.4		V_{DD}	V
t_r , t_f	Output Rise / Fall Times between 0.6V and 2.2V			100	ns
C_L	Load Capacitance			50	pF

5342-04.TBL

ELECTRICAL CHARACTERISTICS (continued)
V_{DD} = 5V, V_{SS} = 0V, T_A = - 20 to + 70°C

Symbol	Parameter	Min	Typ	Max	Unit
INPUT/OUTPUTS (continued)					
	SDA (Pin 20)				
V_{IL}	Low Level Input Voltage	0		1.5	V
V_{IH}	High Level Input Voltage	3		V_{DD}	V
t_r , t_f	Input Rise / Fall Times			2	µs
$I_{I(L)}$	Input Leakage Current (V_I = 0 to V_{DD} and output in high impedance state)	-10		+10	µA
C_I	Input Capacitance			7	pF
V_{OL}	Low Level Output Voltage (I_{OL} = 3mA)	0		0.5	V
t_f	Output Fall Time between 3.0V and 1.0V			200	ns
C_L	Load Capacitance			400	pF
	D0-D7 (Pins 22-29)				
V_{IL}	Low Level Input Voltage	0		0.8	V
V_{IH}	High Level Input Voltage	2		V_{DD}	V
$I_{I(L)}$	Input Leakage Current (V_I = 0 to V_{DD} and output in high impedance state)	-10		+10	µA
C_I	Input Capacitance			7	pF
V_{OL}	Low Level Output Voltage (I_{OL} = 1.6mA)	0		0.4	V
V_{OH}	High Level Output Voltage ($-I_{OH}$ = 0.2mA)	2.4		V_{DD}	V
t_r , t_f	Output Rise / Fall Times between 0.6V and 2.2V			50	ns
C_L	Load Capacitance			120	pF
OUTPUTS					
	$\overline{ODD}$/EVEN ••(Pin 8)				
V_{OL}	Low Level Output Voltage (I_{OL} = 0.4mA)	0		0.4	V
V_{OH}	High Level Output Voltage ($-I_{OH}$ = 0.2mA)	2.4		V_{DD}	V
t_r , t_f	Output Rise / Fall Times between 0.6V and 2.2V			100	ns
C_L	Load Capacitance			50	pF
	SAND (Pin 11)				
V_{OL}	Low Level Output Voltage (I_{OL} = 0.2mA)	0	-	0.25	V
V_{OI}	Middle Level Output Voltage (I_{OL} = ± 10 µA)	1.1	-	2.9	V
V_{OH}	High Level Output Voltage ($-I_{OH}$ = 0 to 10µA)	4		V_{DD}	V
t_{r1} t_{r2}	Output Rise Time : ● V_{OL} to V_{OI} from 0.4 to 1.1V ● V_{OI} to V_{OH} from 2.9 to 4.0V	- -	- -	400 200	ns
t_f	Output Fall Time V_{OH} to V_{OI} from 4.0 to 0.4V	-	-	50	ns
C_L	Load Capacitance	-	-	30	pF
	R, G, B, $\overline{COR}$, BLAN, Y (Pins 13-18)				
V_{OL}	Low Level Output Voltage : ● I_{OL} = 2mA ● I_{OL} = 5mA	 0 0	 - -	 0.4 1	V
V_{PU}	Pull-up Voltage (with R = 1kΩ to V_{DD})	-	-	V_{DD}	V
t_f	Output Fall Time from 4.5 to 1.5V (with R = 1kΩ to V_{DD})	-	-	20	ns
t_{SK}	Skew Delay on Falling Edges (at 3V with R = 1kΩ connected to V_{DD})	-	-	20	ns
C_L	Load Capacitance	-	-	25	pF
I_{LO}	Output Leakage Current (V_{PU} = 0 to V_{DD} output off)	-	-	20	µA

5342-05.TBL

ELECTRICAL CHARACTERISTICS (continued)

V_{DD} = 5V, V_{SS} = 0V, T_A = - 20 to + 70°C

Symbol	Parameter	Min	Typ	Max	Unit
TIMING					
	SERIAL BUS (referred to V_{IH} = 3V, V_{IL} = 1.5V) (see Fig. 6)				
t_{LOW}	Low Period Clock	4	-	-	µs
t_{HIGH}	High Period Clock	4	-	-	µs
$t_{SU,DAT}$	Data Set-up Time	250	-	-	ns
$t_{HD,DAT}$	Data Hold Time	170	-	-	ns
$t_{SU,STO}$	Stop Set-up Time from Clock High	4	-	-	µs
t_{BUF}	Start Set-up Time Following a Stop	4	-	-	µs
$t_{HD,STA}$	Start Hold Time	4	-	-	µs
$t_{SU,STA}$	Start Set-up Time Following Clock Low to High Transition	4	-	-	µs

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Figure 1 : F6, TTC, TTD Input Internal Connections

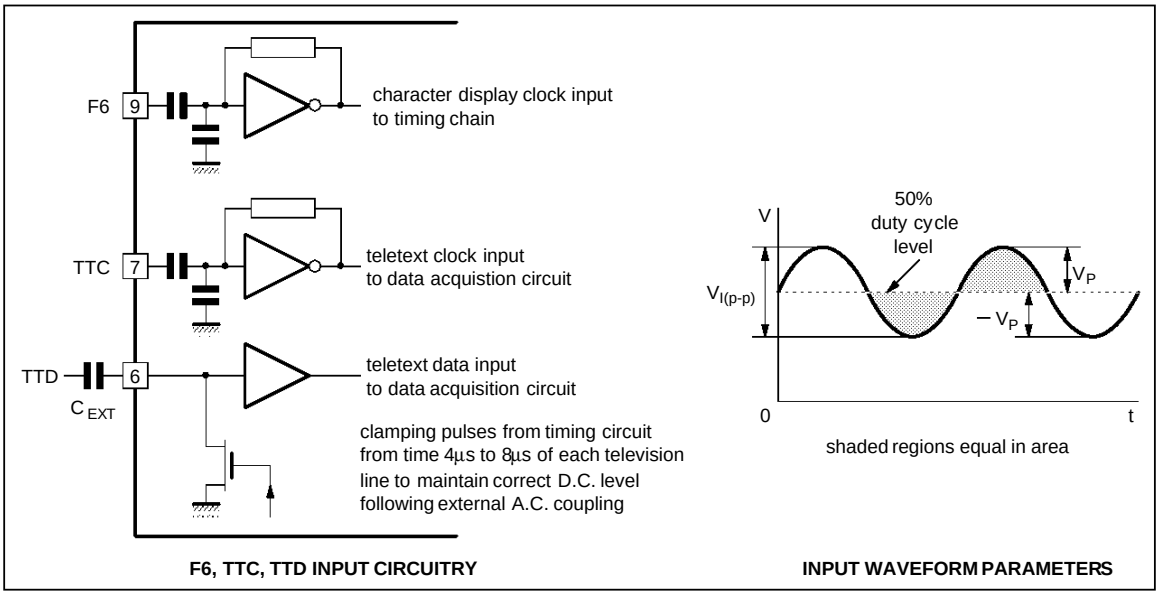

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Figure 2 : Teletext Data Input Timing

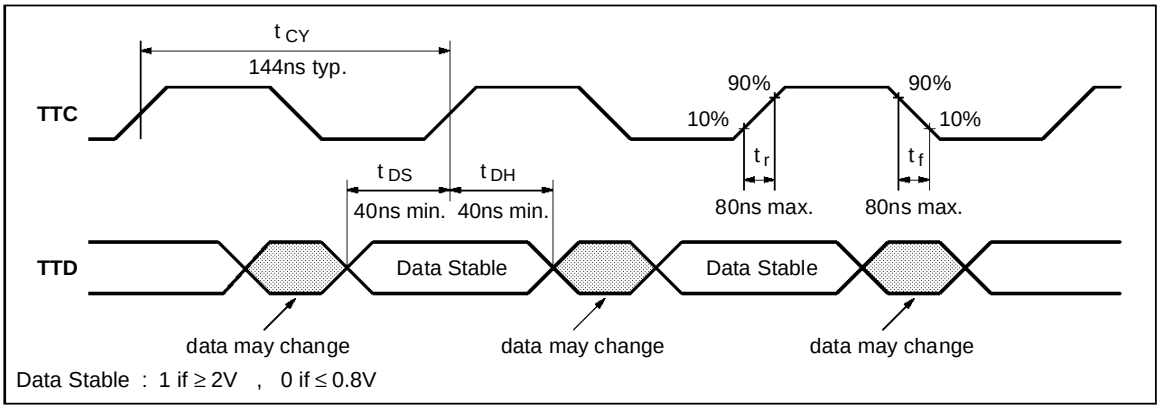

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Figure 3 : Synchronization Timing

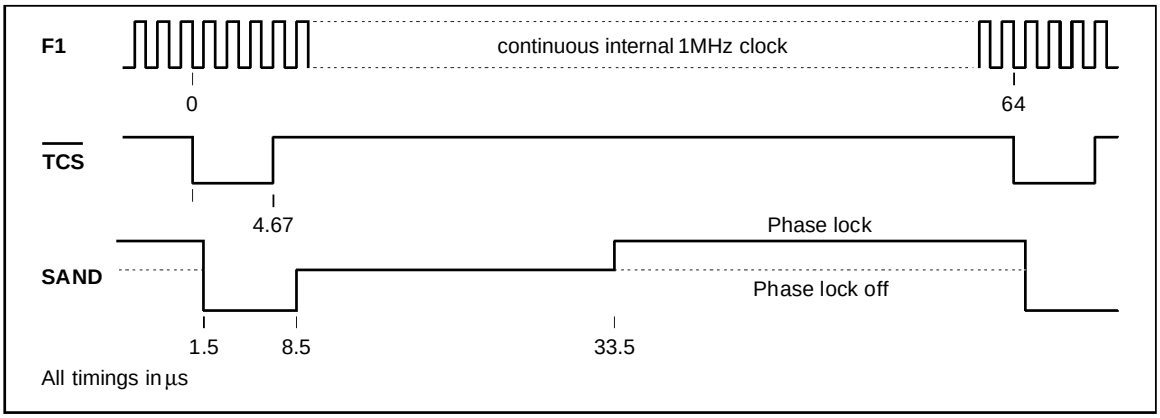
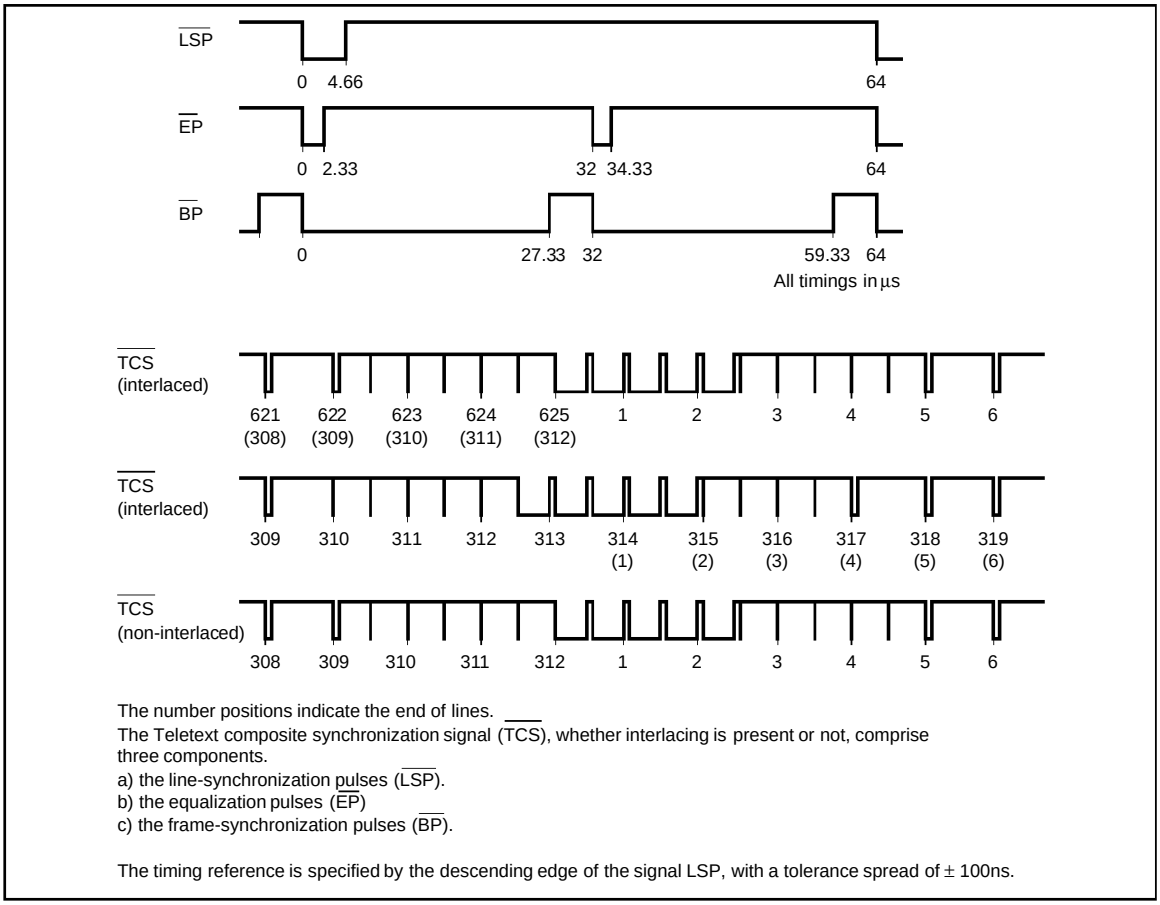


Figure 4 : Composite Sync. Waveforms



The number positions indicate the end of lines.
The Teletext composite synchronization signal (TCS), whether interlacing is present or not, comprise three components.
a) the line-synchronization pulses (LSP).
b) the equalization pulses (EP)
c) the frame-synchronization pulses (BP).

The timing reference is specified by the descending edge of the signal LSP, with a tolerance spread of ± 100ns.

Figure 5 : Display Output Timing

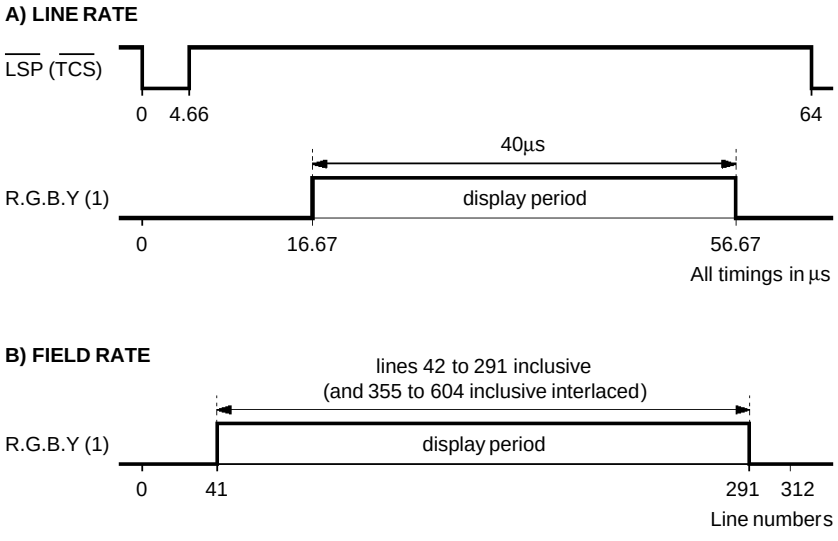


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Figure 6 : Serial Bus Timing

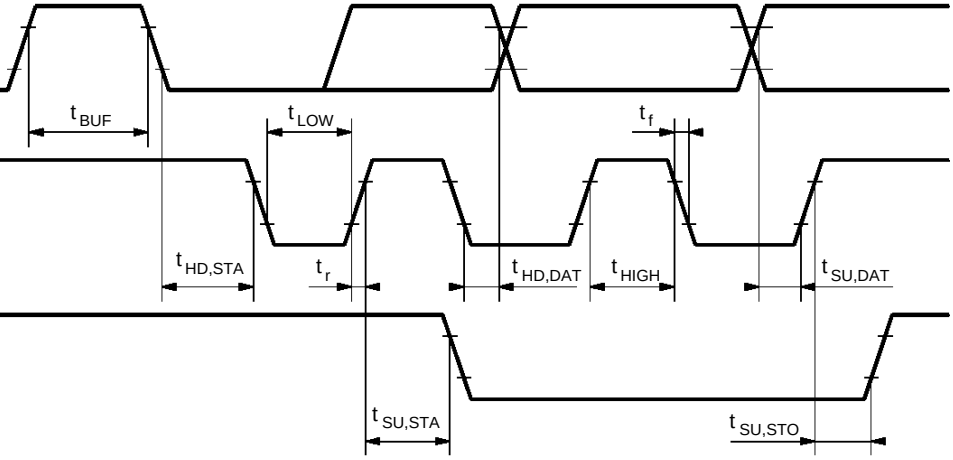

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Figure 7 : Master Synchronization Mode

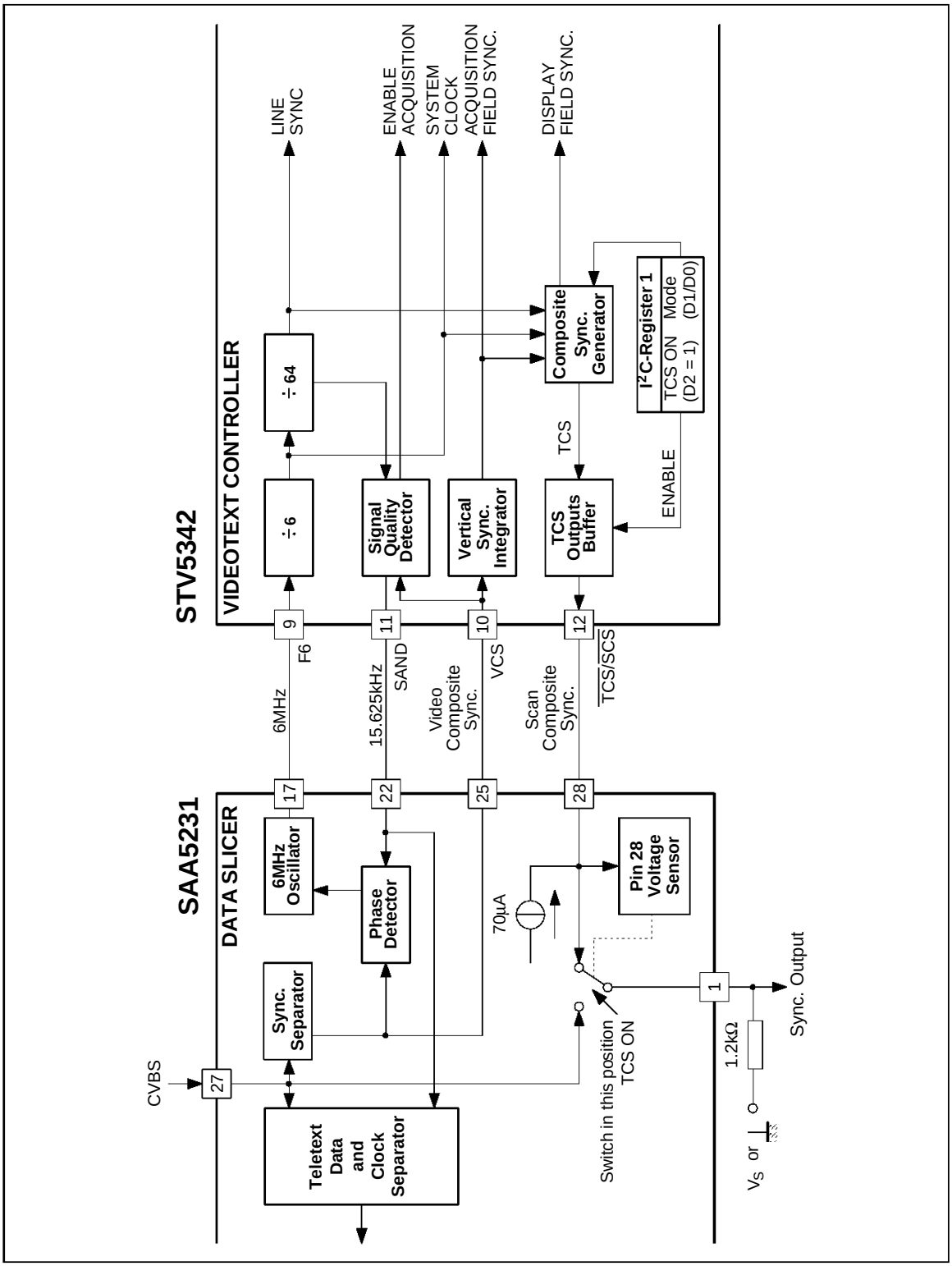

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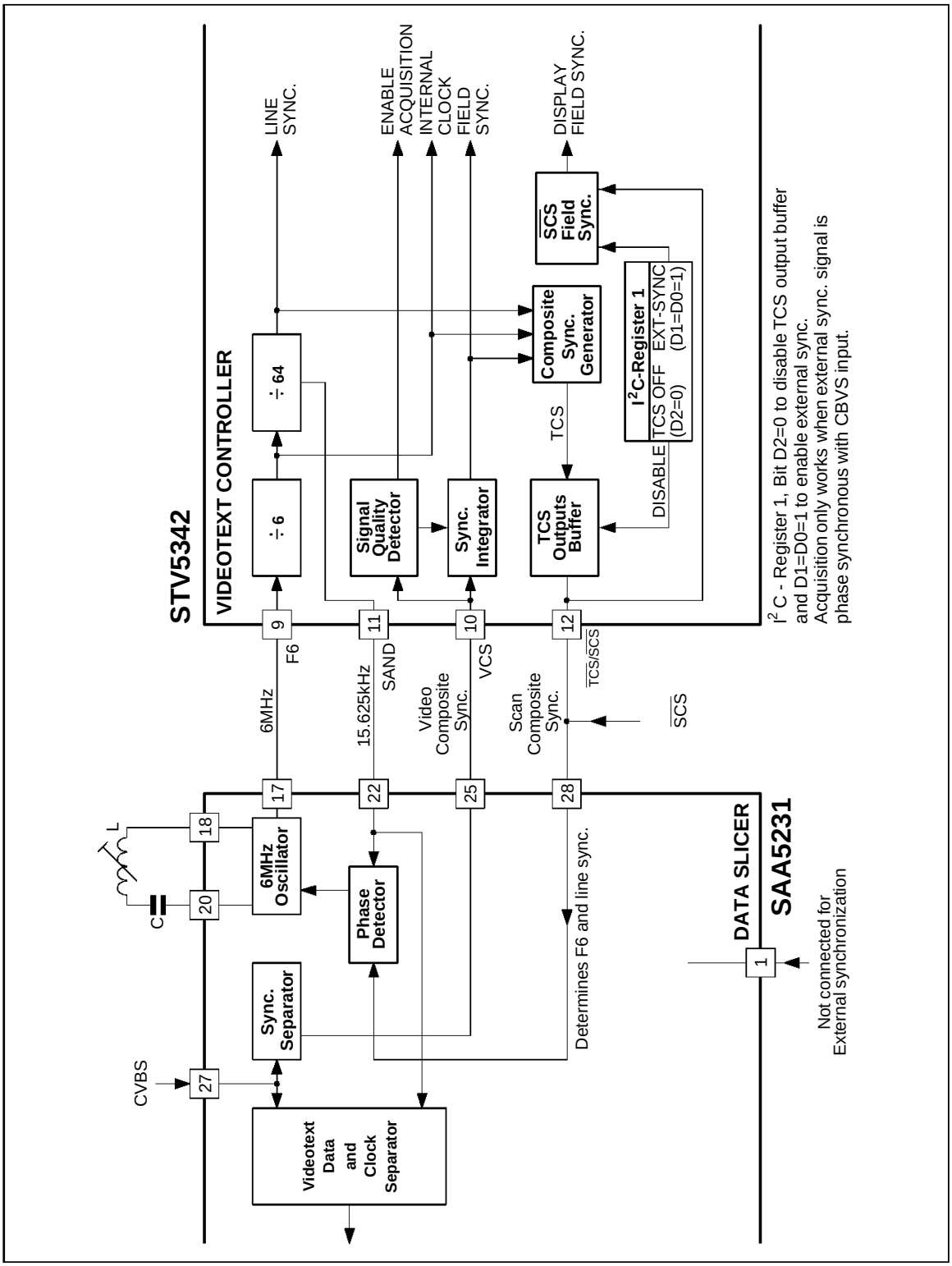
Figure 8 : Slave Synchronization Mode



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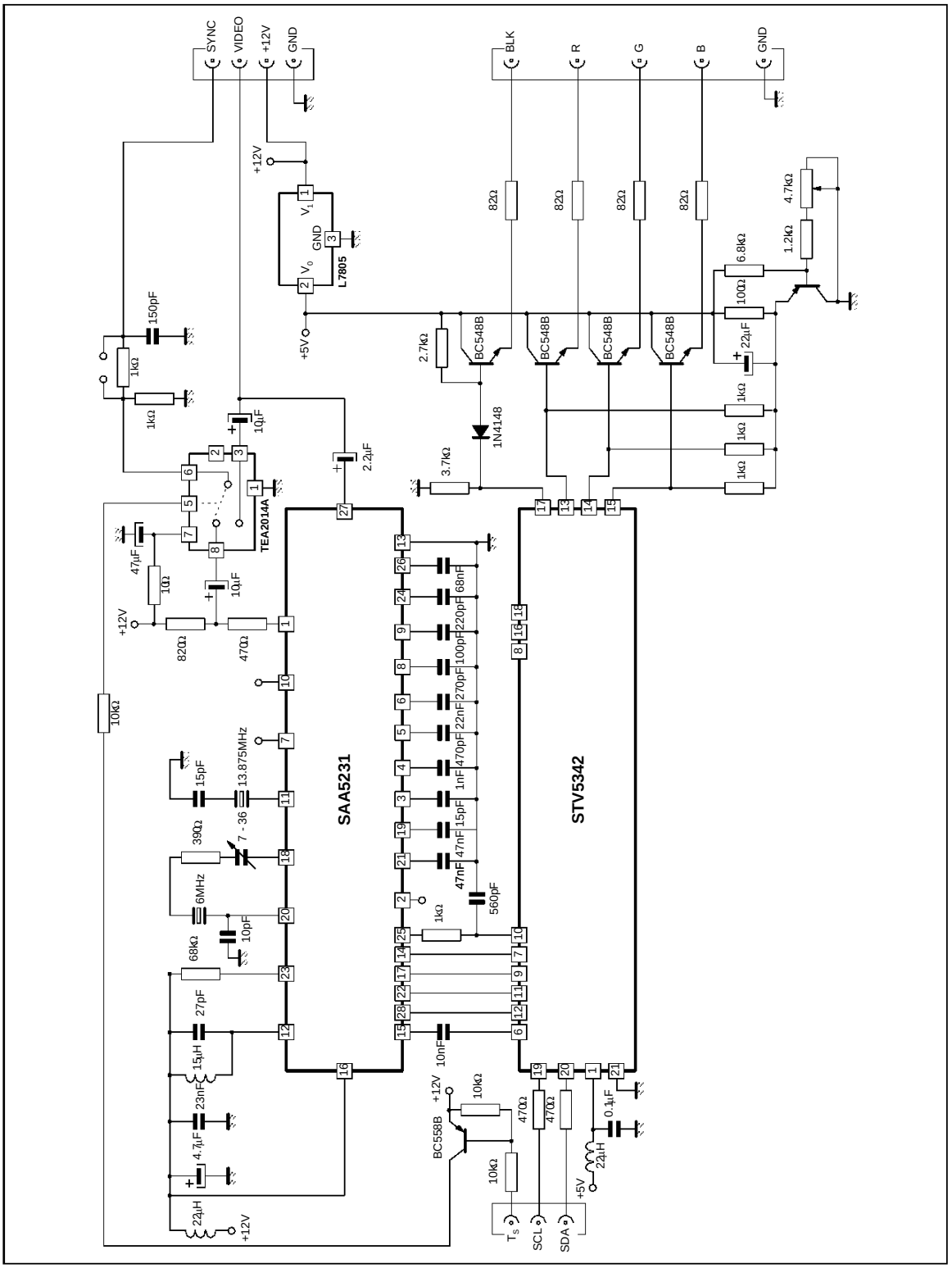
APPLICATION DIAGRAM



APPLICATION NOTES

ORGANIZATION OF A PAGE-MEMORY

The organization of a page-memory is shown in Figure 9. The STV5342 chip provides a display format of 25 rows of 40 characters per row.

Row number twenty-four is used by the microprocessor for the display of information.

Row zero contains the page header.

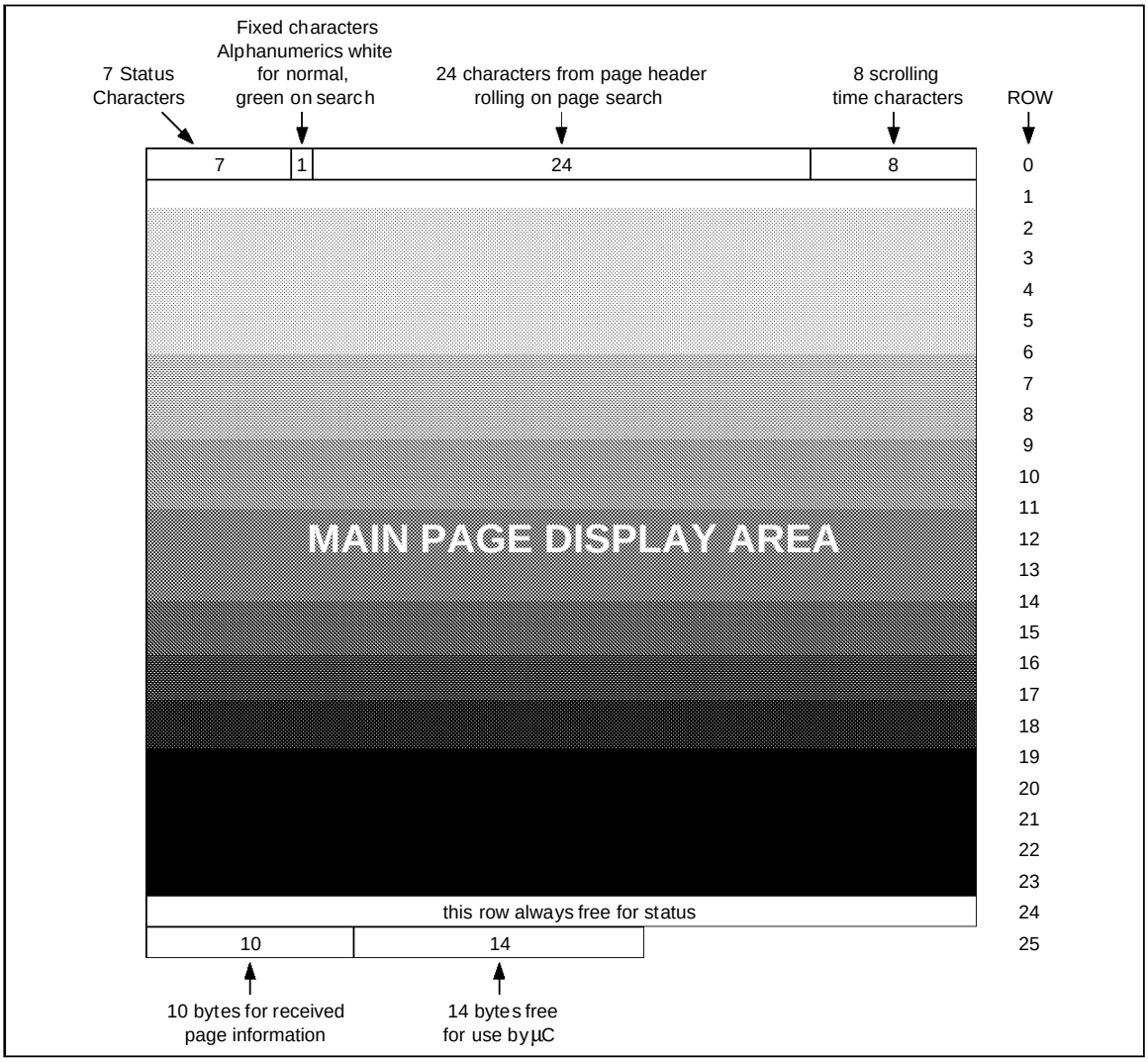
The organization is as follows :

The first seven characters (0 - 6) are used for messages regarding the operational status.

The eighth character is an alphanumeric control character either ”white” or ”green” defining the ”search” status of the page. When it is ”white” the operational state is normal and the header appears white ; when it is ”green” the operational state corresponds to ”search mode” and the header appears green. The following twenty-four characters give the header of the requested page when the system is in search mode. The last eight characters display the time of day.

Row twenty-five comprises ten bytes of control data concerning the received page (see Table 1) and fourteen free bytes which can be used by the microprocessor.

PAGE MEMORY ORGANIZATION
Figure 9



8/30 READING
8/30 packet is read at row 23 equivalent address.
R8 register must be programmed with D3, D2, D0 = 0 and D2 = 1 (8/30 selection).
R9 register must be programmed with 23 (17h).
R10 register value corresponds to the position of the byte to be read (from 0 to 39).
R11A contents the value of the needed byte.

Table 1 : Row 25 received page control data format

D0	PU0	PT0	MU0	MT0	HU0	HT0	C7	C11	MAG0	0
D1	PU1	PT1	MU1	MT1	HU1	HT1	C8	C12	MAG1	0
D2	PU2	PT2	MU2	MT2	HU2	C5	C9	C13	MAG2	0
D3	PU3	PT3	MU3	C4	HU3	C6	C10	C14	0	0
D4	HAM	HAM	HAM	HAM	HAM	HAM	HAM	HAM	$\overline{\text{FOUND}}$	0
D5	0	0	0	0	0	0	0	0	0	PBLF
D6	0	0	0	0	0	0	0	0	0	0
D7	0	0	0	0	0	0	0	0	0	0
COLUMN	0	1	2	3	4	5	6	7	8	9

Page number : - MAG = magazine, PU = page units, PT = page tens.
Page sub-code : - MU = minutes units, MT = minutes tens, HU = hours units, HT = hours tens.
PBLF = page being looked for, FOUND = low for page found, HAM = hamming error in byte, C4-14 = control bits.

5342-08.TBL

REGISTER MAP (see Table 2)

Registers R0 to R10 are write only whilst R11A is a read/write and R11B is a read only register respect to the microprocessor.
The automatic succession on a byte basis is indicated by the arrows in Table 2.
In the normal operating mode TA, TB and TC should be set to logic level 0.
After power-up the contents of the registers are as follows : all bits in registers R0 to R11A are cleared to zero with the exception of bits D0 and D1 in registers R5 and R6 which are set to logical one.
After power-up all the memory bytes are preset to hexadecimal value 20 H (space) with the exception of the byte corresponding to row 0 of column 7 of chapter 0 which is set to the value corresponding to "alpha white" hexadecimal value 07 H.

Table 2 : Register specification

D7	D6	D5	D4	D3	D2	D1	D0		
*	*	*	*	*	EVEN OFF	TC	SEL11B	R0	Mode 0
TA	$\overline{7+P/8\ BIT}$	$\underline{ACQ.}$ ON/OFF	8/30 ENABLE	$\overline{DEW}$/ FULL FIELD	TCS ON	T1	T0	R1	Mode 1
*	*	ACQ CCT A1	ACQ. CCT A0	TB	START COLUMN SC2	START COLUMN SC1	START COLUMN SC0	R2	Page request adress
*	*	*	PRD4	PRD3	PRD2	PRD1	PRD0	R3	Page request data
*	*	*	*	*	*	A1	A0	R4	Display chapter
BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN	R5	Display control (normal)
BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN	R6	Display control (newsflash / subtitle)
STATUS $\underline{ROW}$ BTM/TOP	CURSOR ON	$\overline{CONCEAL}$/ REVEAL	$\overline{TOP}$/ BOTTOM	$\overline{SINGLE}$/ DOUBLE HEIGHT	BOX ON 24	BOX ON 1-23	BOX ON 0	R7	Display mode
*	*	*	*	CLEAR MEM.	8/30 SELECT	A1	A0	R8	Active chapter
*	*	*	R4	R3	R2	R1	R0	R9	Active row
*	*	C5	C4	C3	C2	C1	C0	R10	Active column
D7 (R/W)	D6 (R/W)	D5 (R/W)	D4 (R/W)	D3 (R/W)	D2 (R/W)	D1 (R/W)	D0 (R/W)	R11A	Active data
60Hz	0	0	0	0	0	0	VCS signal quality	R11B	Status

5342-09.TBL

* Reserved register bits : must be set to 0

REGISTER FUNCTIONS

Register	Function	Bit(s)	Description
R0 Address 00H	R11 adressing and pin functions control	SEL 11B (D0)	Selection of register 11B (D0 = 1) or 11A (D0 = 0)
		TC (D1)	Test bit, must be cleared in the normal working mode
		EVEN OFF (D2)	Control of $\overline{\text{ODD}}$/EVEN pin : EVEN signal output (D2 = 0) or grounded (D2 = 1)
R1 Address 01H	Operating mode controls	T1 T0 0 0 0 1 1 0 1 1	312/313 line MIX - mode with interlace 312/313 line TEXT - mode without interlace 312/312 line Terminal mode without interlace External synchronization TCS/SCS is an input
		TCS ON (D2)	D2 = 1, TCS output on Pin $\overline{\text{TCS}}$/$\overline{\text{SCS}}$ D2 = 0, SCS input on Pin TCS/$\overline{\text{SCS}}$
		$\overline{\text{DEW}}$ / FULLFIELD (D3)	Selection of field flyback mode or full channel mode (D3 = 1)
		8/30 ENABLE (D4)	Selection of 8/30 packet acquisition (D4 = 1)
		ACQUISITION ON / OFF (D5)	Control of acquisition operation (D5 = 0 enables acquisition)
		$\overline{\text{7 bits + parity or 8 bits without parity}}$ (D6)	Selection of received data format either 7 bits with parity (D6 = 0) or 8 bits without parity (D6 = 1).
		TA (D7)	Test bit, must be cleared in the normal working mode
R2 Address 02H	Addressing information for a page request	SC0, SC1, SC2 (D0, D1, D2)	Address the first column of the on chip page request RAM to be written.
		TB (D3)	Test bit, must be cleared in the normal working mode.
		A0 - D4 A1 - D5	Selection of acquisition circuit (1 of 4)
R3 Address 03H	Data relative to the requested page (see Table 3)	PRD0 - PRD4 (D0 - D4)	Written data in the page request RAM, starting with the columns addressed by SC0,SC1,SC2.
R4 Address 04H	Selection of one of 4 pages to display	A0 - D0 A1 - D1	Selection of page to be displayed
R5 Address 05H	Display control for normal operation	PON (D0, D1)	Picture on (IN: D0, OUT: D1)
		TEXT (D2, D3)	Text on (IN: D2, OUT: D3)
		$\overline{\text{COR}}$ (D4, D5)	Contrast reduction on (IN: D4, OUT: D5)
		BKGND (D6, D7)	Background colour on (IN: D6, OUT: D7)
		IN / OUT	Enable inside/outside the box
R6 Address 06H	Display control for news-flash subtitle generation	See R5	See R5
R7 Address 07H	Display mode	BOX ON 0, 1-23,24 (D0, D1, D2)	The "boxing" function is enabled on row 0,1-23 and 24 by D0, D1 and D2 set to one.
		$\overline{\text{TOP}}$/BOTTOM Single/Double Height (D4/D3)	X0 = Normal 01 = double height Rows 0 to 11 11 = double height Rows 12 to 23
		$\overline{\text{Conceal}}$/Reveal (D5)	Conceal Reveal Function
		Cursor ON/$\overline{\text{OFF}}$ (D6)	Cursor position given by row/column value of R9/R10
		STATUS ROW BTM / TOP (D7)	The 25th row is displayed before the "Main text Area" (lines 0-23) or after (D7 = 0).
R8 Address 08H	Active Chapter Address	A0 (D0) A1 (D1)	Selection of chapter to be READ/WRITE
		8/30 SELECT(D2)	To read 8/30 packet R8, D0 and D1 must be "0" and D2 = 1

5342-10.TBL

REGISTER FUNCTIONS

Register	Function	Bit(s)	Description
R9 to R11A Address 09H to 0BH*	Active row address (R9), active column address (R10). Data contained in R11A read (written) from (to) memory by microprocessor via I^2C.		
R11B Address 0BH*	Status	VCS Signal Quality (D0)	Good VCS quality signal detected (D0 = 1) or disturbed (D0 = 0)
		60Hz (D7)	VCS received with 60Hz frequency (D7 = 1) or 50Hz (D7 = 0). Only valid when VCS is good (D0 = 1)

5342-11.TBL

* Reading of R11A or R11B is determined by register 0, bit D0. Nevertheless, write operation is always performed on R11A register.

Table 3 : Register R3

START COLUMN	PRD4	PRD3	PRD2	PRD1	PRD0
0	Do care magazine	$\overline{HOLD}$	MAG2	MAG1	MAG0
1	Do care page tens	PT3	PT2	PT1	PT0
2	Do care page units	PU3	PU2	PU1	PU0
3	Do care hours tens	X	X	HT1	HT0
4	Do care hours units	HU3	HU2	HU1	HU0
5	Do care minutes tens	X	MT2	MT1	MT0
6	Do care minutes units	MU3	MU2	MU1	MU0

5342-12.TBL

The abbreviations have the same significance as in Table 1 with the exception of the "DO CARE" entries. It is only when this bit is "1" that the corresponding digit is taken into consideration on page request. For example, a page defined as "normal" or one defined as "timed" may be selected.
If "$\overline{HOLD}$" is low the page is held. The addressing of successive bytes via the I^2C bus is automatic.

CHARACTER SETS

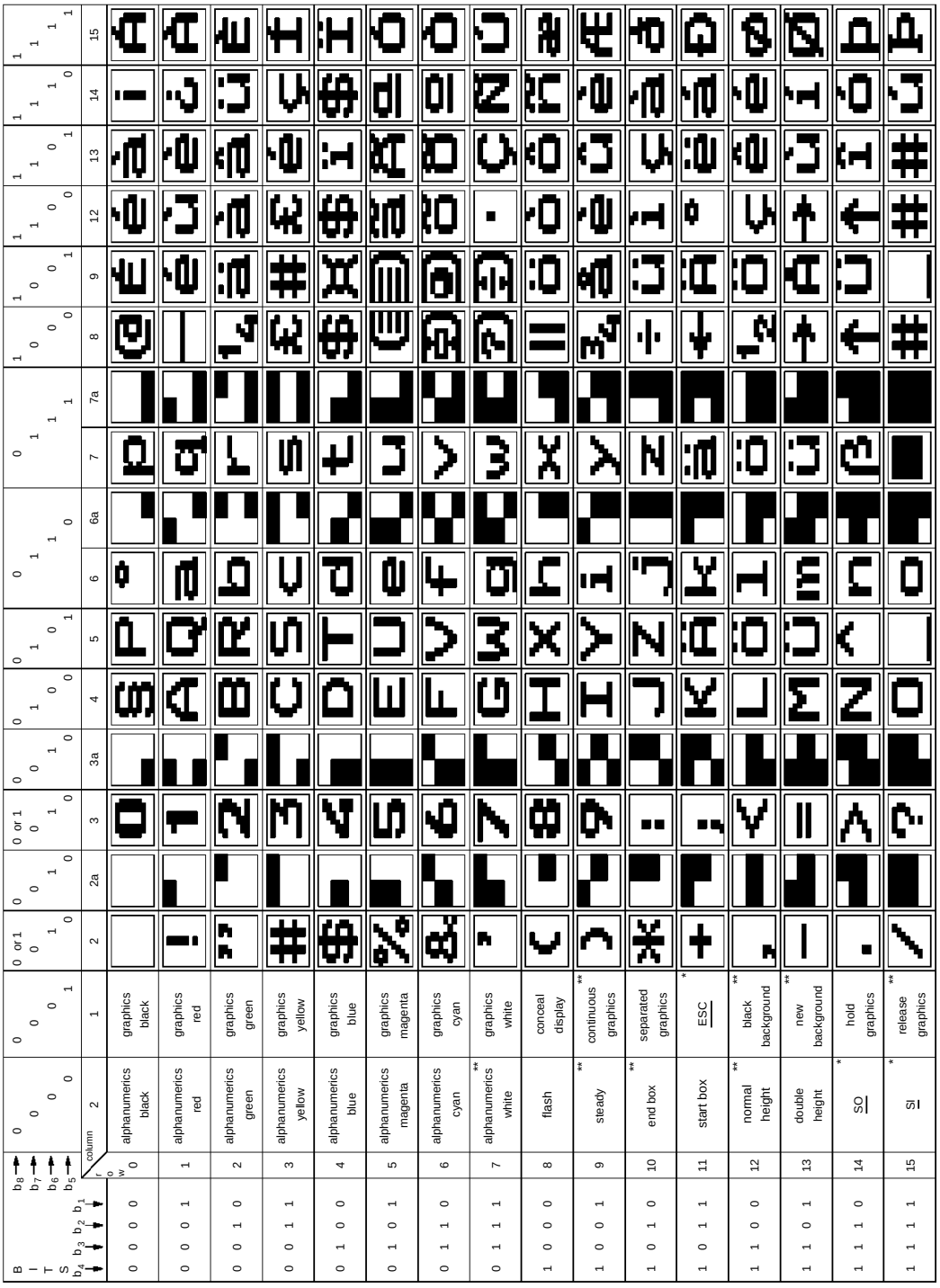
The complete character set with 8-bit decoding is given in Table 4.

Characters in columns 0 and 1 are normally displayed as blanks. Black dots represent the character shape whereas white dots represent the background.
Each character can be identified by a pair of corresponding row and column integers : for example the character "3" may be indicated by 3/3.

A rectangle may be represented as follows : ▭

The characters 8/6, 8/7, 9/5, 9/7 are used as special characters, always in conjunction with 8/5.
The 13 national characters are placed in columns with bit 8 = 0.

Table 4 : Complete character set (with 8 bit codes) - West European Languages



Case using C12 C13 C14 = 001 (German Set)

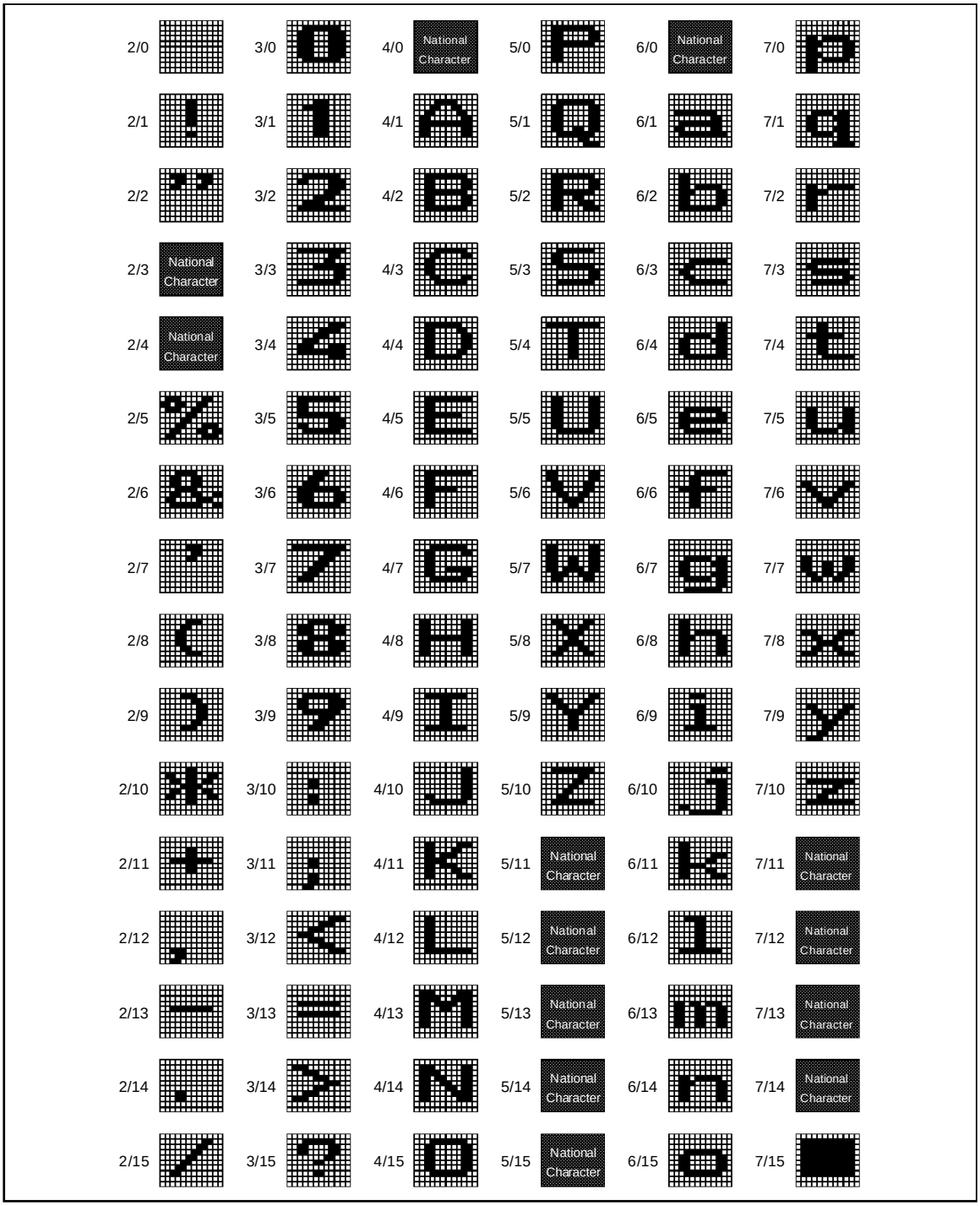
* These control characters are reserved for compatibility with other data codes.
** These control characters are presumed before each row begins

5342-13.EPS

NATIONAL OPTION CHARACTER SETS

The basic set of the 96 characters is shown in Table 5. The location of the 13 national characters are shown in Table 5 whilst full national character sets are depicted in Table 6.

Table 5 : Basic character set.



5342-14.EPS

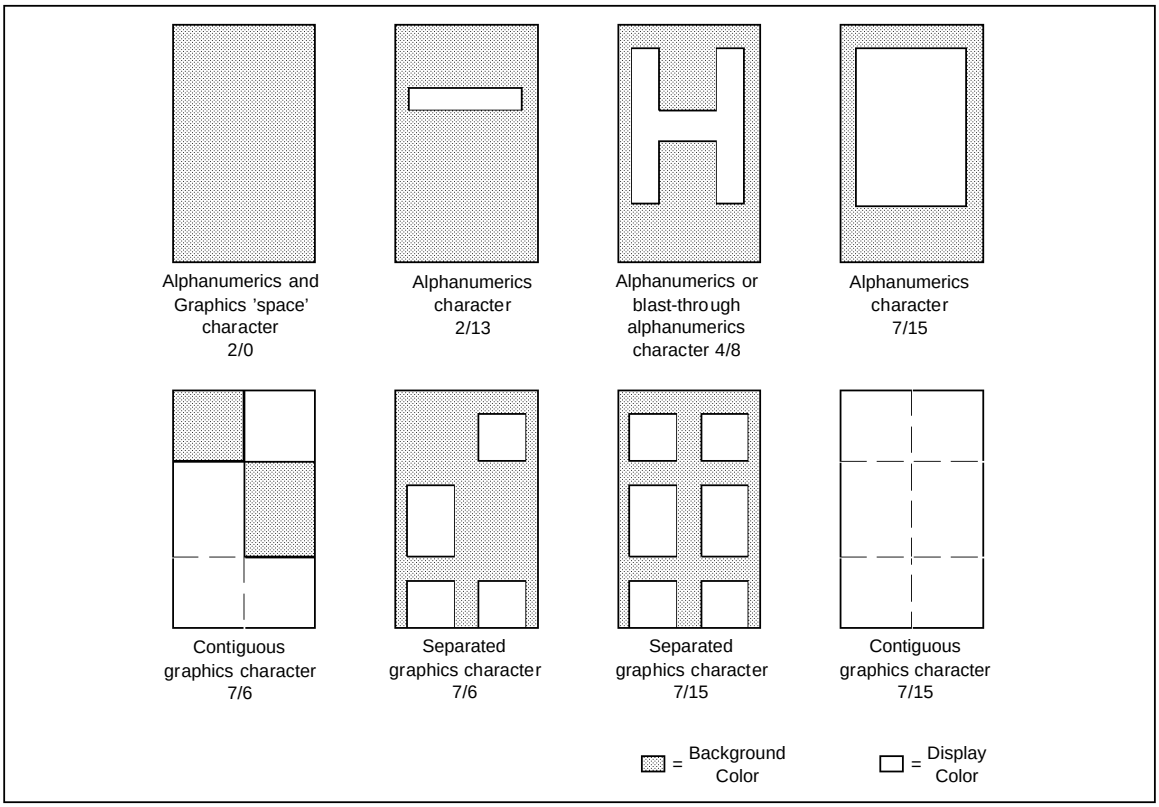
Table 6 : Character Set for STV5342 West European Languages

LANGUAGE	PHCB (1)			CHARACTER POSITION (COLUMN/ROW)												
	C12	C13	C14	2/3	2/4	4/0	5/11	5/12	5/13	5/14	5/15	6/0	7/11	7/12	7/13	7/14
ENGLISH	0	0	0	#	$	@	[	½	]	↑	_	`	¼	‖	¾	÷
GERMAN	0	0	1	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
SWEDISH	0	1	0	#	¤	É	Ä	Ö	Å	Ü	_	é	ä	ö	å	ü
ITALIAN	0	1	1	£	$	§	°	ç	é	^	#	ù	à	ò	è	ì
FRENCH	1	0	0	é	ù	à	°	ç	§	^	#	_	¨	ò	è	ì
SPANISH	1	0	1	¡	$	@	Á	½	¿	^	Ñ	`	¨	ñ	ç	~

5342-15.EPS

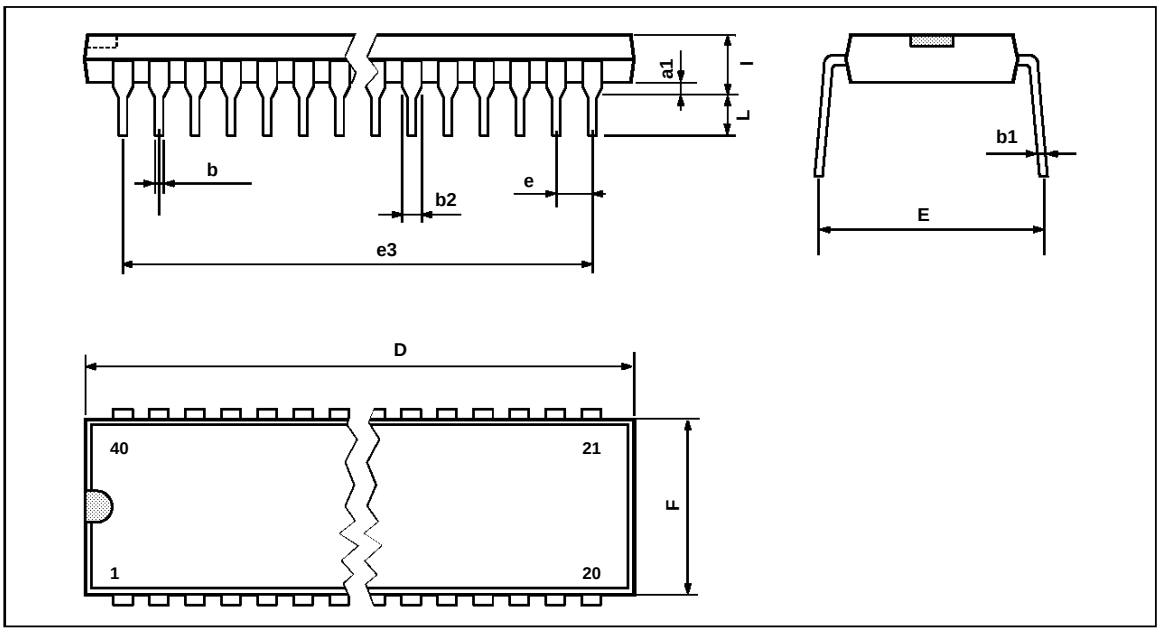
Note 1 : Where PHCB are the Page Header Control bits. Other Combinations default to English. Only the above characters change with the PHCB. All others characters in the basic set are shown in Table 5.

Figure 10 : Character Format



PACKAGE MECHANICAL DATA

40 PINS - PLASTIC DIP



PM-DIP40.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			52.58			2.070
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		48.26			1.900	
F			14.1			0.555
i		4.445			0.175	
L		3.3			0.130	

DIP40.TBL