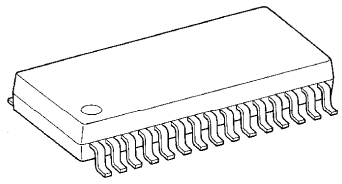
TOSHIBA BIPOLAR LINEAR INTEGRATED CIRCUIT SILICON MONOLITHIC

TA8819F

NTSC VIDEO CHROMA SIGNAL PROCESSOR SYNC PLAYBACK IC FOR LCD TV

TC8819F can be directly driven by battery because it operates on 3.3 to 7.5 V.
Effect of fluctuations in supply voltage are minimized.
Built-in automatic contrast limiter (ACL) utilizes LCD panel dynamic range, delivering clear image reproduction.



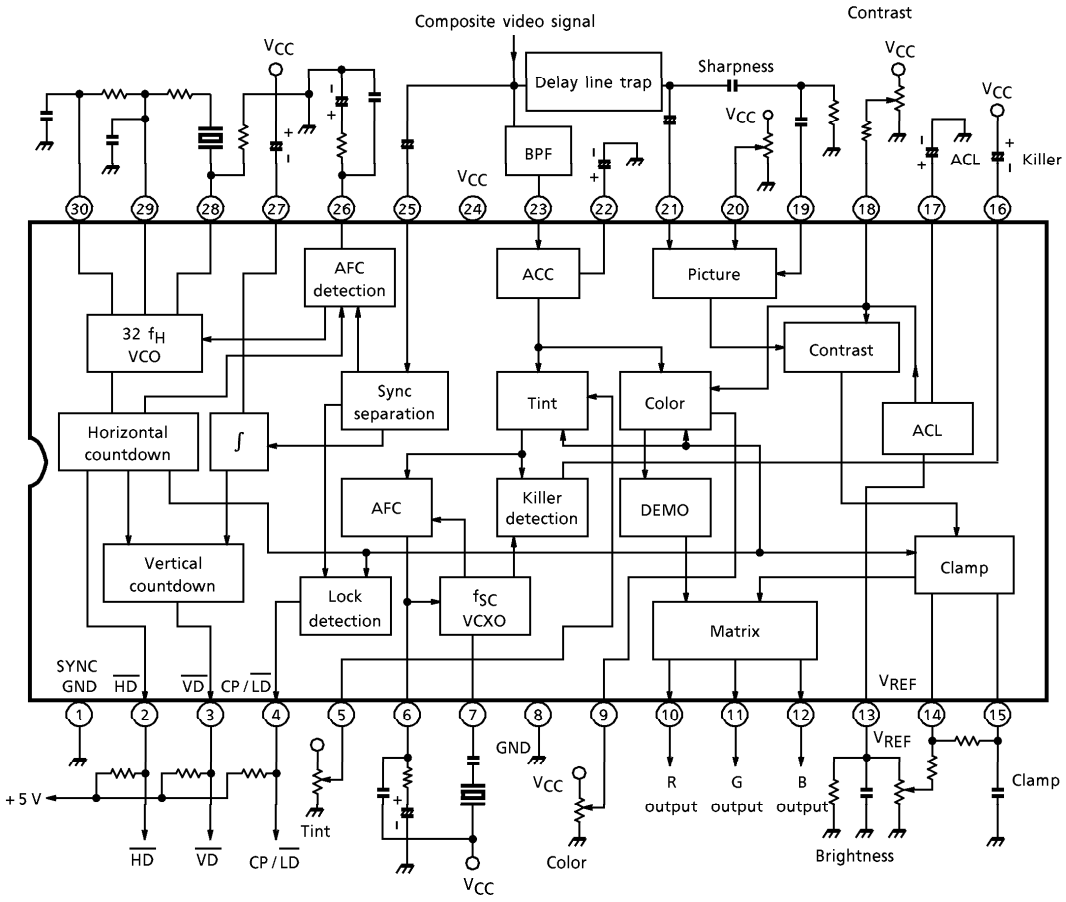
SSOP30-P-375-1.00

Weight : 0.63 g (Typ.)

FEATURES

- Video circuit block
  - Secondary differential sharpness adjustment (DC control)
  - Unicolor contrast control
- Chroma circuit block
  - 2-axis demodulation primary color output
- Sync playback circuit block
  - High-performance sync separation
  - Countdown oscillation frequency adjustment-free
  - Stable vertical sync performance even when synchronization fails

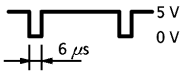
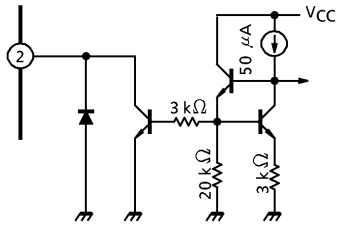
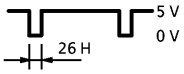
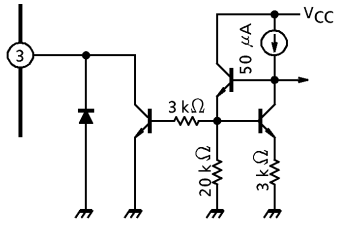
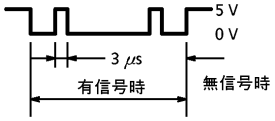
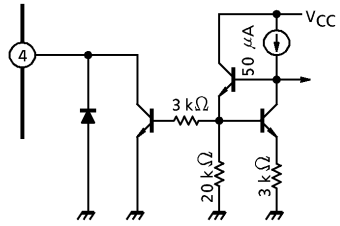
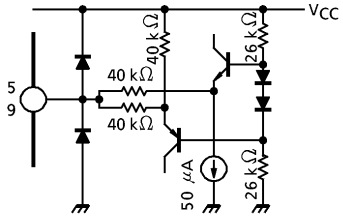
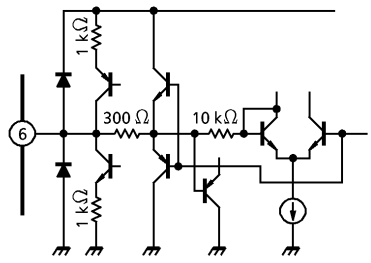
BLOCK DIAGRAM

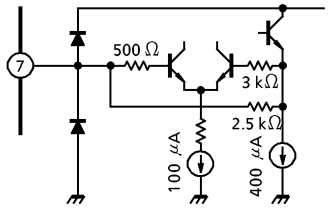
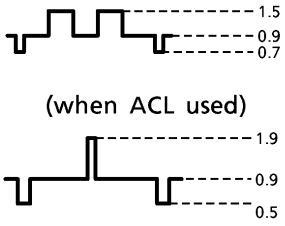
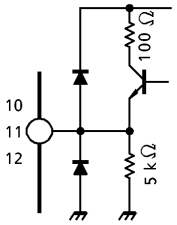
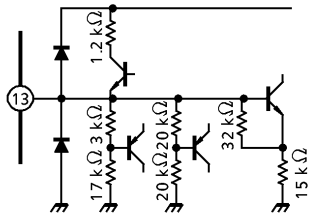
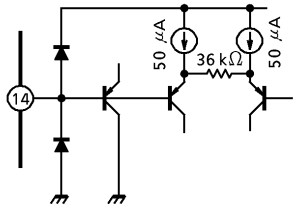
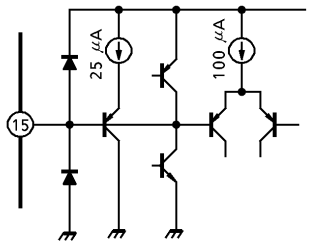


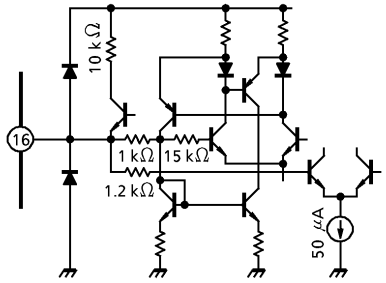
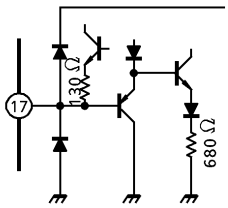
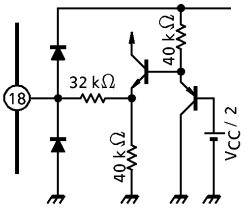
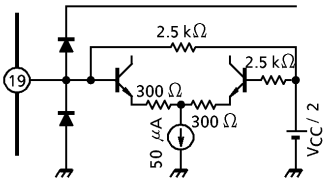
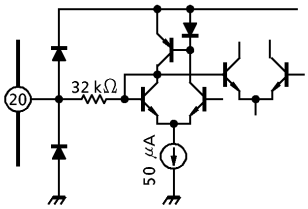
PIN FUNCTIONS

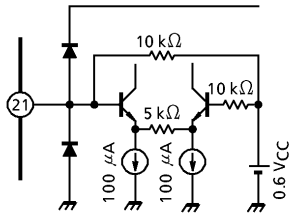
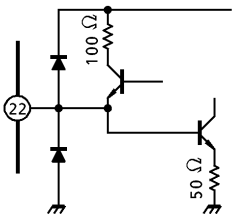
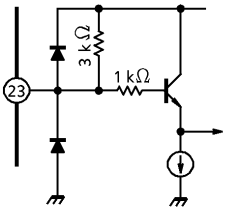
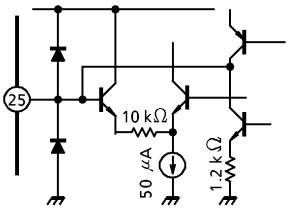
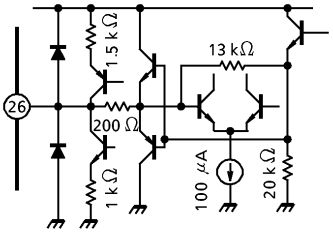
PIN NUMBER	PIN NAME	FUNCTION
1	SYNC GND	Ground for sync playback circuit
2	$\overline{HD}$ OUT	Horizontal output pulse to controller (open collector)
3	$\overline{VD}$ OUT	Vertical output pulse to controller (open collector)
4	CP / $\overline{LD}$ OUT	Sync pull-in signal output for selecting channel (open collector)
5	TINT	Tint adjustment pin
6	APC FILTER	Color subcarrier automatic control filter
7	f_{SC} X	f_{SC} resonator
8	V / C GND	Ground for video chroma circuit
9	COLOR	Color adjustment pin
10	R OUT	Primary color output pin (R)
11	G OUT	Primary color output pin (G)
12	B OUT	Primary color output pin (B)
13	V_{REF} / ACL LEVEL	Reference voltage / ACL level adjustment
14	BRIGHTNESS	Brightness adjustment pin
15	CLAMP C	Video DC playback capacitor
16	KILLER FILTER	Color killer filter
17	ACL FILTER	ACL filter
18	CONTRAST	Contrast (unicolor) adjustment pin
19	YH IN	Input of video high-frequency components
20	SHARPNESS	Sharpness adjustment pin
21	Y IN	Video signal input pin
22	ACC FILTER	Chroma automatic amplitude control filter
23	CHROMA IN	Chroma signal input pin
24	V_{CC}	Power supply
25	SYNC IN	Video signal input pin for sync playback
26	AFC FILTER	Horizontal automatic frequency control filter
27	VRET INTEG	Vertical sync integral capacitor
28	$32f_H$ X	$32f_H$ resonator
29	PH1	$32f_H$ oscillation phase pin
30	PH2	$32f_H$ oscillation phase pin

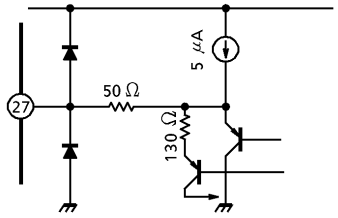
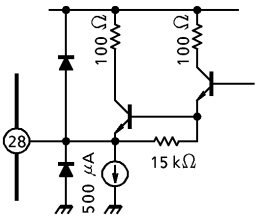
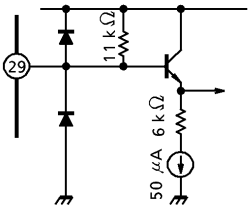
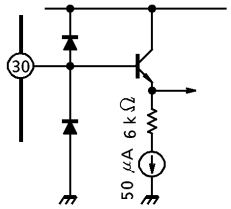
PIN DESCRIPTION

PIN NUMBER	PIN NAME & FUNCTION	TYPICAL SIGNAL LEVEL	INTERNAL CIRCUIT
2	$\overline{HD}$ OUT Horizontal drive pulse output	Saturated open collector output Maximum sink current 2 mA  V_{OH} = 5 V (uses separate power supply)	
3	$\overline{VD}$ OUT Vertical drive pulse output	Saturated open collector output Maximum sink current 2 mA  V_{OH} = 5 V (uses separate power supply)	
4	CP / $\overline{LD}$ Clamp pulse / signal output Pulse output	Saturated open collector output Maximum sink current 2 mA  V_{OH} = 5 V (uses separate power supply)	
5 9	TINT Tint adjustment COLOR Color amplitude adjustment	Internal bias V_{CC} / 2 V_{iH} max = V_{CC} V_{iL} min = GND	
6	APC DET APC filter connecting pin	Internal bias 2.5 V	

PIN NUM-BER	PIN NAME & FUNCTION	TYPICAL SIGNAL LEVEL	INTERNAL CIRCUIT
7	f_{SC} VXO f_{SC} resonator connecting pin	Internal bias 2.5 V V_{OSC} = 50 mV_{p-p}	
10 11 12	R-OUT G-OUT B-OUT Primary color output pins	 (when ACL used) (when ACL not used)	
13	V REF Constant voltage supply output pin	Internal bias 1.8 V	
14	BRIGHT Brightness adjustment control pin	V_{iH} max V REF (= 1.8 V) V_{iL} min GND	
15	CLAMP Clamp capacitor connecting pin	External capacitance 2.2 μF V_{OH} = V REF (= 1.8 V) V_{OL} = GND	

PIN NUM-BER	PIN NAME & FUNCTION	TYPICAL SIGNAL LEVEL	INTERNAL CIRCUIT
16	KILLER Color killer filter connecting pin	External capacitance 0.018 μF V_{OH} = 3.3 V V_{OL} = 2.6 V	
17	ACL ACL sample-and-hold capacitor pin	Internal bias 0 V	
18	CONTRAST Contrast (unicolor) adjustment control pin	Internal bias (V_{CC} / 2) V_{iH} = V_{CC} V_{iL} = GND	
19	Y_H IN Brightness signal (secondary differential) input pin	Internal bias (V_{CC} / 2) Maximum input level 150 mV_{p-p}	
20	SHARPNESS Sharpness adjustment control pin	Internal bias (V_{CC} / 2) V_{iH} = V_{CC} V_{iL} = GND	

PIN NUM-BER	PIN NAME & FUNCTION	TYPICAL SIGNAL LEVEL	INTERNAL CIRCUIT
21	Y_{IN} Brightness signal input pin	Internal bias 2.5 V Maximum input level 1 V_{p-p}	
22	ACC DET ACC sample-and-hold capacitor connecting pin	Permissible load current 0 V_{OL} = GND Load capacitance 0.1 μF	
23	C IN Chroma signal input pin	Internal bias V_{CC} Burst input 75 mV_{p-p} Chroma input 225 mV_{p-p}	
25	SYNC IN Composite sync signal input pin	Video signal 1 V_{p-p} (sync signal 0.28 V_{p-p}) Internal bias 1.5 V	
26	AFC DET AFC filter connecting pin	Internal bias 1.5 V	

PIN NUM-BER	PIN NAME & FUNCTION	TYPICAL SIGNAL LEVEL	INTERNAL CIRCUIT
27	VERT INT Vertical sync signal integral capacitor pin.	Internal bias 3.2 V Load capacitance 1 μF	
28	32f_H VXO 32f_H phase shift signal input pin	Internal bias 2.1 V V_{OL} = 2.5 V V_{OL} = 1.8 V	
29	PS-1 32f_H phase shift signal input pin 1	Internal bias 4.0 V (V_{CC})	
30	PS-2 32f_H phase shift signal input pin 2	Further shifts phase of pin 29 signal and inputs.	

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	8	V
Power Dissipation	P_D (Note)	890	mW
Power Dissipation Reduction Ratio	θ_{ja}	7.2	mW / °C
Operating Temperature	T_{opr}	− 20~75	°C
Storage Temperature	T_{stg}	− 55~150	°C

RECOMMENDED SUPPLY VOLTAGE

PIN NUM-BER	PIN NAME	MIN	TYP.	MAX	UNIT
24	V_{CC}	3.3	5.0	7.5	V

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, V_{CC} = 5 V, Ta = 25°C)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Quiescent Supply Current	I_{CCQ}	—		20	27	38	mA

Video block

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Pin 21 Input Impedance	Ri21	—	Note V-1	7	10	12.5	kΩ
Pin 19 Input Impedance	Ri19	—	Note V-2	1.8	2.5	3.25	kΩ
Brightness Adjustment Voltage	V_{BR}	—	Note V-3	0.7	0.84	0.98	V
Brightness Adjustment Sensitivity	G_{BR}	—	Note V-4	1.0	1.2	1.4	
Brightness Adjustment Range	ΔV_{BR}	—	Note V-5	1.9	2.1	2.3	V_{p-p}
Minimum Linear Video Input	$V_{di\ 1}$	—	Note V-6	—	2.6	3.1	V
Maximum Linear Video Input	$V_{di\ 2}$	—	Note V-7	3.3	4	—	V
Video Input Dynamic Range	V_{di}	—	Note V-8	0.75	0.88	—	V_{p-p}
Minimum Contrast Output	$V_{do\ 1}$	—	Note V-9	—	0.2	0.4	V
Maximum Contrast Output	$V_{do\ 2}$	—	Note V-10	2.6	3.1	—	V
Secondary Differential Input Dynamic Range	V_{dip}	—	Note V-11	0.09	0.12	0.15	V_{p-p}
AC Gain	G_V	—	Note V-12	12	14	15.6	dB
Frequency Characteristic	G_f	—	Note V-13	1.8	2.5	—	MHz
Contrast Adjustment Voltage Range	ΔV_{ct}	—	Note V-14	2.2	2.6	—	V
Contrast Adjustment Gain Range	ΔG_{ct}	—	Note V-15	14	15	—	dB
Frequency Characteristic Change Due to Contrast Adjustment	ΔG_f	—	Note V-16	−3	—	3	dB
Gain Change Amount at Minimum Sharpness Adjustment	$G_{PS}MIN$	—	Note V-17	14	—	—	dB
Gain Change Amount at Maximum Sharpness Adjustment	$G_{PS}MAX$	—	Note V-18	3	6	10	dB
Sharpness Adjustment Characteristic	$G_{PS}O$	—	Note V-19	−8	−4	0	dB
Pin 13 Output Voltage	V_{ref}	—	Note V-20	1.8	1.9	2.0	V
Pedestal Potential After ACL Adjustment	$A_{on\,/\,of}$	—	Note V-21	1.0	1.05	1.1	V
White Amplitude After ACL Adjustment	$A_{H\ 1}$	—	Note V-22	0.56	0.67	0.80	V_{p-p}
3-Axis Output DC Deviation (B / G)	$V_{of\,B\,/\,G}$	—	Note V-23	−200	—	200	mV

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
3-Axis Output DC Deviation (R / G)	V_{of} R / G	—	Note V-24	– 200	—	200	mV
3-Axis AC Gain Deviation (B / G)	ΔG B / G	—	Note V-25	– 6	—	0.5	dB
3-Axis AC Gain Deviation (R / G)	ΔG R / G	—	Note V-26	– 6	—	0.5	dB

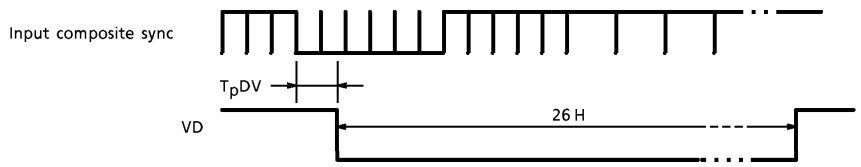
Chroma block

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Pin 23 Input Resistance	Ri23	—	Note C-1	2.25	3.0	3.75	kΩ
Color Difference Output (R-Y)	eR2	—	Note C-2	0.30	0.43	0.56	V_{p-p}
Color Difference Output (G-Y)	eG2	—	Note C-3	0.12	0.18	0.24	V_{p-p}
Color Difference Output (B-Y)	eB2	—	Note C-4	0.35	0.50	0.65	V_{p-p}
Color Change Amount	eC	—	Note C-5	4	6	—	dB
Unicolor Change Amount	eU	—	Note C-6	14	15	—	dB
Tint Change Amount	θt	—	Note C-7	80	100	130	°
Tint Center	θtc	—	Note C-8	– 15	—	5	°
Residual Color		—	Note C-9	—	—	– 40	dB
Demodulation Relative Amplitude (R-Y / B-Y)	R / B	—	Note C-10	0.72	0.84	0.96	—
Demodulation Relative Amplitude (G-Y / B-Y)	G / B	—	Note C-11	0.27	0.34	0.41	—
Demodulation Relative Phase (R-Y / B-Y)	R-B	—	Note C-12	97	104	111	°
Demodulation Relative Phase (G-Y / B-Y)	G-B	—	Note C-13	225	240	250	°
Demodulation Output Residual Carrier	eCR	—	Note C-14	—	—	15	mV_{p-p}
Killer Operation Input Level	eK	—	Note C-15	– 58	– 50	– 44	dB
ACC Characteristic	ACC	—	Note C-16	24	30	—	dB
Control Sensitivity	βfs	—	Note C-17	0.8	—	2.0	Hz / mV
APC Pull-In Range	fsp	—	Note C-18	± 300	—	—	Hz
APC Hold Range	fsh	—	Note C-19	± 300	—	—	Hz

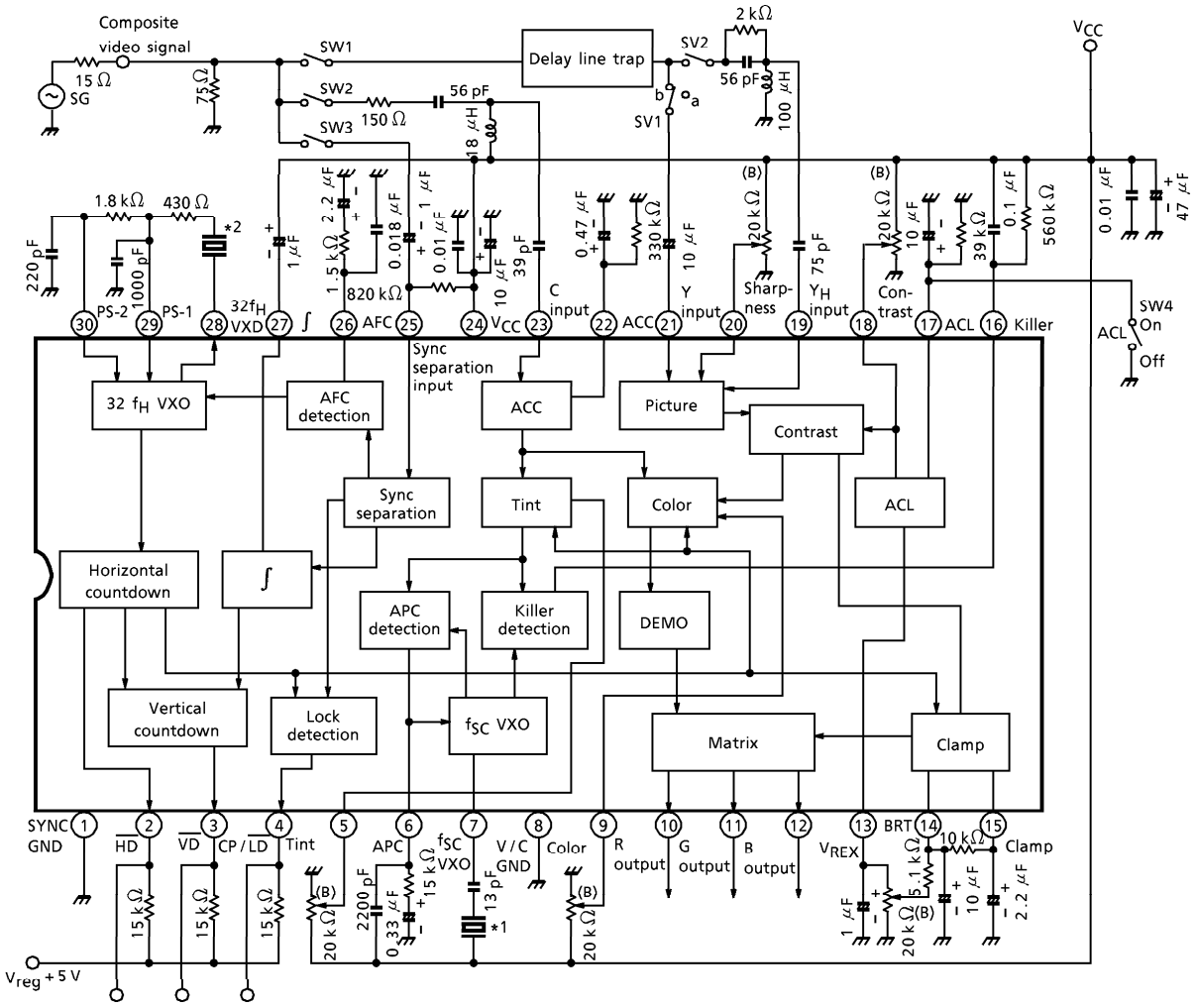
Sync block

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Horizontal Output Pulse Width	P_{WHD}	—	Note D-1	6.0	6.2	6.6	μs
Horizontal Output Pulse Delay Time	T_{pdH}	—	Note D-2	0.36	0.52	0.68	μs
Horizontal Output Saturation Level	V_{olH}	—	Note D-3	—	0.2	0.4	V
Vertical Output Pulse Width	P_{WVD}	—	Note D-4	—	26	26.5	H
Vertical Output Pulse Delay Time	T_{pDV}	—	Note D-5	0.65	0.84	1.03	H
Horizontal Oscillation Frequency	fH	—	Note D-6	15655	15734	15813	Hz
Horizontal AFC Pull-In Range	Δf_{pul}	—	Note D-7	600	700	—	Hz
Horizontal AFC Hold Range	Δf_{hol}	—	Note D-8	600	700	—	Hz
Horizontal AFC Hold Limit Input	V_{inPM}	—	Note D-9	—	—	−20	dB
Gate Pulse Width	P_{WGP}	—	Note D-10	2.6	3.0	3.45	μs
Gate Pulse Delay Time	T_{pdGP}	—	Note D-11	0.65	0.90	1.15	μs
Gate Pulse Generation Limit Input	V_{inGM}	—	Note D-12	—	—	−17	dB
Vertical Sync Pull-In Range	fpv 1	—	Note D-13	—	—	228	H
	fpv 2	—	Note D-14	228	—	—	
Vertical Sync Hold Limit Input	V_{inVM}	—	Note D-15	—	—	−15	dB

VD TIMING PULSE



V/C/S IC TEST CIRCUIT

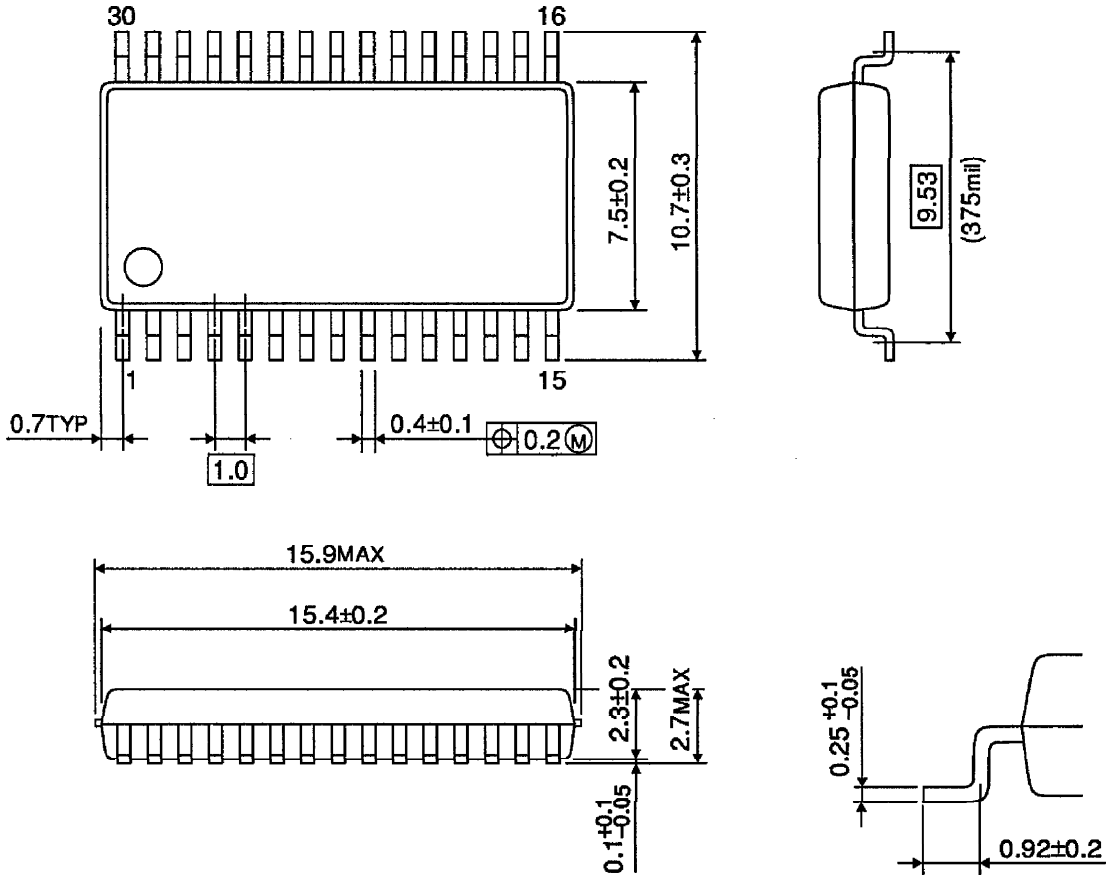


(*1) : 3.58 MHz X'tal NR-18 (HC-49 / U) (made by Nihon Denpa Kogyo Co, Ltd)

(*2) : 32-f_H ceramic oscillator CSB503F10 (made by Murata Manufacturing, Co, Ltd)

PACKAGE DIMENSIONS

SSOP30-P-375-1.00 Unit : mm



Weight : 0.63 g (Typ.)