ANALOG DEVICES

Integrated Synthesizer and VCO

Preliminary Technical Data — ADF4360-2

FEATURES

Output Frequency Range: 1800 MHz to 2150 MHz
Divide-by-2 output
+3.0 V to +3.6V Power Supply
1.8 V Logic Compatibility
Integer-N Synthesizer
Programmable Dual Modulus Prescaler
8/9, 16/17, 32/33
Programmable Output Power Level
3-Wire Serial Interface
Analog and Digital Lock Detect
Hardware and Software Power Down Mode

APPLICATIONS

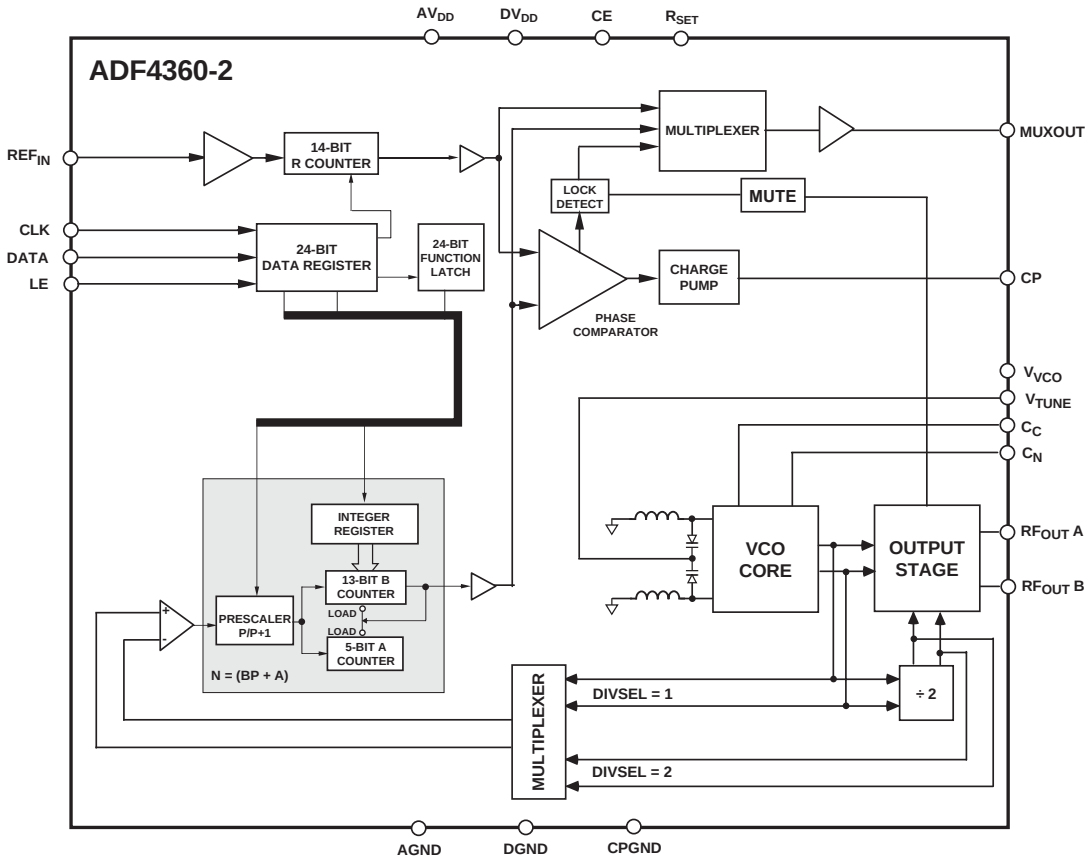
Wireless Handsets (DECT, GSM, PCS, DCS, WCDMA)
Test Equipment
Wireless LANS
CATV Equipment

GENERAL DESCRIPTION

The ADF4360-2 is a fully integrated integer-N synthesizer and voltage controlled oscillator (VCO). The ADF4360-2 is designed for a center frequency of 2000MHz. In addition, there is a divide-by-2 option available, whereby the user gets an RF output of between 900MHz and 1075MHz.

Control of all the on-chip registers is via a simple 3-wire interface. The device operates with a power supply ranging from 3.0V to 3.6V and can be powered down when not in use.

ADF4360-2 FUNCTIONAL BLOCK DIAGRAM



REV. PrA 07/03

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ADF4360-2 SPECIFICATIONS[1]

(AV_{DD} = DV_{DD} = V_{VCO} = +3.3V ± 10%; AGND = DGND = 0 V; T_A = T_{MIN} to T_{MAX} unless otherwise noted)

Parameter		Units	Test Conditions/Comments
REFIN CHARACTERISTICS			
REFIN Input Frequency	10/250	MHz min/max	For f < 10MHz, use dc-coupled CMOS compatible square wave
REFIN Input Sensitivity	-3/0	dBm min/max	AC coupled.
	0 to AV_{DD}	Volts max	(CMOS compatible)
REFIN Input Capacitance	5.0	pF max	
REFIN Input Current	±100	µA max	
PHASE DETECTOR			
Phase Detector Frequency[2]	8	MHz max	
CHARGE PUMP			
I_{CP} sink/source[3]			With R_{SET} = 4.7kΩ
High Value	2.5	mA typ	
Low Value	0.312	mA typ	
R_{SET} Range	2.7/10	kΩ	
I_{CP} 3-State Leakage Current	0.2	nA typ	
Sink and Source Current Matching	2	% typ	1.25V ≤ V_{CP} ≤ 2.5
I_{CP} vs. V_{CP}	1.5	% typ	1.25V ≤ V_{CP} ≤ 2.5
I_{CP} vs. Temperature	2	% typ	V_{CP} = 2.0V
LOGIC INPUTS			
V_{INH}, Input High Voltage	1.5	V min	
V_{INL}, Input Low Voltage	0.6	V max	
I_{INH}/I_{INL}, Input Current	±1	µA max	
C_{IN}, Input Capacitance	3.0	pF max	
LOGIC OUTPUTS			
V_{OH}, Output High Voltage	DV_{DD}-0.4	V min	CMOS output chosen
I_{OH}	500	µA max	
V_{OL}, Output Low Voltage	0.4	V max	I_{OL} = 500µA
POWER SUPPLIES			
AV_{DD}	3.0/3.6	V min/V max	
DV_{DD}	AV_{DD}		
VVco	AV_{DD}		
AI_{DD}[4]	10	mA typ	
DI_{DD}[4]	2.5	mA typ	
I_{VCO}[4,5]	24.0	mA typ	I_{CORE} = 15mA.
I_{RFOUT}[4]	3.5-11.0	mA typ	RF Output Stage is Programmeable
Low Power Sleep Mode	7	µA typ	
RF OUTPUT CHARACTERISTICS[5]			
VCO Output Frequency	1800/2150	MHz min/max	I_{CORE} = 15mA.
VCO Sensitivity	57	MHz/Volt	
Lock Time	400	us typ	To within 10Hz of final frequency.
Frequency Pushing, (Open Loop)	TBD	MHz/Volt typ	
Frequency Pulling, (Open Loop)	TBD	kHz typ	Into 2.00 VSWR Load
Harmonic Content (2nd)	-20	dBc typ	
(3rd)	-35	dBc typ	
Output Power[5,7]	-13/-6	dBm typ	Programmable in 3dB steps.Table 3.
Output Power Variation	+/- 3	dB typ	For Tuned loads see page 18.
VCO Tuning Range	1.25/2.5	V min/max	

NOTES
1. Operating temperature range is as follows: B Version: –40°C to +85°C.
2. Guaranteed by design. Sample tested to ensure compliance.
3. I_{CP} is internally modified to maintain constant loop gain over the frequency range.
4. T_A = +25°C; AV_{DD} = DV_{DD} = V_{VCO} = 3.3V; P = 32.
5. These Characteristics are guaranteed for VCO Core Power = 15mA.
6. Jumping from 1.8GHz to 2.15GHz. PFD frequency = 200kHz, Loop bandwidth = 10kHz.
7. Using 50Ohm resistors to VVco, Into a 50Ohm load. For Tuned Loads see page 18.

ADF4360-2 SPECIFICATIONS[1]

(AV_{DD} = DV_{DD} = V_{VCO} = +3.3V ± 10%; AGND = DGND = 0 V; T_A = T_{MIN} to T_{MAX} unless otherwise noted)

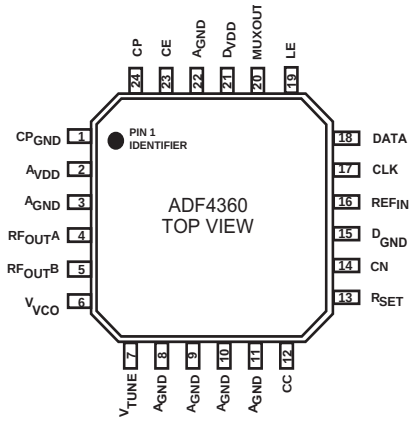
Parameter	Typical	Units	Test Conditions/Comments
NOISE CHARACTERISTICS			
VCO Phase Noise Performance[2]	-110	dBc/Hz	@ 100kHz offset from carrier
	-130	dBc/Hz	@ 1MHz offset from carrier
	-141	dBc/Hz	@ 3MHz offset from carrier
Synthesizer Phase Noise Floor[3]	-172	dBc/Hz	@ 25kHz PFD Frequency
	-163	dBc/Hz	@ 200kHz PFD Frequency
	-147	dBc/Hz	@ 8MHz PFD Frequency
Inband Phase Noise[4,5]	-83	dBc/Hz	@ 1kHz offset from carrier
RMS Integrated Phase Error[6]	0.64	degrees	(100Hz-100kHz)
Spurious Signals due to PFD Frequency[5,7]	-70	dBc	

NOTES
1. Operating temperature range is as follows: –40°C to +85°C. All measurements on this page for Core Power = 15mA.
2. The noise of the VCO is meaured in open-loop conditions.
3. The synthesizer phase noise floor is estimated by measuring the in-band phase noise at the output of the VCO and subtracting 20logN (where N is the N divider value).
4. The phase noise is measured with the EVAL-ADF4360-xEB1 Evaluation Board and the HP8562E Spectrum Analyzer. The spectrum analyzer provides the REFIN for the synthesizer, f_{REFIN} = 10MHz; Offset frequency = 1 kHz.
5. f_{REFIN} = 10 MHz; f_{PFD} = 200 kHz; N = 10000; Loop B/W = 10kHz.
6. f_{REFIN} = 10 MHz; f_{PFD} = 1 MHz; N = 2000; Loop B/W = 25kHz.
7. The spurious signals are measured with the EVAL-ADF4360-xEB1 Evaluation Board and the HP8562E Spectrum Analyzer. The spectrum analyzer provides the REFIN for the synthesizer (f_{REFOUT} = 10MHz @ 0dBm).

ORDERING GUIDE

Model	Temperature Range	Frequency Range	Package Option*
ADF4360-1BCP	–40°C to +85°C	2050-2450 MHz	CP-24
ADF4360-2BCP	–40°C to +85°C	1700-2200 MHz	CP-24
ADF4360-3BCP	–40°C to +85°C	1550-1950 MHz	CP-24
ADF4360-4BCP	–40°C to +85°C	1400-1800 MHz	CP-24
ADF4360-5BCP	–40°C to +85°C	1150-1400 MHz	CP-24
ADF4360-6BCP	–40°C to +85°C	1000-1250 MHz	CP-24
ADF4360-7BCP	–40°C to +85°C	Set by External L	CP-24

PIN CONFIGURATION
TOP VIEW



TIMING CHARACTERISTICS

(AV_{DD} = DV_{DD} = V_{VCO} = +3.3V ± 10%; AGND = DGND = 0 V; 1.8V and 3V Logic Levels Used; T_A = T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	Limit at T_{MIN} to T_{MAX} (B Version)	Units	Test Conditions/Comments
t_1	20	ns min	LE Set Up Time
t_2	10	ns min	DATA to CLOCK Set Up Time
t_3	10	ns min	DATA to CLOCK Hold Time
t_4	25	ns min	CLOCK High Duration
t_5	25	ns min	CLOCK Low Duration
t_6	10	ns min	CLOCK to LE Set Up Time
t_7	20	ns min	LE Pulse Width

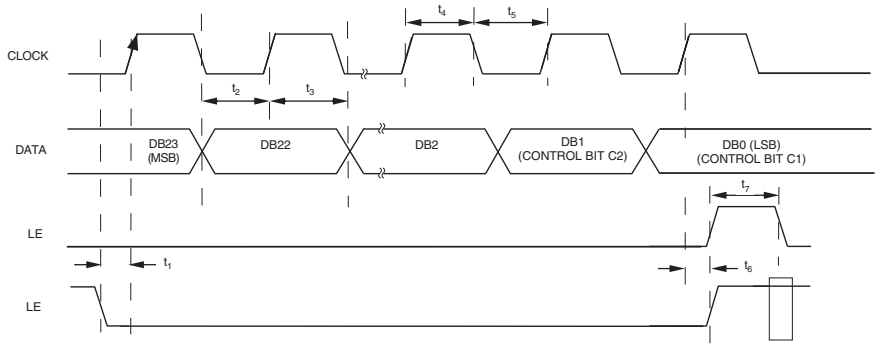


Figure 1. Timing Diagram

ABSOLUTE MAXIMUM RATINGS[1, 2]

(T_A = +25°C unless otherwise noted)

AV_{DD} to GND[3].....–0.3 V to +3.9 V
AV_{DD} to DV_{DD} .....–0.3 V to +0.3 V
V_{VCO} to GND.....–0.3 V to +3.9 V
V_{VCO} to AV_{DD} .....–0.3 V to +0.3 V
Digital I/O Voltage to GND.....–0.3 V to V_{DD} + 0.3 V
Analog I/O Voltage to GND.....–0.3 V to V_{DD} + 0.3 V
REF_{IN}, to GND.....–0.3 V to V_{DD} + 0.3 V
OperatingTemperature Range
Maximum Junction Temperature.....+150°C
CSP θ_{JA} Thermal Impedance
(Paddle Soldered).....50°C/W
(Paddle Not Soldered).....88°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec).....+215°C
Infrared (15 sec).....+220°C

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. This device is a high-performance RF integrated circuit with an ESD rating of < 1kV and it is ESD sensitive. Proper precautions should be taken for handling and assembly.

3. GND = AGND = DGND = 0V

TRANSISTOR COUNT

12543 (CMOS) and 700 (Bipolar)

CAUTION

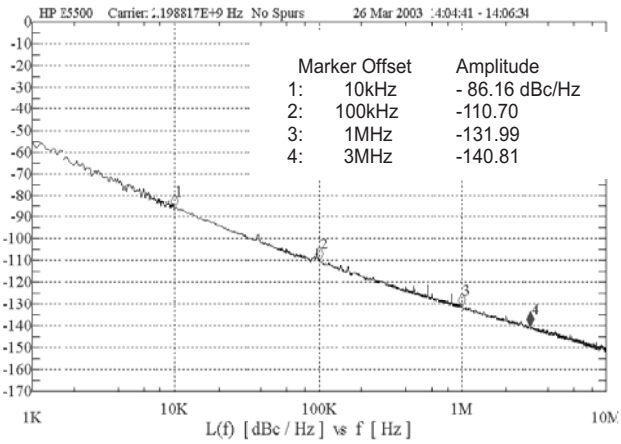
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADF4360 family features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN DESCRIPTION

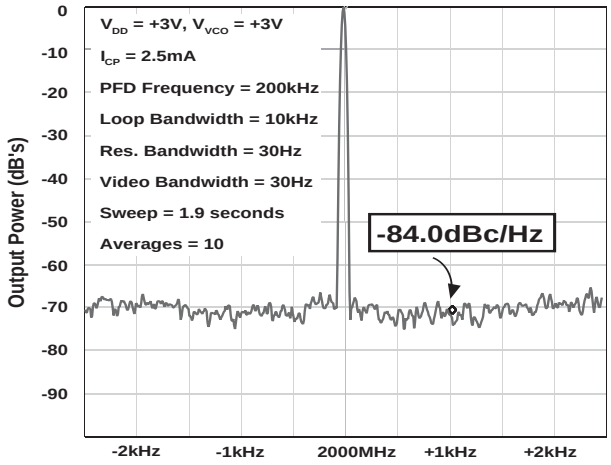
Mnemonic	Function
AV_{DD}	Analog Power Supply. This may range from 3.0V to 3.6V. Decoupling capacitors to the analog ground plane should be placed as close as possible to this pin. AV_{DD} must be the same value as DV_{DD}.
DV_{DD}	Digital Power Supply. This may range from 3.0V to 3.6V. Decoupling capacitors to the digital ground plane should be placed as close as possible to this pin. DV_{DD} must be the same value as AV_{DD}.
V_{VCO}	Power supply for the VCO. This may range from 3.0V to 3.6V. Decoupling capacitors to the analog ground plane should be placed as close as possible to this pin. V_{VCO} must be the same value as AV_{DD}.
R_{SET}	Connecting a resistor between this pin and CPGND sets the maximum charge pump output current for the synthesizer. The nominal voltage potential at the R_{SET} pin is 0.6V. The relationship between I_{CP} and R_{SET} is $$I_{CPmax} = \frac{11.75}{R_{SET}}$$ So, with R_{SET} = 4.7kΩ, I_{CPmax} = 2.5mA.
MUXOUT	This multiplexer output allows either the Lock Detect, the scaled RF or the scaled Reference Frequency to be accessed externally.
CP	Charge Pump Output. When enabled this provides $\pm I_{CP}$ to the external loop filter, which in turn drives the internal VCO.
V_{TUNE}	Control input to the VCO. This voltage determines the output frequency and is derived from filtering the CP_{OUT} voltage.
C_C	Internal compensation node. This pin must be decoupled to ground with a 10nF capacitor.
C_N	Internal compensation node. This pin must be decoupled to V_{VCO} with a 10uF capacitor.
$RF_{OUT}A$	VCO output. The output level is programmable from -6dBm to -13dBm. See Page 18 for a description of various output stages.
$RF_{OUT}B$	VCO complementary output. The output level is programmable from -6dBm to -13dBm. See Page 18 for a description of various output stages.
CPGND	Charge Pump Ground. This is the ground return path for the charge pump.
DGND	Digital Ground.
AGND	Analog Ground. This is the ground return path of the prescaler & VCO.
LE	Load Enable, CMOS Input. When LE goes high, the data stored in the shift registers is loaded into one of the four latches, the relevant latch is selected using the control bits.
DATA	Serial Data Input. The serial data is loaded MSB first with the two LSBs being the control bits. This input is a high impedance CMOS input.
CLK	Serial Clock Input. This serial clock is used to clock in the serial data to the registers. The data is latched into the 24-bit shift register on the CLK rising edge. This input is a high impedance CMOS input.
CE	Chip Enable. A logic low on this pin powers down the device and puts the charge pump into three state mode. Taking the pin high will power up the device depending on the status of the power-down bits.
REFIN	Reference Input. This is a CMOS input with a nominal threshold of $V_{DD}/2$ and a dc equivalent input resistance of 100kΩ. See Figure 2. This input can be driven from a TTL or CMOS crystal oscillator or it can be ac coupled.

ADF4360-2

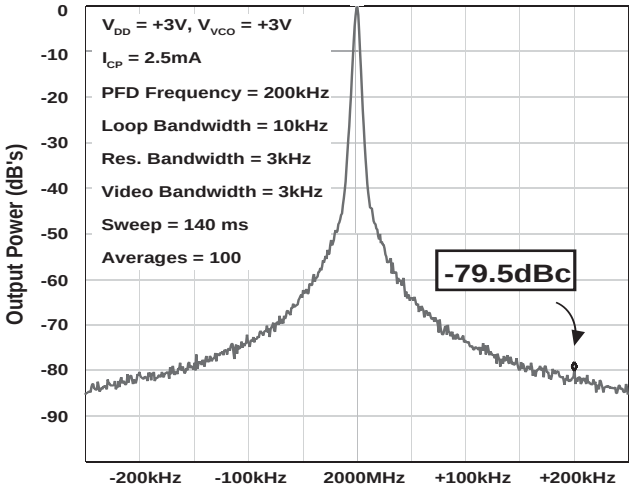
Typical Performance Characteristics:



TPC 1. Open Loop VCO Phase Noise

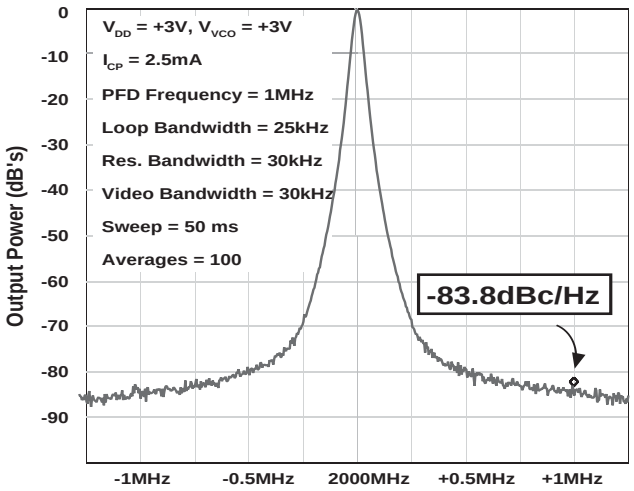


TPC 4. Close-In Phase Noise at 2000MHz (200kHz Channel Spacing)



TPC 2. VCO Phase Noise, 2000MHz, 200kHz PFD, 10kHz loop bandwidth.

TPC 5. Reference Spurs at 2000MHz (200kHz Channel Spacing, 10kHz loop bandwidth)



TPC 3. VCO Phase Noise, 1000MHz, Divide by 2 Enabled 200kHz PFD, 10kHz loop bandwidth.

TPC 6 Reference Spurs at 2000MHz (1MHz Channel Spacing, 25kHz loop bandwidth)

CIRCUIT DESCRIPTION

REFERENCE INPUT SECTION

The Reference Input stage is shown below in Figure 2. SW1 and SW2 are normally-closed switches. SW3 is normally-open. When Powerdown is initiated, SW3 is closed and SW1 and SW2 are opened. This ensures that there is no loading of the REF_{IN} pin on powerdown.

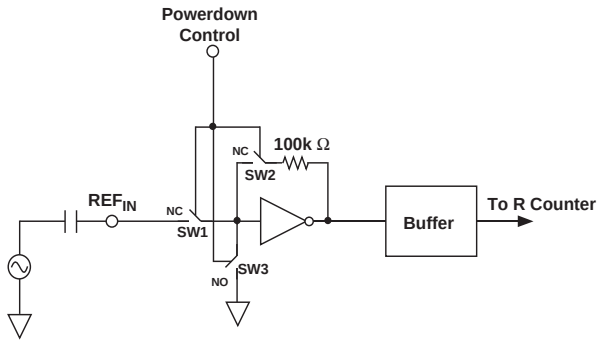


Figure 2. Reference Input Stage

PRESCALER (P/P+1)

The dual modulus prescaler (P/P+1), along with the A and B counters, enables the large division ratio, N, to be realised (N = BP + A). The dual-modulus prescaler, operating at CML levels, takes the clock from the VCO and divides it down to a manageable frequency for the CMOS A and B counters. The prescaler is programmable. It can be set in software to 8/9, 16/17 or 32/33. It is based on a synchronous 4/5 core. There is a minimum divide ratio possible for fully contiguous output frequencies. This minimum is determined by P, the prescaler value and is given by: (P^2-P).

A AND B COUNTERS

The A and B CMOS counters combine with the dual modulus prescaler to allow a wide ranging division ratio in the PLL feedback counter. The counters are specified to work when the prescaler output is 300MHz or less. Thus, with an VCO frequency of 2.5GHz, a prescaler value of 16/17 is valid but a value of 8/9 is not valid.

Pulse Swallow Function

The A and B counters, in conjunction with the dual modulus prescaler make it possible to generate output frequencies which are spaced only by the Reference Frequency divided by R . The equation for the VCO frequency is as follows:

$$f_{VCO} = [(P \times B) + A] \times f_{REFIN}/R$$

f_{VCO} Ouput Frequency of voltage controlled oscillator (VCO).

P Preset modulus of dual modulus prescaler (8/9, 16/17, etc.,).

B Preset Divide Ratio of binary 13-bit counter (3 to 8191).

A Preset Divide Ratio of binary 5-bit swallow counter (0 to 31).

f_{REFIN} External reference frequency oscillator.

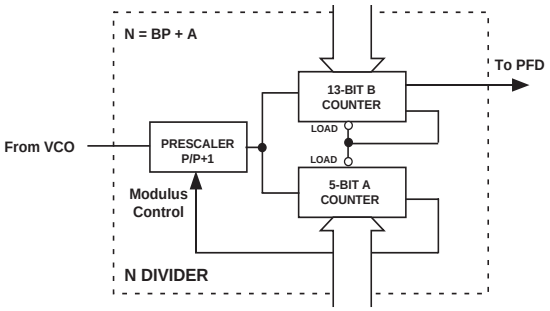


Figure 3. A and B Counters

R COUNTER

The 14-bit R counter allows the input reference frequency to be divided down to produce the reference clock to the phase frequency detector (PFD). Division ratios from 1 to 16,383 are allowed.

PHASE FREQUENCY DETECTOR (PFD) AND CHARGE PUMP

The PFD takes inputs from the R counter and N counter (N=BP+A) and produces an output proportional to the phase and frequency difference between them. Figure 4 is a simplified schematic. The PFD includes a programmable delay element which controls the width of the anti-backlash pulse. This pulse ensures that there is no deadzone in the PFD transfer function and minimizes phase noise and reference spurs. Two bits in the R Counter Latch, ABP2 and ABP1 control the width of the pulse. See Page 14.

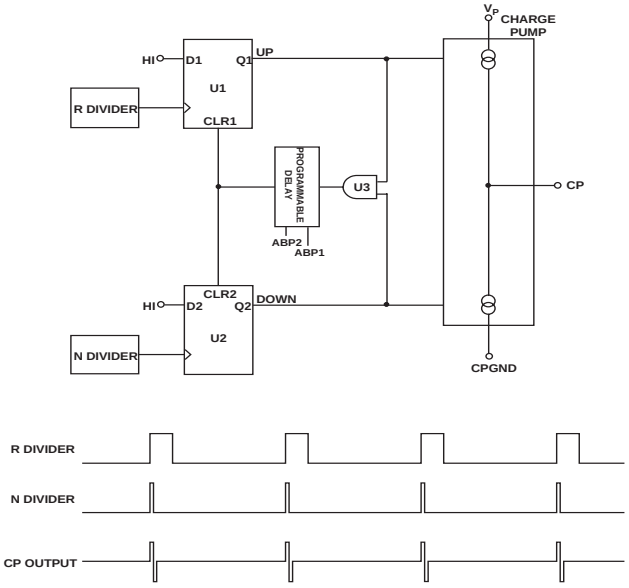


Figure 4. PFD Simplified Schematic and Timing (In Lock)

MUXOUT AND LOCK DETECT

The output multiplexer on the ADF4360 family allows the user to access various internal points on the chip. The state of MUXOUT is controlled by M3, M2 and M1 in the Function Latch. The full truth table is shown on page 13. Figure 5 shows the MUXOUT section in block diagram form.

Lock Detect

MUXOUT can be programmed for two types of lock detect: digital lock detect and analog lock detect.
Digital lock detect is active high. When LDP in the R Counter latch is set to 0, digital lock detect is set high when the phase error on three consecutive Phase Detector cycles is less than 15ns.

With LDP set to "1", five consecutive cycles of less than 15ns phase error are required to set the lock detect. It will stay set high until a phase error of greater than 25ns is detected on any subsequent PD cycle.
The N-channel open-drain analog lock detect should be operated with an external pull-up resistor of 10kΩ nominal. When lock has been detected this output will be high with narrow low-going pulses.

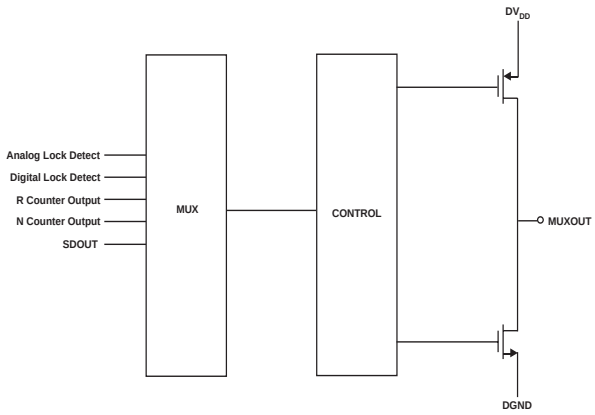


Figure 5. MUXOUT Circuit

INPUT SHIFT REGISTER

The ADF4360 family's digital section includes a 24-bit input shift register, a 14-bit R counter and a 18-bit N counter, comprising a 5-bit A counter and a 13-bit B counter. Data is clocked into the 24-bit shift register on each rising edge of CLK. The data is clocked in MSB first. Data is transferred from the shift register to one of four latches on the rising edge of LE. The destination latch is determined by the state of the two control bits (C2, C1) in the shift register. These are the two lsb's DB1, DB0 as shown in the timing diagram of Figure 1. The truth table for these bits is shown in Table 1. Table 2 shows a summary of how the latches are programmed. Please note that the Test Modes Latch is used for Factory Testing snd should not be programmed by the user.

Table I. C2, C1 Truth Table

Control Bits C2	Control Bits C1	Data Latch
0	0	Control Latch
0	1	R Counter
1	0	N Counter (A & B)
1	1	Test Modes Latch

0000–0–01/00 (rev. 0) 00000

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VCO

The VCO core in the ADF4360 family uses eight overlapping bands as shown in figure 6 to allow a wide frequency range to be covered without a large VCO sensitivity (Kv) and resultant poor phase noise and spurious performance.

The correct band is chosen automatically by the band select logic at power-up or whenever the N Counter latch is updated. It is important that the correct write sequence be followed at power-up. This sequence is:

1) R Counter latch

2) Control latch

3) N Counter latch

During band select, which takes five PFD cycles, The VCO Vtune is disconnected from the output of the loop filter and connected to an internal reference voltage.

Figure 6 Frequency vs Vtune, ADF4360-2

The R Counter output is used as the clock for the band select logic and should not exceed 1MHz. A programmable divider is provided at the R Counter input to allow division by 1,2,4 or 8, and is controlled by bits BSC1 and BSC2 in the R Counter Latch. Where the required PFD frequency exceeds 1 MHz the divide ratio should be set to allow enough time for correct band selection.

After band select, normal PLL action resumes. The nominal value of Kv is 57MHz/Volt or 28MHZ/Volt if divide by two operation has been selected (by programming DIVSEL (DB22), high in the N Counter latch). The ADF4360 family contains linearisation circuitry to minimise any variation of the product of Icp and Kv.

The operating current in the VCO core is programmable in four steps, 5mA, 10mA, 15mA & 20mA. This is controlled by bits PC1 & PC2 in the Control latch.

OUTPUT STAGE

The RFoutA and RFoutB pins of the ADF4360 family are connected to the collectors of an NPN differential pair driven by buffered outputs of the VCO as shown in figure 7. To allow the user to optimise his/her power dissipation vs output power requirements, The tail current of the differential pair is programmable via bits PL1 & PL2 in the Control latch. Four current levels may be set; 3.5mA, 5mA, 7.5mA and 11mA giving output power levels of -13dBm, -10.5dBm, -8dBm & -6dBm using a 50Ohm resistor to Vdd and ac-coupling into a 50Ohm load. Alternatively, both outputs can be combined in a 1+1:1 transformer or a 180° microstrip coupler. See Page 19.

If the outputs are to be used individually, then the optimum output stage consists of a shunt inductor to Vdd.

Another feature of the ADF4360 family is provided whereby the supply current to the RF output stage is shut down until the part achieves lock as measured by the Digital Lock Detect circuitry. This is enabled by the MTLD (Mute Till Lock Detect) bit in the Control latch.

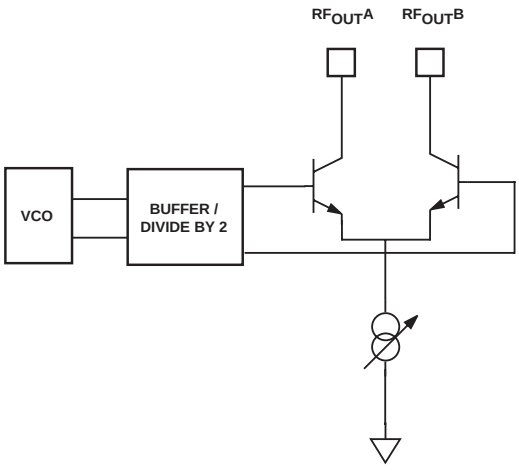

Figure 7 RF Output Stage ADF4360-2

TABLE II: LATCH STRUCTURE

The diagram below shows the three on-chip latches for the ADF4360 family. The two LSB's decide which latch is programmed.

Control Latch

Prescaler Value		Power Down 2	Power Down 1	Current Setting 2			Current Setting 1			Output Power Level		Mute Till LD	CP Gain	CP 3-State	Phase Detector Polarity	MUXOUT Control			Counter Reset	Core Power Level		Control Bits	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P2	P1	PD2	PD1	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	PL2	PL1	MTLD	CPG	CP	PDP	M3	M2	M1	CR	PC2	PC1	C2 (0)	C1 (0)

N Counter Latch

Divide by 2 Select	Divide by 2	CP Gain	13-Bit B Counter													Reserved	5-Bit A Counter					Control Bits	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
DIVSEL	DIV2	CPG	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	RSV	A5	A4	A3	A2	A1	C2 (1)	C1 (0)

R Counter Latch

Reserved		Band Select Clock		Test Mode Bit	Lock Detect Precision	Anti Backlash Width		14-Bit Reference Counter, R														Control Bits	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
RSV	RSV	BSC2	BSC1	TMB	LDP	ABP2	ABP1	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2 (0)	C1 (1)

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TABLE III: CONTROL LATCH

Prescaler Value		Power Down 2	Power Down 1	Current Setting 2			Current Setting 1			Output Power Level		Mute Till LD	CP Gain	CP 3-State	Phase Detector Polarity	MUXOUT Control			Counter Reset	Core Power Level		Control Bits	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P2	P1	PD2	PD1	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	PL2	PL1	MTLD	CPG	CP	PDP	M3	M2	M1	CR	PC2	PC1	C2 (0)	C1 (0)

PC2	PC1	Core Power Level
0	0	5mA
0	1	10mA
1	0	15mA
1	1	20mA

CPI6	CPI5	CP14	I_{CP} (mA)
CPI3	CPI2	CPI1	4.7kΩ
0	0	0	0.31
0	0	1	0.62
0	1	0	0.93
0	1	1	1.25
1	0	0	1.56
1	0	1	1.87
1	1	0	2.18
1	1	1	2.50

PDP	Phase Detector Polarity
0	Negative
1	Positive

CR	Counter Operation
0	Normal
1	R, A, B Counters held in Reset

CP	Charge Pump Output
0	Normal
1	3-State

CPG	CP Gain
0	Current Setting 1
1	Current Setting 2

MTLD	Mute Till Lock Detect
0	Disabled
1	Enabled

P2	P1	Output Power Level	
		Current	Power into 50Ohm, (using 50Ohm to Vvco)
0	0	3.5mA	-6dBm
0	1	5.0mA	-8dBm
1	0	7.5mA	-10.5dBm
1	1	11.0mA	-13.0dBm

M3	M2	M1	Output
0	0	0	3-State Output
0	0	1	Digital Lock Detect (Active High)
0	1	0	N Divider Output
0	1	1	DV_{DD}
1	0	0	R Divider Output
1	0	1	N-Channel Open-Drain Lock Detect
1	1	0	Serial Data Output
1	1	1	DGND

CE Pin	PD2	PD1	Mode
0	X	X	Asynchronous Power-Down
1	X	0	Normal Operation
1	0	1	Asynchronous Power-Down
1	1	1	Synchronous Power-Down

P2	P1	Prescaler Value
0	0	8/9
0	1	16/17
1	0	32/33
1	1	32/33

TABLE IV: R COUNTER LATCH

Reserved	Reserved	Band Select Clock		Test Mode Bit	Lock Detect Precision	Anti Backlash Width		14-Bit Reference Counter														Control Bits	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
X	X	BSC2	BSC1	T1	LDP	ABP2	ABP1	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2 (0)	C1 (1)

X = Don't Care

These bits are not used by the device and are Don't Care Bits.

Test Mode Bit should be set to 0 for Normal Operation

R14	R13	R12	.....	R3	R2	R1	Divide Ratio
0	0	0	.....	0	0	1	1
0	0	0	.....	0	1	0	2
0	0	0	.....	0	1	1	3
0	0	0	.....	1	0	0	4
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
1	1	1	.....	1	0	0	16380
1	1	1	.....	1	0	1	16381
1	1	1	.....	1	1	0	16382
1	1	1	.....	1	1	1	16383

ABP2	ABP1	Anti-Backlash Pulse Width
0	0	3.0ns
0	1	1.3ns
1	0	6.0ns
1	1	3.0ns

LDP	Lock Detect Precision
0	3 consecutive cycles of phase delay less than 15ns must occur before lock detect is set.
1	5 consecutive cycles of phase delay less than 15ns must occur before lock detect is set.

BSC2	BSC1	Band Select Clock Divider
0	0	1
0	1	2
1	0	4
1	1	8

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TABLE V: N COUNTER LATCH

Reserved		CP Gain	13-Bit B Counter													Reserved	5-Bit A Counter					Control Bits	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
X	X	CPG	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	RSV	A5	A4	A3	A2	A1	C2 (1)	C1 (0)

X = Don't Care

These bits are not used by the device and are Don't Care Bits.

A5	A4	.....	A2	A1	A Counter Divide Ratio
0	0	.....	0	0	0
0	0	.....	0	1	1
0	0	.....	1	0	2
0	0	.....	1	1	3
.	.	.....	.	.	.
.	.	.....	.	.	.
.	.	.....	.	.	.
1	1	.....	0	0	28
1	1	.....	0	1	29
1	1	.....	1	0	30
1	1	.....	1	1	31

B13	B12	B11	.....	B3	B2	B1	B Counter Divide Ratio
0	0	0	.....	0	0	0	Not Allowed
0	0	0	.....	0	0	1	Not Allowed
0	0	0	.....	0	1	0	Not Allowed
0	0	0	.....	1	1	1	3
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
1	1	1	.....	1	0	0	8188
1	1	1	.....	1	0	1	8189
1	1	1	.....	1	1	0	8190
1	1	1	.....	1	1	1	8191

F4 (Function Latch) Fastlock Enable	CP Gain	Operation
0	0	Charge Pump Current Setting 1 is permanently used
0	1	Charge Pump Current Setting 2 is permanently used

N = BP + A, P is Prescaler value set in the Control Latch. B must be greater than or equal to A. For continuously adjacent values of (N x F_{REF}), at the output, N_{MIN} is (P^2 - P)

These bits are not used by the device and are Don't Care Bits.

CONTROL LATCH
With (C2, C1) = (0,0), the Control Latch is programmed. Table III shows the input data format for programming the Control latch.

Prescaler Value
In the ADF4360 family, P2 and P1 in the Control Latch set the Prescaler values.

Power-Down
DB21 (PD2) and DB20 (PD1) provide programmable power-down modes.

In the programmed asynchronous power-down, the device powers down immediately after latching a "1" into bit PD1, with the condition that PD2 has been loaded with a "0". In the programmed synchronous power-down, the device power down is gated by the charge pump to prevent unwanted frequency jumps. Once the power-down is enabled by writing a "1" into bit PD1 (on condition that a "1" has also been loaded to PD2), then the device will go into power-down on the second rising edge of the R counter output, after LE goes high.

When the CE pin is low, the device is immediately disabled regardless of the states of PD1 or PD2.

When a power down is activated (either synchronous or asynchronous mode), the following events occur:

All active DC current paths are removed.

The R, N and timeout counters are forced to their load state conditions.

The charge pump is forced into three-state mode.

The digital lock detect circuitry is reset.

The RF outputs are debiased to a high impedance state.

The reference input buffer circuitry is disabled.

The input register remains active and capable of loading and latching data.

Charge Pump Currents
CPI3, CPI2, CPI1 in the ADF4360 family determine Current Setting 1. CPI6, CPI5, CPI4 determine Current Setting 2. The truth table is given in Table III.

Output Power Level
Bits PL1 & PL2 set the output power level of the VCO. The truth table is given in Table III.

Mute Till Lock Detect
DB11 of the Control Latch in the ADF4360 family is the Mute Till Lock Detect Bit. This function, when enabled, ensures that the RF outputs are not switched on until the PLL has achieved lock.

CP Gain Bit
DB10 of the Control Latch in the ADF4360 family is the Charge Pump Gain bit. When this is programmed to a "1" then Current Setting 2 is used. When programmed to a "0", Current Setting 1 is used.

Charge Pump Three-State
This bit puts the charge pump into three-state mode when programmed to a "1". It should be set to "0" for normal operation.

Phase Detector Polarity
The PDP bit in the ADF4360 family sets the Phase Detector Polarity. The positive setting enabled by programming a "1" is used when using the on-chip VCO with a passive loop filter or with an active non-inverting filter. It can also be set to "0". This is required if an active inverting loop filter is used.

MUXOUT Control
The on-chip multiplexer is controlled by M3, M2, M1. Table 3 shows the truth table.

Counter Reset
DB4 is the counter reset bit for the ADF4360 family. When this is "1", the R counter and the A,B counters are reset. For normal operation this bit should be "0".

Core Power Level
PC1 and PC2 set the power level in the VCO core. The recommended setting is 15mA. The truth table is given in Table III.

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R COUNTER LATCH
With (C2, C1) = (0,1), the R Counter Latch is programmed.

R Counter
R1 to R14 sets the counter divide ratio. The divide range is 1 (00.....001) to 16383 (111.....111).

Anti-Backlash Pulse Width
DB16 and DB17 set the anti-backlash pulse width.

Lock Detect Precision Bit
DB18 is the Lock Detect Precision Bit and sets the number of references cycles with less than 15ns phase error for entering the locked state. With LDP at "1", 5 cycles are taken and with LDP at "0", 3 cycles are taken.

Test Mode Bit.
DB19 is the Test Mode Bit (TMB) and should be set to zero. With TMB = 0, the contents of the Test Mode Latch are ignored and normal operation occurs as determined by the contents of the Control Latch, R Counter Latch, and N Counter Latch. Please note that Test Modes are for Factory testing only, and should not be programmed by the user.

Band Select Clock Bits
These Bits set a divider for the band select logic clock input, The output of the R Counter is by default the value used to clock the band select logic, but if this value is too high (>1MHz), a divider can be switched in to divide the R counter output to a smaller value. See Table 4.

Reserved Bits
DB23 - DB22 are spare bits and have been designated as "Reserved". They should be programmed to "0".

N COUNTER LATCH
With (C2, C1) = (1,0), the N Counters Latch is programmed.

A Counter Latch
A5 - A1 program the 5-bit A counter. The divide range is 0 (00000) to 31 (11111).

Reserved Bits
DB7 is a spare bit and has been designated as "Reserved". It should be programmed to "0".

B Counter Latch
B13 - B1 program the B counter. The divide range here is 3 (00.....0011) to 8191 (11....111).

Overall Divide Range
The overall divide range is defined by ((PxB) + A), where P is the prescaler value.

CP Gain Bit
DB21 of the N Counter Latch in the ADF4360 family is the Charge Pump Gain bit. When this is programmed to a "1" then Current Setting 2 is used. When programmed to a "0", Current Setting 1 is used. This bit can also be programmed via DB10 of the Control Latch. The bit will always reflect the latest value written to it, whether this is through the Control Latch or the N Counter Latch.

Divide by 2
DB22 is the divide-by-2 bit. When set to a "1", the output divide by 2 function is chosen. When it is set to "0", normal operation occurs.

Divide by 2 Select
DB23 is the divide-by-2 select bit. When this is programmed to a "1", the divide-by-2 output is selected as the prescaler input. When it is set to a "0", the fundamental is used as the prescaler input. For Example: Using the Output Divide by Two feature, and a PFD frequency of 200kHz the user will need a value of N = 10000 to generate 1GHz. With the divide by two select bit high, the user may keep N = 5000.

ADF4360-2

APPLICATIONS SECTION
DIRECT CONVERSION MODULATOR

Direct Conversion Architectures are being increasingly used to implement base station transmitters. Figure 7 shows how ADI parts can be used to implement such a system.

The circuit block diagram shows the AD9761 TxDAC being used with the AD8349. The use of dual integrated DAC's such as the the AD9761 with specified ±0.02dB and ±0.004dB gain and offset matching characteristics ensures minimum error contribution (over temperature) from this portion of the signal chain.

The Local Oscillator is implemented using the ADF4360-2. The low-pass filter was designed using ADIsimPLL, for a channel spacing of 100kHz and an open-loop bandwidth chosen of 10kHz. The frequency range of the ADF4360-2 (1.8-2.15GHz) makes it ideally suited for implementation of a W-CDMA transceiver.

The LO ports of the AD8349 can be driven differentially from the complementary RFoutA and RFoutB outputs of the ADF4360-2. This gives a better performance than a single-ended LO driver, and eliminates the often necessary use of a balun to convert from a single-ended LO input to the more desireable differential LO inputs for the AD8349. The typical rms phase noise (100Hz-100kHz) of the LO in this configuration is 2.1 degrees.

The AD8349 accepts LO drive levels from -10 to 0dBm. The optimum LO power can be software programmed on the ADF4360-2, which allows levels from -12 to -3 dBm from each output.

The RF output is designed to drive a 50 Ω load, but must be AC-coupled as shown in Figure 8. If the I and Q inputs are driven in quadrature by 2V p-p signals, the resulting output power from the modulator will be around +2dBm.

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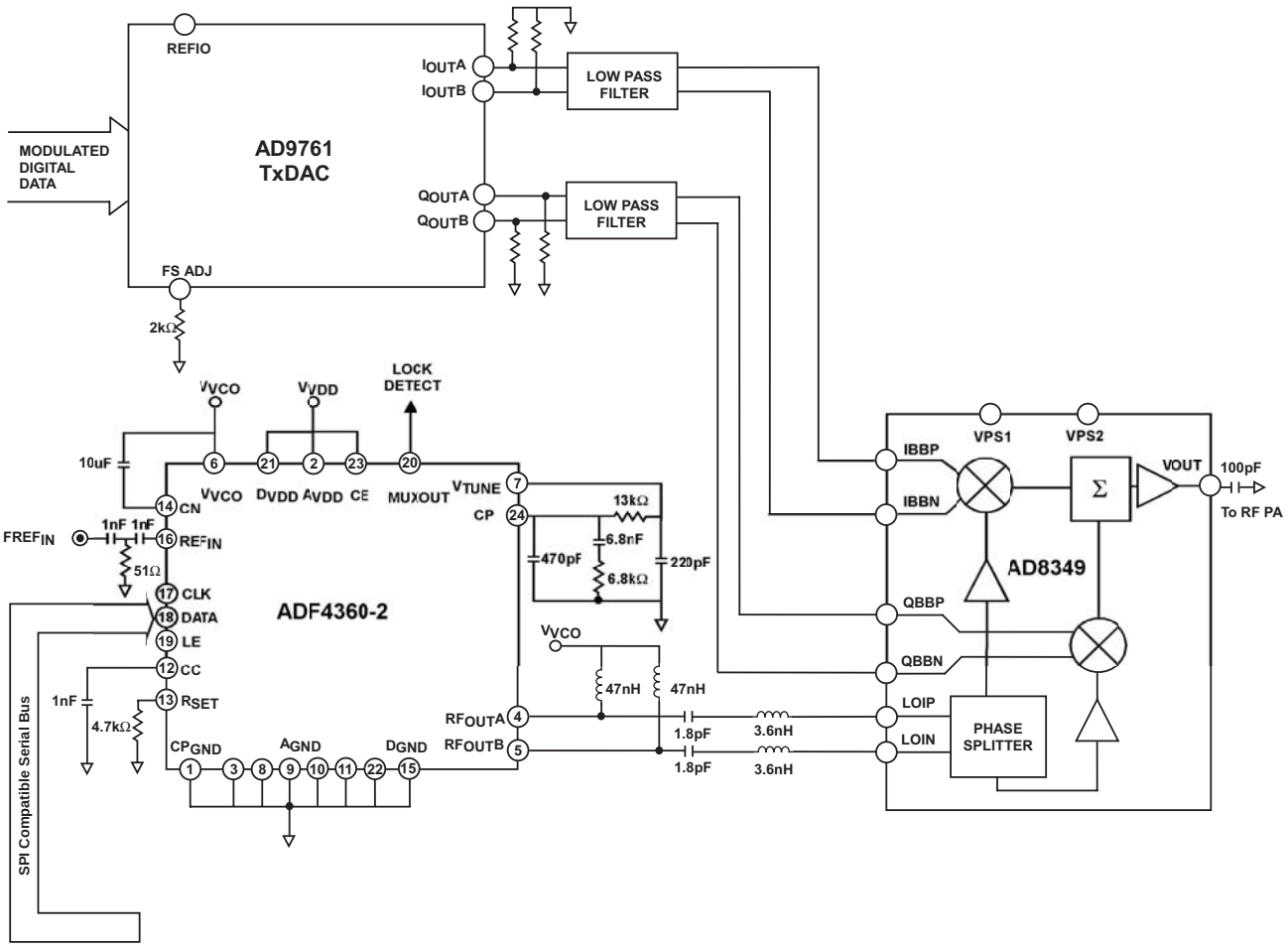

Figure 8. Direct Conversion Modulator

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FIXED FREQUENCY LO:

The following diagram shows the ADF4360-2 used as a fixed frequency LO at 2.0GHz. The low-pass filter was designed using ADIsimPLL, for a channel spacing of 8MHz and an open-loop bandwidth of 45kHz. 8MHz is the maximum PFD frequency of the ADF4360-2. Since using a larger PFD frequency allows us to use a smaller N. The In-band phase noise is reduced to as low as possible, -99dBc/Hz. The 40kHz bandwidth is chosen to be just greater than the point at which open-loop phase-noise of the VCO is -99dBc/Hz, thus giving the best possible Integrated noise. The typical rms phase noise (100Hz-100kHz) of the LO in this configuration is 0.3 degrees.

The reference frequency is from a 16MHz TCXO from Fox. Thus an R value of 2 is programmed. Taking account of the high PFD frequency, and the effect this has on the band select logic, the band select clock divider is enabled. In this case a value of 8 is chosen. A very simple pull-up resistor and DC blocking capacitor complete the RF output stage.

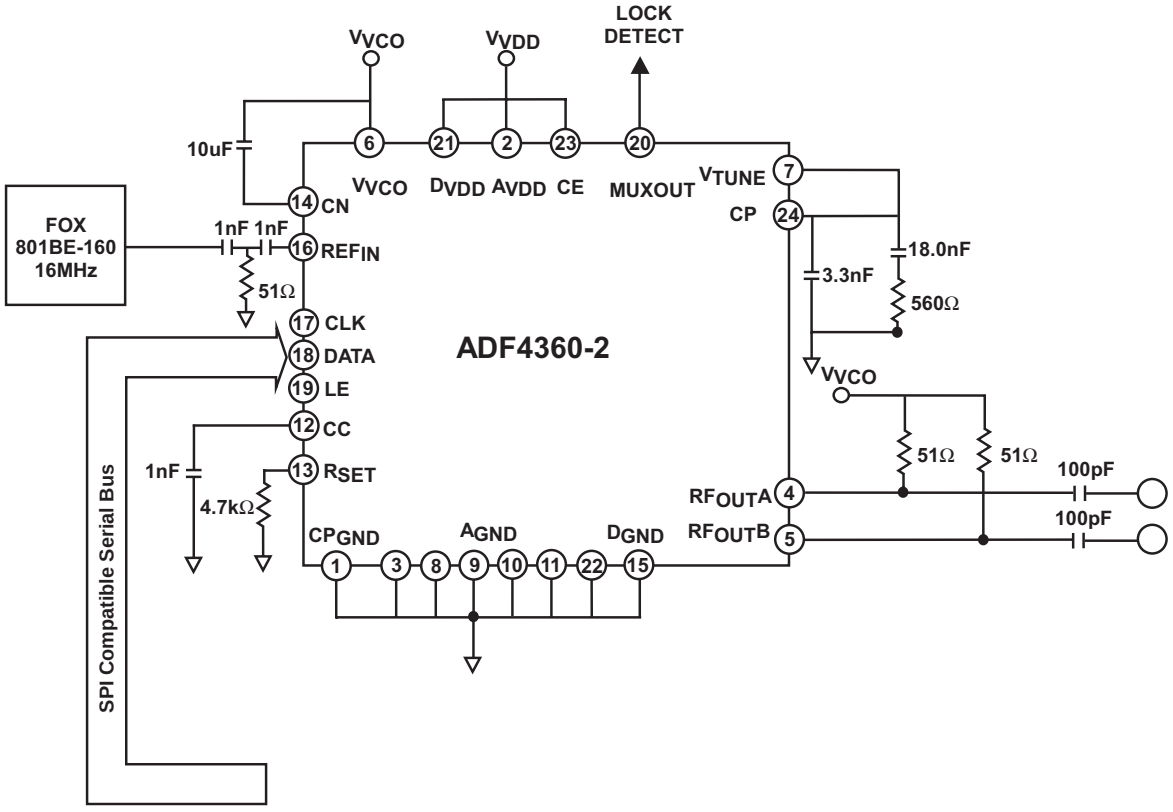

Figure 9. Single Frequency LO.

POWER UP.
After power-up, the part needs a three writes for normal operation. The correct sequence is to the R Counter latch, followed by the Control latch and finally the N Counter latch.

INTERFACING

The ADF4360 family has a simple SPI-compatible serial interface for writing to the device. CLK , DATA and LE control the data transfer. When LE goes high the 24 bits which have been clocked into the appropriate register on each rising edge of CLK will get transferred to the appropriate latch. See figure 1 for the Timing diagram and Table I for the Latch Truth Table.
The maximum allowable serial clock rate is 20MHz. This means the maximum update rate possible is 833kHz or one update every 1.2 microseconds. This is certainly more than adequate for systems that will have typical lock times in hundreds of microseconds.

ADuC812 Interface

Figure 9 shows the interface between the ADF4360 family and the ADuC812 microconverter. Since the ADuC812 is based on an 8051 core, this interface can be used with any 8051-based microcontroller. The microconverter is setup for SPI master mode with CPHA = 0. To initiate the operation, the I/O port driving LE is brought low. Each latch of the ADF4360 family is needs a 24-bit word. This is accomplished by writing three 8-bit bytes from the microconverter to the device. When the third byte has been written the LE input should be brought high to complete the transfer.

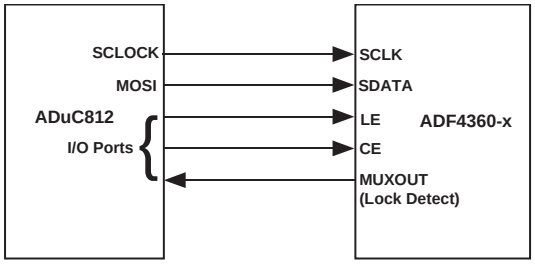

Figure 10. ADuC812 to ADF4360-x Interface

I/O port lines on the ADuC812 are also used to control powerdown (CE input) and to detect lock (MUXOUT configured as lock detect and polled by the port input). When operating in the mode described, the maximum SCLOCK rate of the ADuC812 is 4MHz. This means that the maximum rate at which the output frequency can be changed is 166kHz.

ADSP-2181 Interface

Figure 10 shows the interface between the ADF4360 family and the ADSP-21xx Digital Signal Processor. The ADF4360 family needs a 24-bit serial word for each latch write. The easiest way to accomplish this is using the ADSP -21xx family is to use the Autobuffered Transmit Mode of operation with Alternate Framing. This provides a means for transmitting an entire block of serial data before an interrupt is generated.

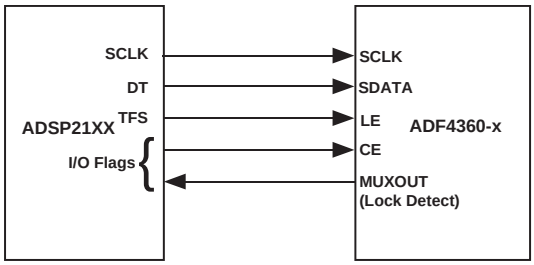

Figure 11. ADSP-21xx to ADF4360-x Interface

Set up the word length for 8 bits and use three memory locations for each 24-bit word. To program each 24-bit latch, store the 8-bit bytes, enable the Autobuffered mode and then write to the the transmit register of the DSP. This last operation initiates the autobuffer transfer.

PCB DESIGN GUIDELINES FOR CHIP SCALE PACKAGE

The lands on the chip scale package (CP-24) are rectangular. The printed circuit board pad for these should be 0.1mm longer then the package land length and 0.05mm wider than the package land width. The land should be centered on the pad. This will ensure that the solder joint size is maximised.

The bottom of the chip scale package has a central thermal pad. The thermal pad on the printed circuit board should be at least as large as this exposed pad. On the printed curcuit board, there should be a clearance of at least 0.25 mm between the thermal pad and the inner edges of the pad pattern. This will ensure that shorting is avoided.

Thermal vias may be used on the printed circuit board thermal pad to improve thermal performance of the package. If vias are used, they should be incorporated in the thermal pad at 1.2mm pitch grid. The via diameter should be between 0.3mm and 0.33mm and the via barrel should be plated with 1oz copper to plug the via.

The user should connect the printed circuit thermal pad to AGND. This is internally connected to AGND.

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OUTPUT MATCHING

There are a number of ways to match the output of the ADF4360-2 for optimum operation. The most basic of these is to use a 50Ohm resistor to Vvco. A DC bypass capacitor of 100pF is connected in series as shown below. Because the resistor is not frequency dependent, This provides a good broadband match. The output power in a circuit below gives typically -6dBm output power into a 50Ohm load.

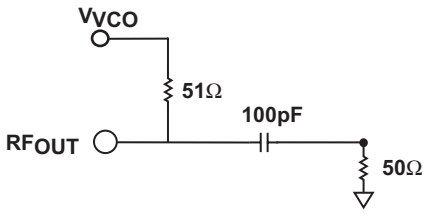


Figure 12. Simple ADF4360-2 Output Stage

A better solution is to use a shunt inductor (acting as an RF Choke) to Vvco, This gives a better match and hence more output power, Additionally a series inductor is added after the DC bypass capacitor to provide a resonant LC circuit. This tunes the oscillator output and provides approximately 10dB further rejection of the 2nd harmonic. The shunt inductor needs to be a relatively high value (>40nH). Experiments have shown that the following circuit provides an excellent match to 50Ohms over the operating range of the ADF4360-2. This gives approximately -2dBm output power across the frequency range of the ADF4360-2. Both single-ended architectures can be examined using the EVAL_ADF4360-2EB1 evaluation board.

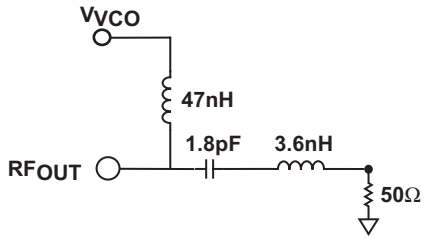


Figure 13. Optimum ADF4360-2 Output Stage

If the user does not need differential outputs available on the ADF4360, The user may either terminate the unused output, or combine both outputs using a balun. The circuit below shows how best to combine the outputs.

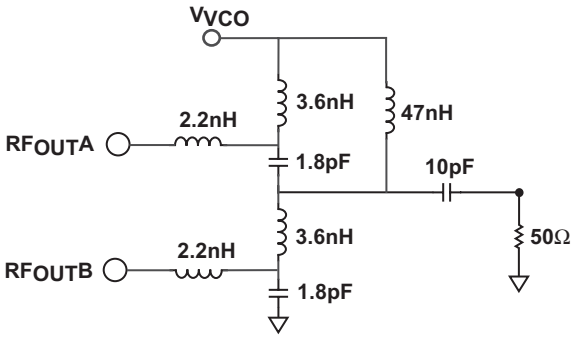
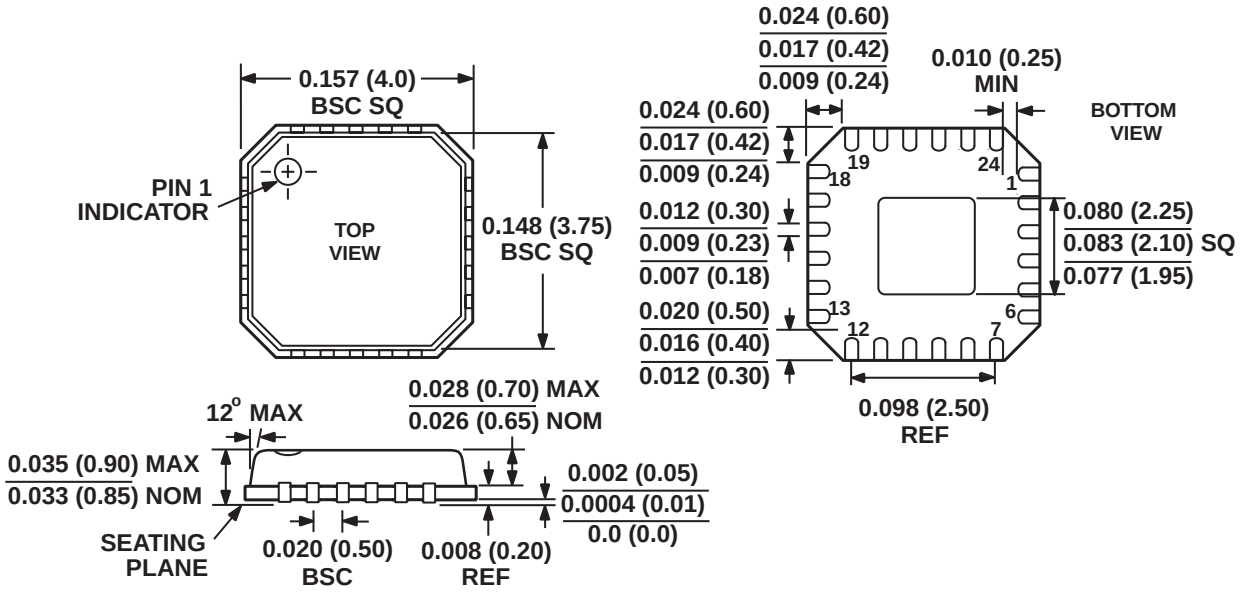


Figure 14. Balun for Combining ADF4360-2 RF Outputs

The above circuit is a lumped Lattice type LC balun. It is designed for a centre frequency of 2.0GHz and outputs +1.0dBm at this frequency. The series 2.2nH inductor is used to tune out any parasitic capacitance due to the board layout from each input, and the remainder of the circuit is used to shift the output of one RF input by +90°, and the second by -90°, thus combining the two. The action of the 3.6nH inductor and the 1.8pF capacitor accomplish this. The 47nH is used to provide an RF choke in order to feed the supply voltage and the 10pF capacitor provides the necessary DC block. To ensure good RF performance, Both of the above circuits were implemented with Coilcraft 0402/0603 Inductors, and AVX 0402 thin-film Capacitors.
Alternatively, instead of the LC balun shown above, both outputs may be combined using a 180 degrees rat-race coupler.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm)



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