

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74HC4049AP, TC74HC4049AF, TC74HC4049AFN, TC74HC4049AFT
TC74HC4050AP, TC74HC4050AF, TC74HC4050AFN, TC74HC4050AFT
TC74HC4049AP/AF/AFN/AFT HEX BUFFER / CONVERTER (INVERTING)
TC74HC4050AP/AF/AFN/AFT HEX BUFFER / CONVERTER

The TC74HC4049A and TC74HC4050A are high speed CMOS HEX BUFFERS fabricated with silicon gate C²MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The TC74HC4049A is an inverting buffer, while the TC74HC4050A is a non - inverting buffer. The internal circuits are composed of 3 - stages (HC4049A) or 2 - stages (HC4050A) of inverters, which provided high noise immunity and stable output.

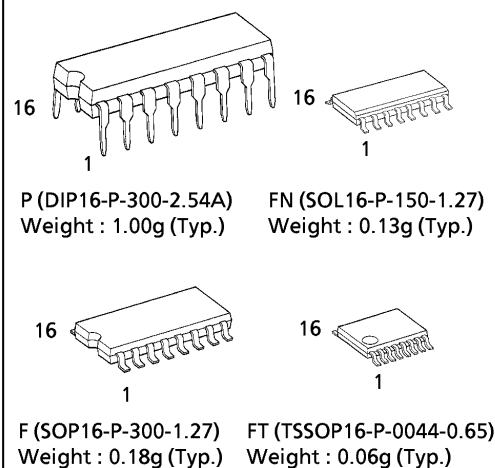
Input protection circuits are different from those of other high speed CMOS IC's. They eliminate the diodes on the V_{CC} side thus providing of logic - level conversion from high - level voltages up to 15V to low - level voltages.

They are useful for battery back up circuits, because input voltage can be applied on IC's which are not biased by V_{CC}.

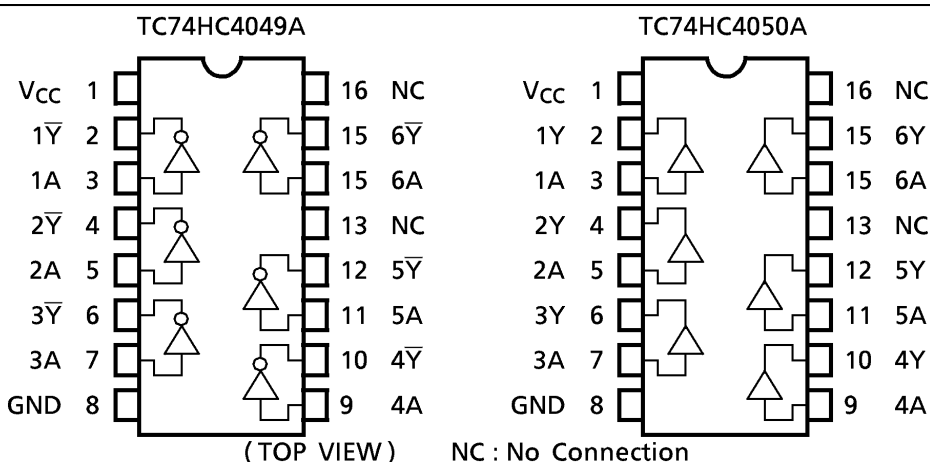
FEATURES :

- High Speed..... $t_{pd} = 9\text{ns}(\text{typ.})$ at $V_{CC} = 5\text{V}$
- Low Power Dissipation..... $I_{CC} = 1\mu\text{A}(\text{Max.})$ at $T_a = 25^\circ\text{C}$
- High Noise Immunity..... $V_{NIH} = V_{NIL} = 28\% V_{CC} (\text{Min.})$
- Output Drive Capability.....15 LSTTL Loads
- Symmetrical Output Impedance... $|I_{OH}| = I_{OL} = 6\text{mA} (\text{Min.})$
- Balanced Propagation Delays..... $t_{pLH} \approx t_{pHL}$
- Wide Operating Voltage Range.... $V_{CC} (\text{opr.}) = 2\text{V} \sim 6\text{V}$
- Pin and Function Compatible with 4049B / 4050B

(Note) The JEDEC SOP (FN) is not available in Japan.

**TRUTH TABLE**

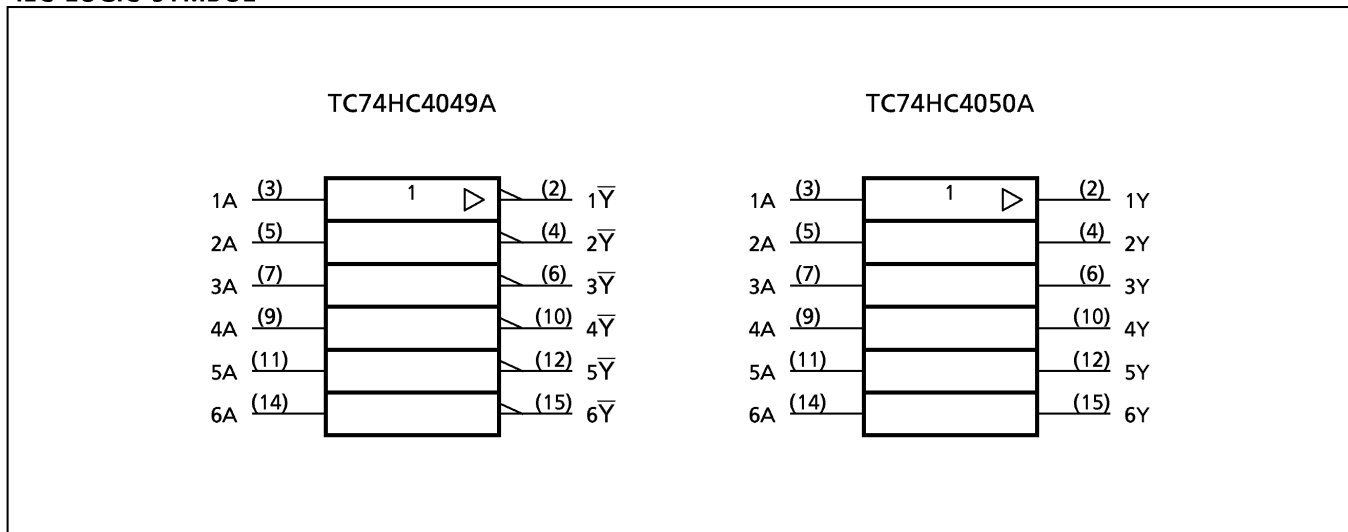
A	$\bar{Y}$ (4049A)	Y (4050A)
L	H	L
H	L	H

PIN ASSIGNMENT

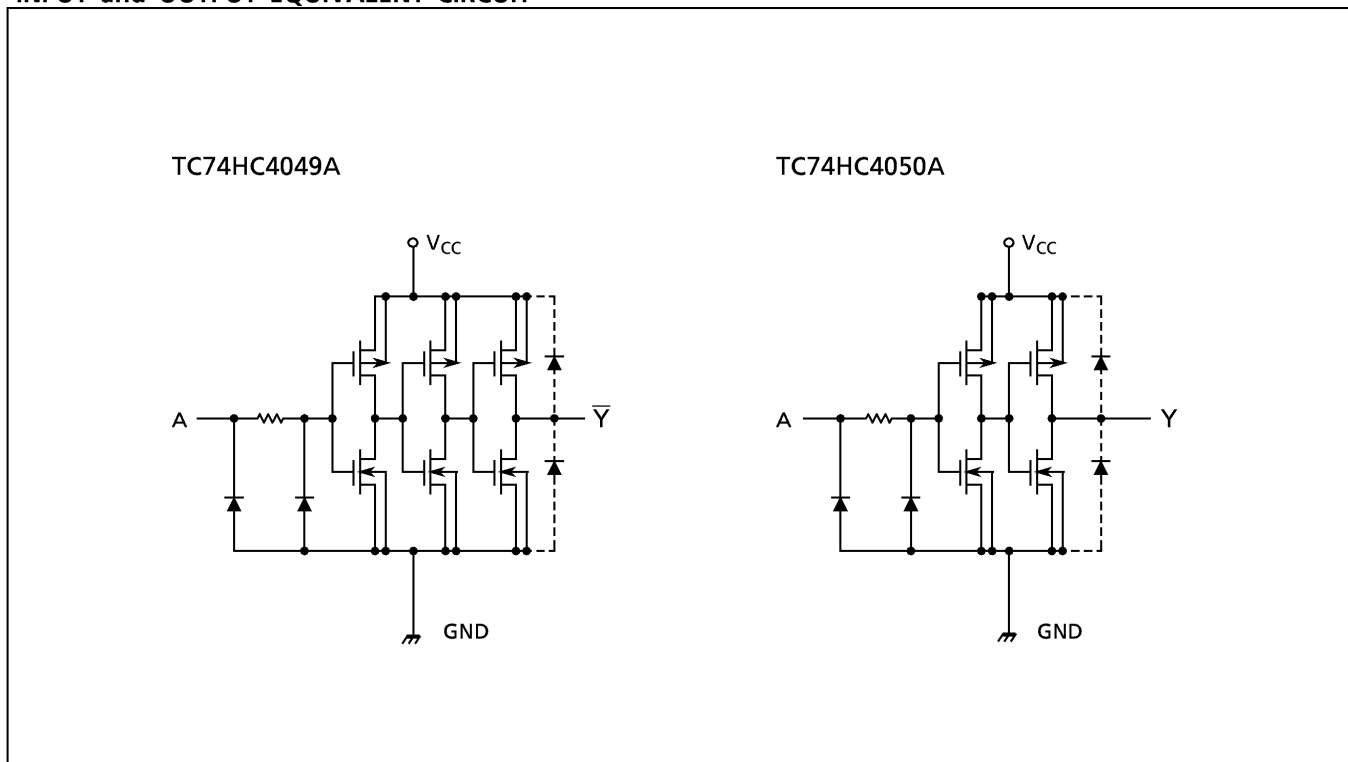
961001EBA2

● TOSHIBA is continually working to improve the quality and the reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to observe standards of safety, and to avoid situations in which a malfunction or failure of a TOSHIBA product could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent products specifications. Also, please keep in mind the precautions and conditions set forth in the TOSHIBA Semiconductor Reliability Handbook.

IEC LOGIC SYMBOL



INPUT and OUTPUT EQUIVALENT CIRCUIT



961001EBA2'

- The products described in this document are subject to foreign exchange and foreign trade control laws.
- The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA CORPORATION for any infringements of intellectual property or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any intellectual property or other rights of TOSHIBA CORPORATION or others.
- The information contained herein is subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim 18^*$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	-20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 35	mA
DC V_{CC} /Ground Current	I_{CC}	± 75	mA
Power Dissipation	P_D	500(DIP)**/180(SOP,TSSOP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	$^{\circ}\text{C}$

Note) * DC input voltage (V_{IN}) specified is measured to GND and is not related to V_{CC} .

Recommended operating range is 0V to 15V and it is possible to convert logic-levels from 15V to 5V or 5V to 2V.

** 500mW in the range of $T_a = -40^{\circ}\text{C} \sim 65^{\circ}\text{C}$. From $T_a = 65^{\circ}\text{C}$ to 85°C a derating factor of $-10\text{mW}/^{\circ}\text{C}$ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2~6	V
Input Voltage	V_{IN}	0~15	V
Output Voltage	V_{OUT}	0~ V_{CC}	V
Operating Temperature	T_{opr}	$-40 \sim 85$	$^{\circ}\text{C}$
Input Rise and Fall Time	t_r, t_f	0~1000 ($V_{CC} = 2.0\text{V}$) 0~500 ($V_{CC} = 4.5\text{V}$) 0~400 ($V_{CC} = 6.0\text{V}$)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	$T_a = 25^{\circ}\text{C}$			$T_a = -40 \sim 85^{\circ}\text{C}$		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}		2.0 4.5 6.0	1.50 3.15 4.20	— — —	— — —	1.50 3.15 4.20	— — —	V
Low - Level Input Voltage	V_{IL}		2.0 4.5 6.0	— — —	— — —	0.50 1.35 1.80	— — —	0.50 1.35 1.80	V
High - Level Output Voltage	V_{OH}	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -20\mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	1.9 4.4 5.9	— — —	V
				4.5 6.0	4.18 5.68	4.31 5.80	4.13 5.63	— —	
Low - Level Output Voltage	V_{OL}	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 20\mu\text{A}$	2.0 4.5 6.0	— — —	0.0 0.0 0.0	— — —	0.1 0.1 0.1	V
				4.5 6.0	— —	0.17 0.18	— —	0.33 0.33	
Input Leakage Current	I_{IN}	$V_{IN} = V_{CC} \text{ or GND}$	6.0	—	—	± 0.1	—	± 1.0	μA
		$V_{IN} = 15\text{V}$	6.0	—	—	± 0.5	—	± 5.0	
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC} \text{ or GND}$	6.0	—	—	1.0	—	10.0	

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	CL (pF)	V _{CC} (V)	Ta = 25°C			Ta = -40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		50	2.0	—	25	60	—	75	ns
				4.5	—	6	12	—	15	
				6.0	—	5	10	—	13	
Propagation Delay Time	t_{pLH} t_{pHL}		50	2.0	—	30	75	—	95	
				4.5	—	9	15	—	19	
				6.0	—	8	13	—	16	
			150	2.0	—	45	100	—	145	
				4.5	—	14	20	—	29	
				6.0	—	12	17	—	25	
Input Capacitance	C _{IN}				—	5	10	—	10	pF
Power Dissipation Capacitance	C _{PD} (1)				—	26	—	—	—	

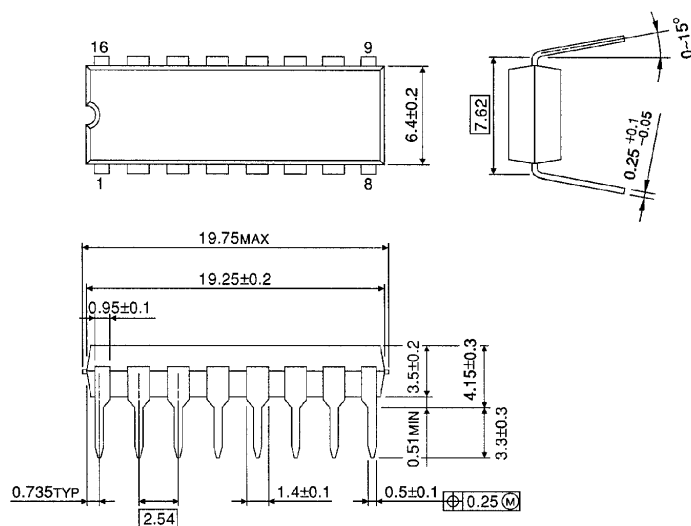
Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{\text{CC}}(\text{opr}) = C_{\text{PD}} \cdot V_{\text{CC}} \cdot f_{\text{IN}} + I_{\text{CC}}/6 \text{ (per Gate)}$$

DIP 16PIN OUTLINE DRAWING (DIP16-P-300-2.54A)

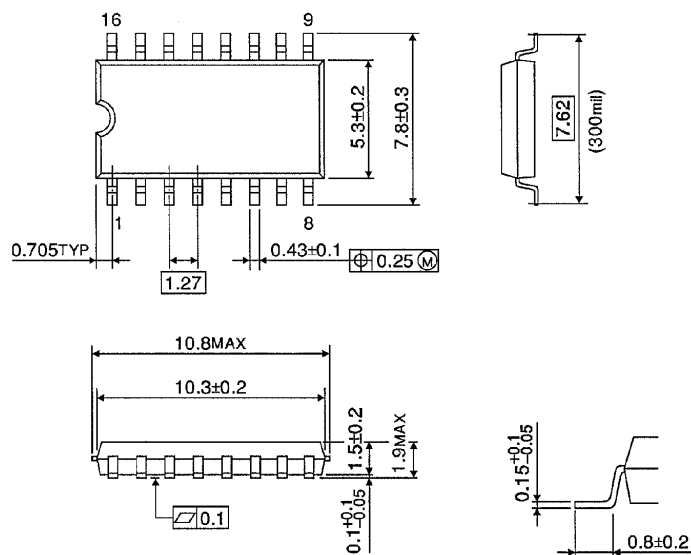
Unit in mm



Weight : 1.00g (Typ.)

SOP 16PIN (200mil BODY) OUTLINE DRAWING (SOP16-P-300-1.27)

Unit in mm



Weight : 0.18g (Typ.)

Unit in mm

Technical drawing of the 16-pin connector showing top, side, and detail views with dimensions.

Top View Dimensions:

- Pin 16 to Pin 9: 3.9 ± 0.1
- Pin 9 to Pin 8: 6.0 ± 0.2
- Pin 1 to Pin 8: 0.505 TYP
- Pin 8 to Pin 1: 0.42 ± 0.07
- Pin 1 to Pin 8: 1.27
- Pin 8 to Pin 1: 0.25 (M)

Side View Dimensions:

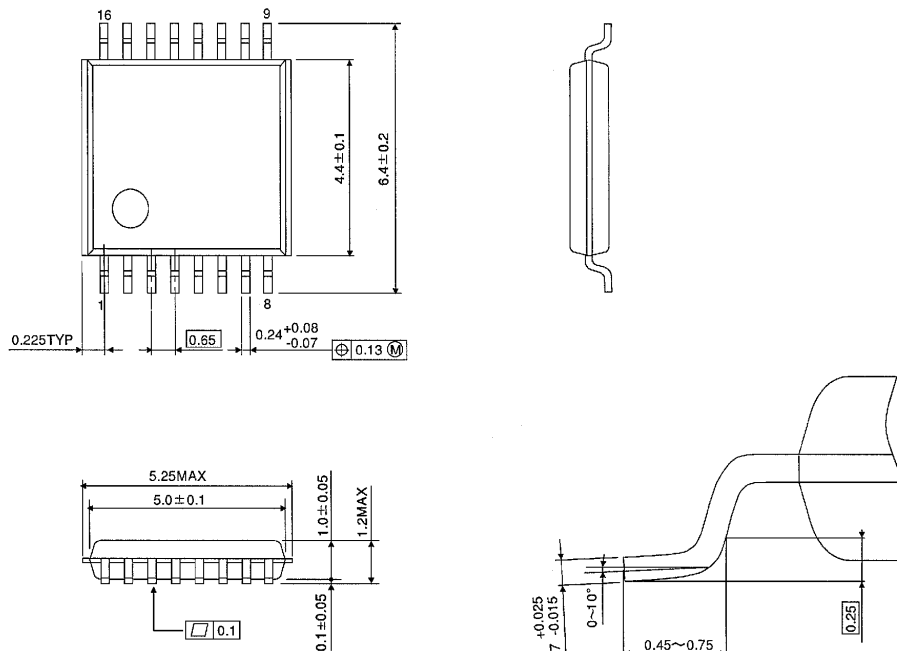
- Pin 16 to Pin 9: 9.9 ± 0.1
- Pin 9 to Pin 8: 1.375 ± 0.2
- Pin 8 to Pin 1: 1.75 MAX
- Pin 1 to Pin 8: 0.175 ± 0.075
- Pin 8 to Pin 1: 0.1

Detail View Dimensions:

- Pin 16 to Pin 9: $0.15^{+0.1}_{-0.05}$
- Pin 9 to Pin 8: 0.7 ± 0.3
- Pin 8 to Pin 1: 45°

Weight : 0.13g (Typ.)

Unit in mm



Weight : 0.06g (Typ.)