TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74HC4538AP, TC74HC4538AF, TC74HC4538AFN, TC74HC4538AFT

DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR

The TC74HC4538A is a high speed CMOS MONOSTABLE MULTIVIBRATOR fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

There are two trigger inputs, A input (Positive edge input), and $\overline{B}$ input (Negative edge input). These inputs are valid for a slow rise/fall time signal (tr = tf = 1sec.) as they are schmitt trigger inputs.

After triggering, the output stays in a MONOSTABLE state for the time period determined by the external resistor and capacitor (Rx, Cx). A low level at $\overline{CD}$ input breaks this STABLE STATE. In the MONOSTABLE state, if a new trigger is applied, it makes the MONOSTABLE period longer (retrigger mode).

Limitations for Cx and Rx are as follows:

External capacitor Cx ····· No limitation

External resistor Rx ····· V_{CC} = 2.0V more than 5kΩ

$V_{CC} \geq$ 3.0V more than 1kΩ

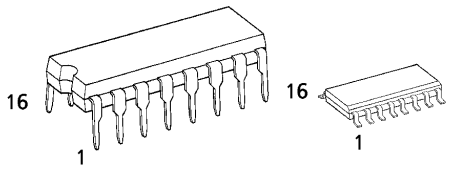
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· t_{pd} = 25ns (typ.) at V_{CC} = 5V
- Low Power Dissipation
  - Stand by State ····· I_{CC} = 4μA(Max.) at Ta = 25°C
  - Active State ····· I_{CC} = 300μA(Max.) at Ta = 25°C
- High Noise Immunity ····· $V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}| = I_{OL}$ = 4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \simeq t_{pHL}$
- Wide Operating Voltage Range ···· V_{CC} (opr.) = 2V ~ 6V
- Pin and Function Compatible with 4538B

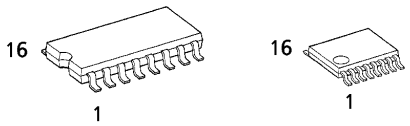
Note: In the case of using only one circuit, $\overline{CD}$ should be tied to GND, $T1 \cdot T2 \cdot Q \cdot \overline{Q}$ should be tied to OPEN, the other inputs should be tied to V_{CC} or GND.

(Note) The JEDEC SOP (FN) is not available in Japan.



P (DIP16-P-300-2.54A) Weight : 1.00g (Typ.)

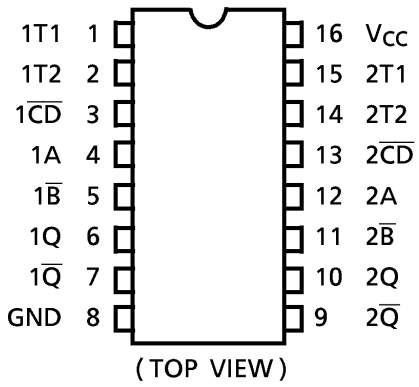
FN (SOL16-P-150-1.27) Weight : 0.13g (Typ.)



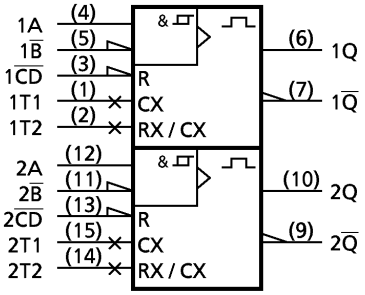
F (SOP16-P-300-1.27) Weight : 0.18g (Typ.)

FT (TSSOP16-P-0044-0.65) Weight : 0.06g (Typ.)

PIN ASSIGNMENT



IEC LOGIC SYMBOL



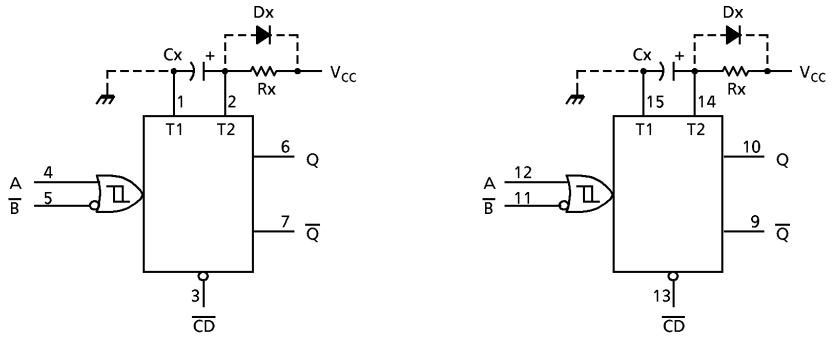
980508EBA2

TRUTH TABLE

INPUT			OUTPUT		NOTE
A	$\overline{B}$	$\overline{CD}$	Q	$\overline{Q}$	
↑	H	H	⊓	⊔	OUTPUT ENABLE
X	L	H	L	H	INHIBIT
H	X	H	L	H	INHIBIT
L	↓	H	⊓	⊔	OUTPUT ENABLE
X	X	L	L	H	RESET

X : Don't Care

BLOCK DIAGRAM



Notes : (1) Cx, Rx, Dx are external.
Capacitor, Resistor, and Diode, respectively.

(2) External clamping diode, Dx

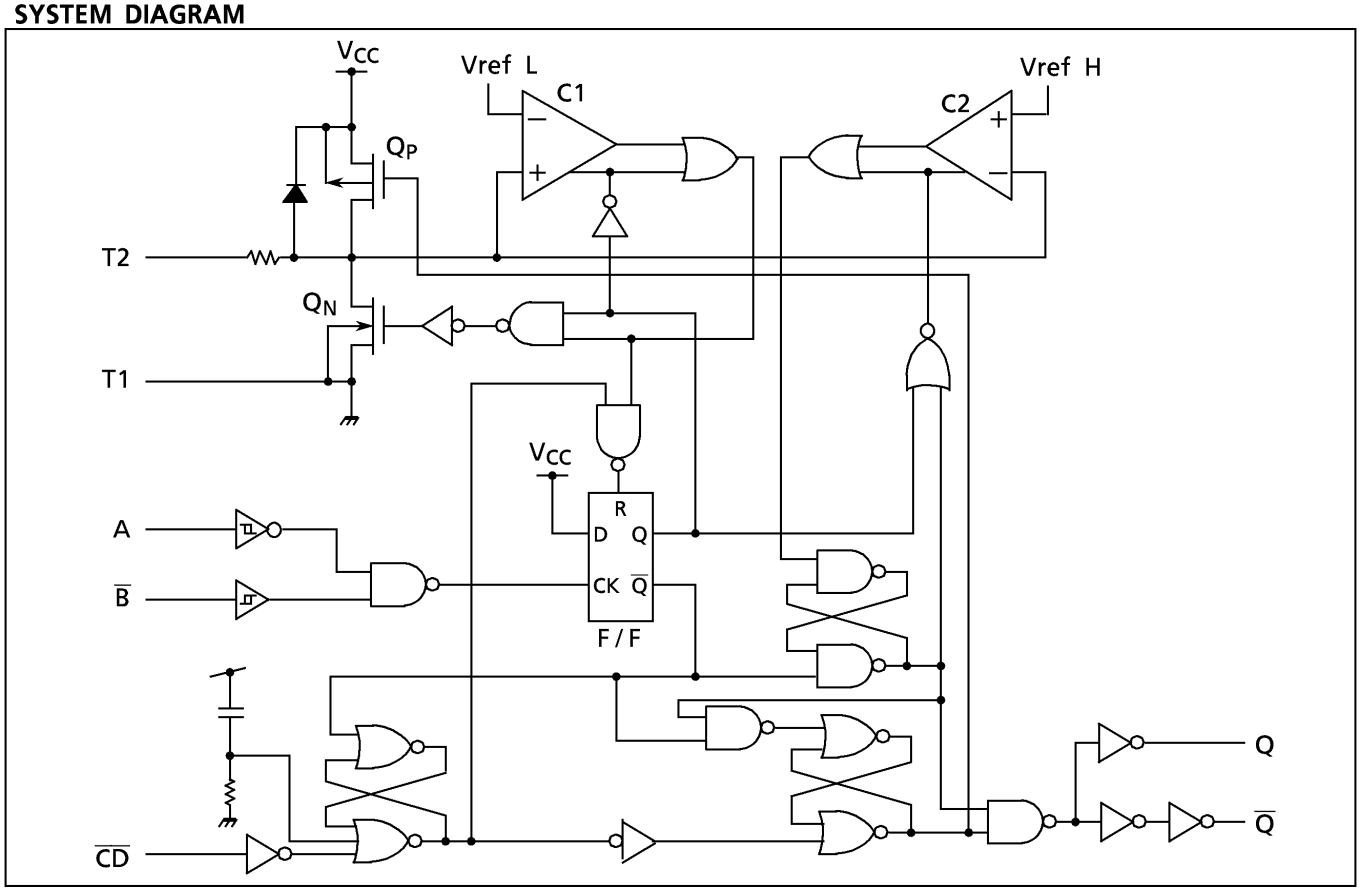
The external capacitor is charged to V_{CC} level in the wait state, i.e. when no trigger is applied. Supply voltage is turned off and Cx is discharged mainly through the internal (parasitic) diode. If Cx is sufficiently large and V_{CC} drops rapidly, there will be some possibility of damaging the IC by rush current or latch-up. If the capacitance of the supply voltage filter is large enough and V_{CC} drops slowly, the rush current is automatically limited and damage to the IC is avoided.
The maximum value of forward current through the parasitic diode is ±20mA.
In the case of a large Cx, the limitation of fall time of the supply voltage is determined as follows :

$$t_f \geq (V_{CC} - 0.7)\, Cx / 20mA$$

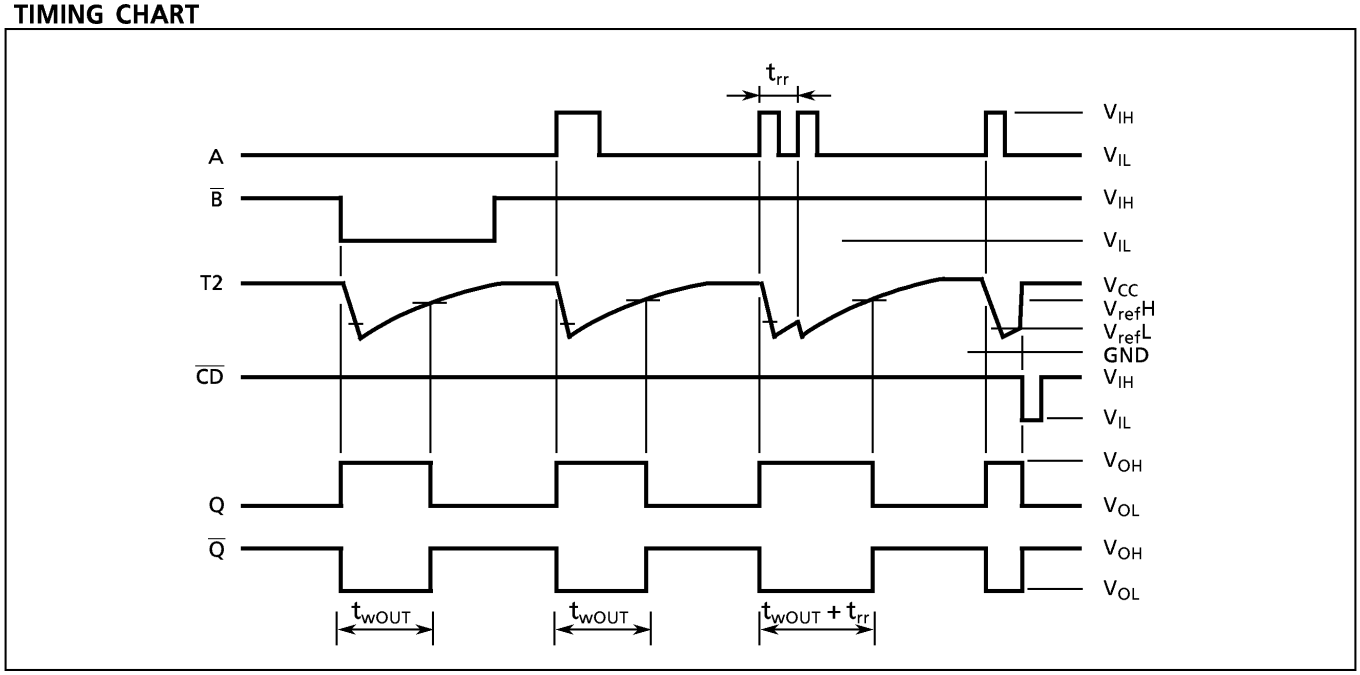
(t_f is the time from the voltage supply turning off to the level of supply voltage reaching 0.4 V_{CC}.)

In the care of a system that does not satisfy the above condition, an external clamping diode is needed to protect the IC from rush current.

SYSTEM DIAGRAM



TIMING CHART



FUNCTIONAL DESCRIPTION

(1)Stand-by State

The external capacitor is fully charge to V_{CC} in the stand-by state. That means, before triggering, Q_P and Q_N transistors which are connected to the T2 node are in the off state. Two comparators that relate to the timing of the output pulse, and two reference voltage supplies stop their operation. The total supply current is only leakage current.

(2)Trigger operation

Trigger operation is effective in either of the following two cases. One is the condition where the A input is low, and the $\overline{B}$ input has a falling signal. The other, where the $\overline{B}$ input is high, and the A input has a rising signal.
After trigger becomes effective, comparators C1 and C2 start operating, and Q_N is turned on. The external capacitor discharges through Q_N. The voltage level at the T2 node drops. If the T2 voltage level falls to the internal reference voltage Vref L, the output of C1 becomes low. The flip-flop is then reset and Q_N turns off. At that moment C1 stops but C2 continues operating.
After Q_N turns off, the voltage at T2 start rising at a rate determined by the time constant of external capacitor Cx and resistor Rx.
After the triggering, output Q becomes high, following some delay time of the internal F/F and gates. It stays high even if the voltage of T2 changes from falling to rising. When T2 reaches the internal reference voltage Vref H, the output of C2 becomes low, the output Q goes low and C2 stops its operation. That means, after triggering, when the voltage level of T2 reaches Vref H, the IC returns to its MONOSTABLE state.
In the case of large value of Cx and Rx, and ignoring the discharge time of the capacitor and internal delays of the IC, the width of the output pulse, (tw_{OUT}), is as follows :

$$tw_{OUT} = 0.70 \cdot Cx \cdot Rx$$

(3)Retrigger operation

When anoter new trigger is applied to input A or $\overline{B}$ while in the MONOSTABLE state, it is effective only if the IC is chaging Cx. The voltage level of T2 then falls to Vref L level again.
Therefore the Q output stays high if the next trigger comes in before the time period set by Cx and Rx.
If the 2nd trigger is very close to previous trigger, such as application during the dischagre cycle, the 2nd trigger will not be effective.
The minimum time for effective 2nd trigger, trr (Min), depends on Vcc and Cx.

(4)Reset operation

In normal operation, $\overline{CD}$ input is held high. If $\overline{CD}$ is low, a trigger has no effect because the Q output is held low and the trigger control F/F is reset. Also Q_P turns on and Cx is charged rapidly to V_{CC}.
This means if $\overline{CD}$ input is set low, the IC goes into a wait state.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7	V
DC Input Voltage	V_{IN}	−0.5~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP / TSSOP)	mW
Storage Temperature	T_{stg}	−65~150	°C

*500mW in the range of Ta= −40°C~65°C. From Ta=65°C to 85 °C a derating factor of −10mW/ °C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2~6	V
Input Voltage	V_{IN}	0~V_{CC}	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time ($\overline{CD}$ Only)	t_r, t_f	0~1000 (V_{CC}=2.0V) 0~ 500 (V_{CC}=4.5V) 0~ 400 (V_{CC}=6.0V)	ns
External Capacitor	Cx	No Limitation *	F
External Resistor	Rx	≥5k * (V_{CC}=2.0V) ≥1k * (V_{CC} ≥3.0V)	Ω

* The maximum allowable values of Cx and Rx are a function of leakage of capacitor Cx, the leakage of TC74HC4538A, and leakage due to board layout and surface resistance.
Susceptibility to externally induced noise signals may occur for Rx>1MΩ.

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C MIN.	Ta = 25°C TYP.	Ta = 25°C MAX.	Ta = −40~85°C MIN.	Ta = −40~85°C MAX.	UNIT
High - Level Input Voltage	V_{IH}			2.0 4.5 6.0	1.50 3.15 4.20	— — —	— — —	1.50 3.15 4.20	— — —	V
Low - Level Input Voltage	V_{IL}			2.0 4.5 6.0	— — —	— — —	0.50 1.35 1.80	— — —	0.50 1.35 1.80	V
High - Level Output Voltage (Q, $\overline{Q}$)	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	— — —	1.9 4.4 5.9	— — —	V
			I_{OH} = −4 mA I_{OH} = −5.2mA	4.5 6.0	4.18 5.68	4.31 5.80	— —	4.13 5.63	— —	
Low - Level Output Voltage (Q, $\overline{Q}$)	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20μA	2.0 4.5 6.0	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	0.1 0.1 0.1	V
			I_{OL} = 4 mA I_{OL} = 5.2mA	4.5 6.0	— —	0.17 0.18	0.26 0.26	— —	0.33 0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	—	—	±0.1	—	±1.0	μA
T2 Terminal Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	—	—	±0.5	—	±5.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	—	—	4.0	—	40.0	
Active - State * Supply Current	I_{CC}	V_{IN} = V_{CC} or GND T2 ext = 0.5 V_{CC}		2.0 4.5 6.0	— — —	40 200 300	120 300 600	— — —	160 400 800	μA

∗ : per circuit

TIMING REQUIREMENTS (Input $t_r = t_f$ = 6ns)

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C TYP.	Ta = 25°C LIMIT	Ta = −40~85°C LIMIT	UNIT
Minimum Pulse Width (A, $\overline{B}$)	$t_{W(L)}$ $t_{W(H)}$			2.0 4.5 6.0	— — —	75 15 13	95 19 16	ns
Minimum Clear Width ($\overline{CD}$)	$t_{W(L)}$			2.0 4.5 6.0	— — —	75 15 13	95 19 16	
Minimum Clear Removal Time	t_{rem}			2.0 4.5 6.0	— — —	15 5 5	15 5 5	
Minimum Retrigger Time	t_{rr}	Rx = 1kΩ Cx = 100pF		2.0 4.5 6.0	380 92 72	— — —	— — —	
		Rx = 1kΩ Cx = 0.01μF		2.0 4.5 6.0	6.0 1.4 1.2	— — —	— — —	μs

AC ELECTRICAL CHARACTERISTICS (C_L = 15pF, V_{CC} = 5V, Ta = 25°C, Input $t_r = t_f$ = 6ns)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		—	6	12	ns
Propagation Delay Time (A, $\overline{B}$ — Q, $\overline{Q}$)	t_{pLH} t_{pHL}		—	25	44	
Propagation Delay Time ($\overline{CD}$ — Q, $\overline{Q}$)	t_{pLH} t_{pHL}		—	21	34	

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C			Ta = −40~85°C		UNIT
			V_{CC} (V)	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0 4.5 6.0	— — —	30 8 7	75 15 13	— — —	95 19 16	ns
Propagation Delay Time (A, $\overline{B}$ — Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0 4.5 6.0	— — —	120 30 25	250 50 43	— — —	315 63 54	
Propagation Delay Time ($\overline{CD}$ — Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0 4.5 6.0	— — —	100 25 20	195 39 33	— — —	245 49 42	
Output Pulse Width	tw_{OUT}	Cx = 0F Rx = 5kΩ (V_{CC} = 2V) Rx = 1kΩ (V_{CC} = 4.5V,6V)	2.0 4.5 6.0	— — —	540 180 150	1200 250 200	— — —	1500 320 260	ns
		Cx = 0.01μF Rx = 10kΩ	2.0 4.5 6.0	70 69 69	83 77 77	96 85 85	70 69 69	96 85 85	μs
		Cx = 0.1μF Rx = 10kΩ	2.0 4.5 6.0	0.67 0.67 0.67	0.75 0.73 0.73	0.83 0.77 0.77	0.67 0.67 0.67	0.83 0.77 0.77	ms
Output Pulse Width Error Between Circuits (In same Package)	Δtw_{OUT}			—	±1	—	—	—	%
Input Capacitance	C_{IN}			—	5	10	—	10	pF
Power Dissipation Capacitance	C_{PD}	Note (1)		—	70	—	—	—	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

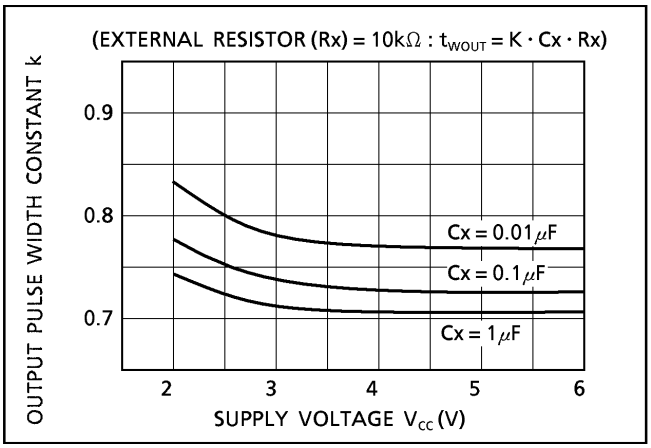
Average operating current can be obtained by the equation :

$I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}' \cdot Duty / 100 + I_{CC} / 2$ (per Circuit)

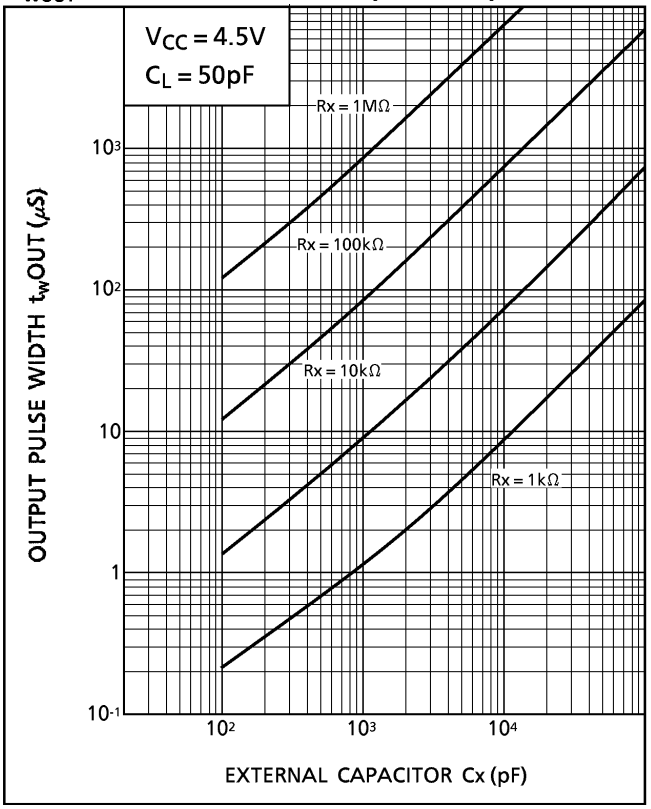
(I_{CC}' : Active Supply Current)

(Duty : %)

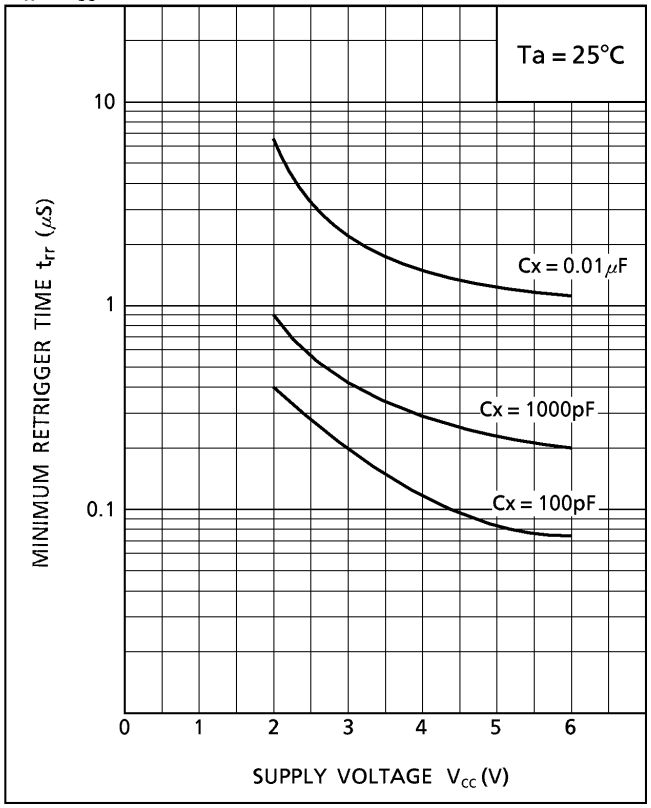
OUTPUT PULSE WIDTH CONSTANT K- SUPPLY VOLTAGE (TYPICAL)



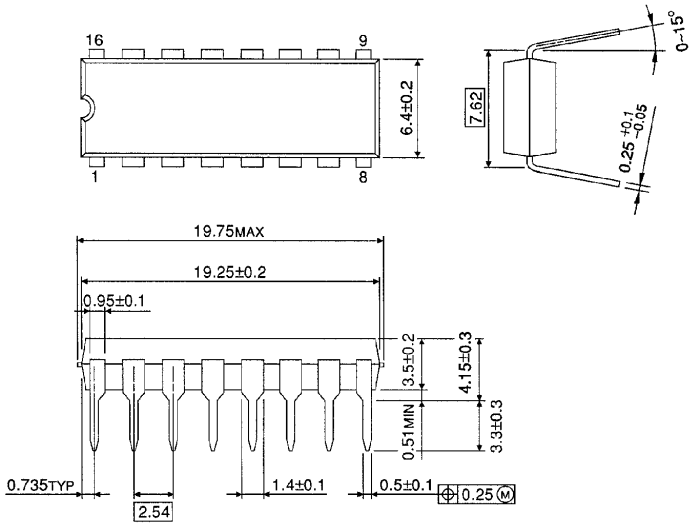
t_{WOUT} - Cx CHARACTERISTICS (TYPICAL)



t_{rr} - V_{CC} CHARACTERISTICS (TYPICAL)

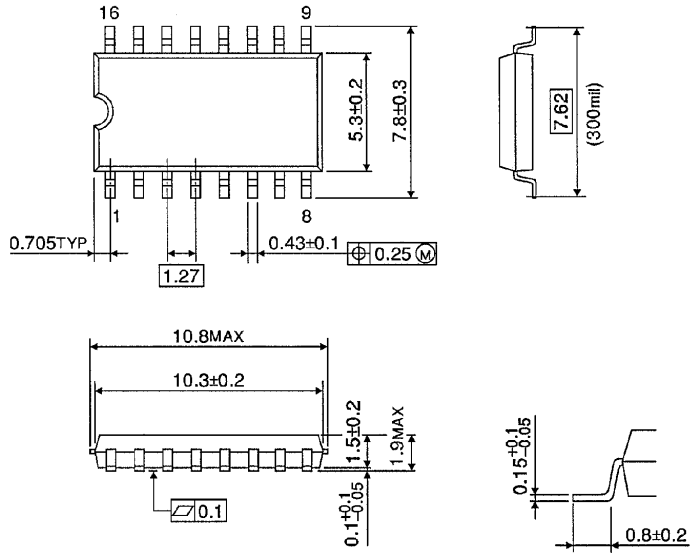


DIP 16PIN OUTLINE DRAWING (DIP16-P-300-2.54A) Unit in mm



Weight : 1.00g (Typ.)

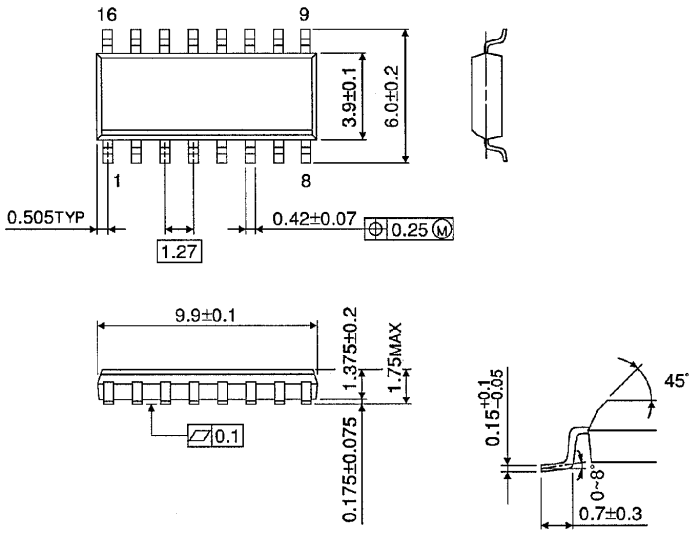
SOP 16PIN (200mil BODY) OUTLINE DRAWING (SOP16-P-300-1.27) Unit in mm



Weight : 0.18g (Typ.)

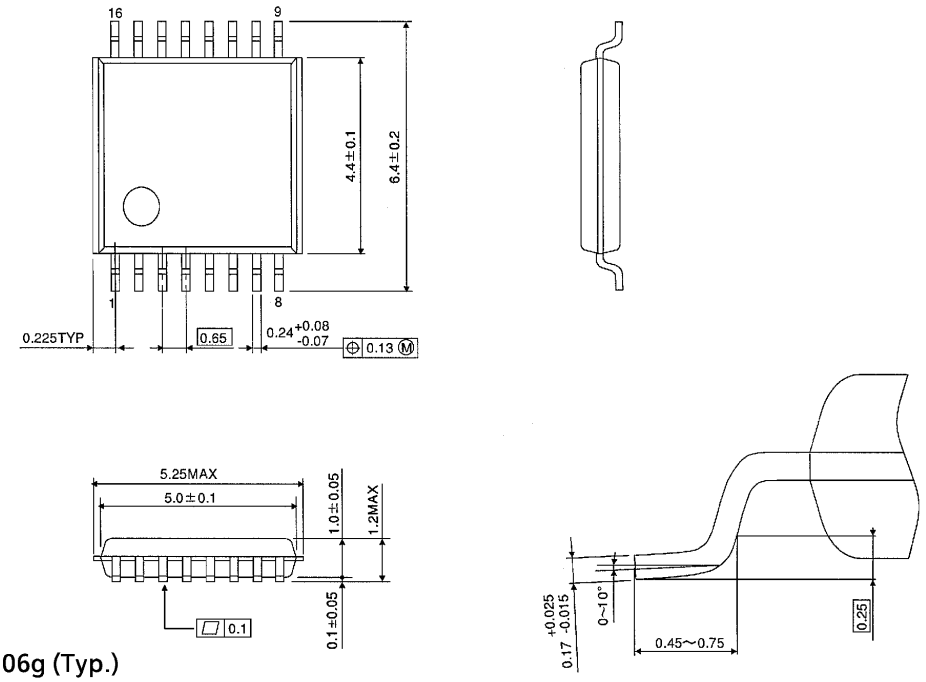
SOP 16PIN (150mil BODY) OUTLINE DRAWING (SOL16-P-150 -1.27) Unit in mm

(Note) This package is not available in Japan.



Weight : 0.13g (Typ.)

TSSOP 16PIN OUTLINE DRAWING (TSSOP16-P-0044-0.65) Unit in mm



Weight : 0.06g (Typ.)