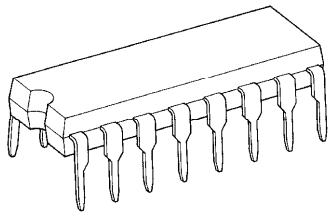
TOSHIBA DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC9216P, TC9217P, TC9217F

HIGH SPEED PLL FOR DTS

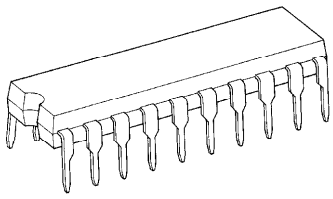
TC9216P, TC9217P, TC9217F are a high speed PLL-LSI with built-in 2 modulus prescaler. Each function is controlled through 3 serial bus lines and high performance digital tuning system can be constituted.

TC9216P



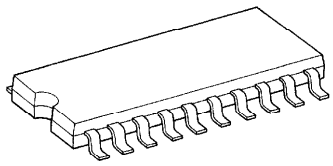
DIP16-P-300-2.54A

TC9217P



DIP20-P-300-2.54A

TC9217F



SOP20-P-300-1.27

Weight
DIP16-P-300-2.54A : 1.0g (Typ.)
DIP20-P-300-2.54A : 1.4g (Typ.)
SOP20-P-300-1.27 : 0.48g (Typ.)

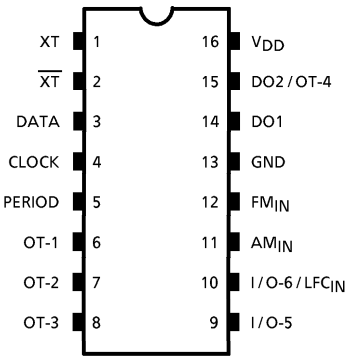
FEATURES

- Suitable for DTS of Hi-Fi tuner and car stereo
- Built-in prescaler, and it can operate 30~140MHz (2 modulus type) at FM band and 0.5~40MHz (2 modulus type or direct frequency dividing type) at AM band.
- Built-in 16bit programmable counter, two parallel outputs phase comparator, crystal oscillator and reference counter.
- Crystal resonator can be used 4.5MHz or 7.2MHz.
- 15 kinds of reference frequency can be selected. (when crystal is used 4.5MHz) (Ref = 0.5k, 1k, 2.5k, 3k, 3.125k, 3.90625k, 5k, 6.25k, 7.8125k, 9k, 10k, 12.5k, 25k, 50k, 100kHz)
- Frequency measurement (HFC_{IN}, LFC_{IN}) of intermediate frequency etc. and periodic measurement (SC_{IN}) of low frequency pilot signal etc. are possible by built-in 16bit universal type frequency counter.
  (Note : TC9216P does not have periodic measurement function.)
- Built-in abundant general purpose input / output terminal and usable for control radio circuit part.
- All of function controls are performed through 3 serial bus lines.
- Operating voltage range : $V_{DD} = 5.0 \pm 0.5V$, and it is CMOS structure.
- Package is DIP-16 pin (TC9216P) and DIP-20 pin (TC9217P) and SOP-20 pin (TC9217F).

980508EBA2

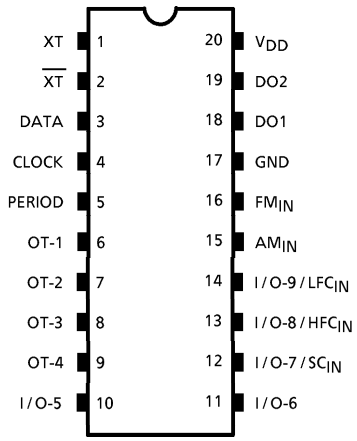
PIN CONNECTION

TC9216P



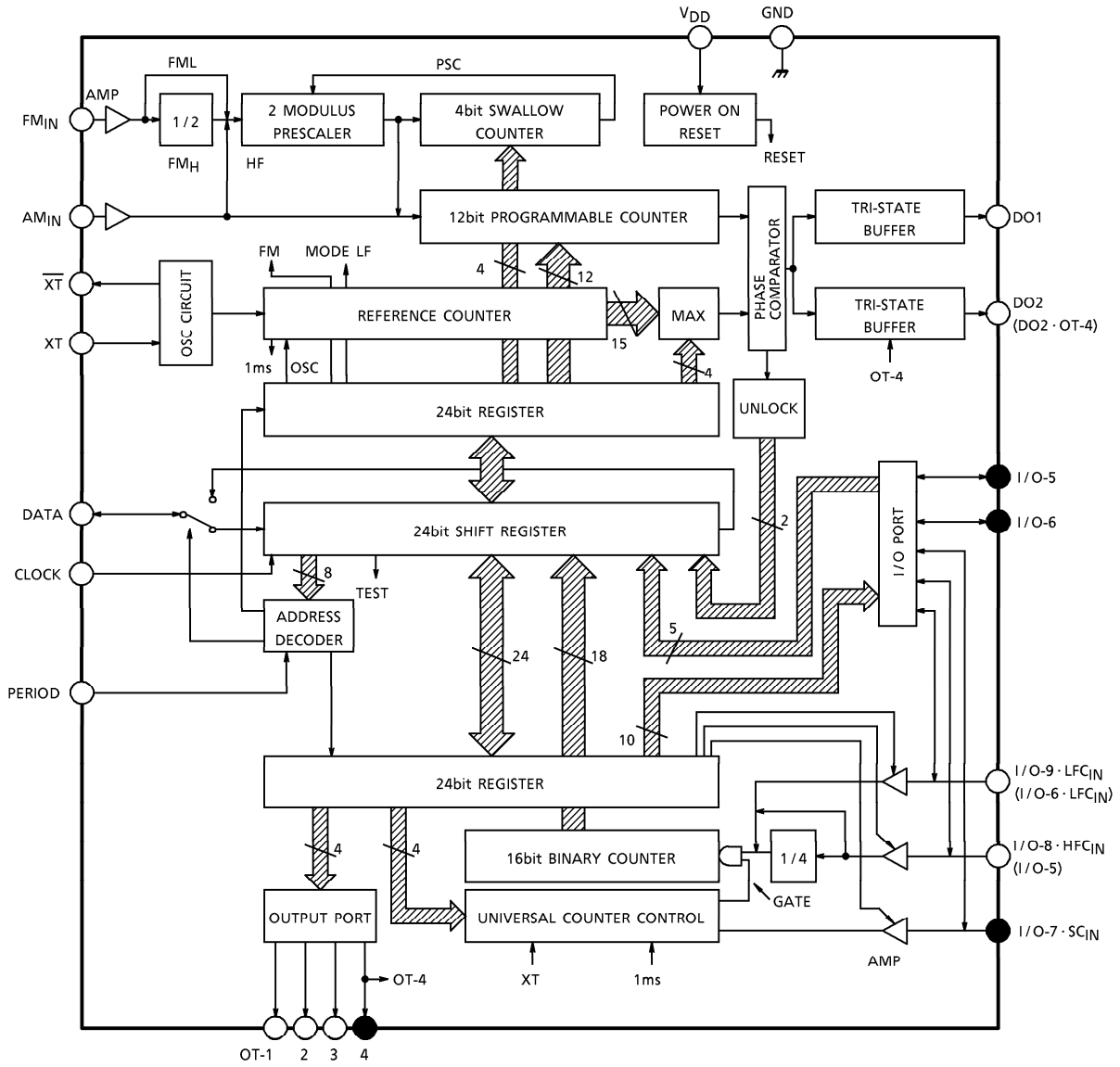
TOP VIEW
DIP-16 pin

TC9217P, TC9217F



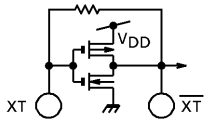
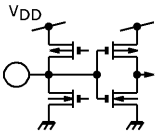
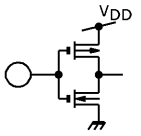
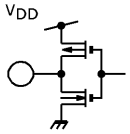
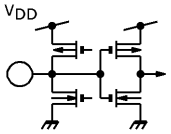
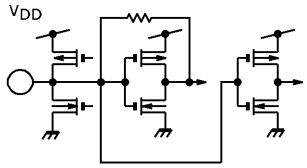
TOP VIEW
DIP-20 pin, SOP-20 pin

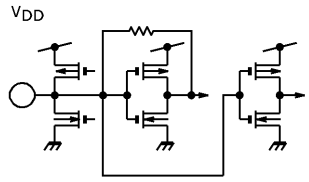
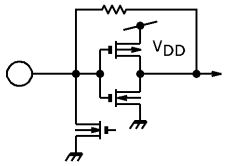
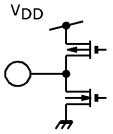
BLOCK DIAGRAM



(Note) ● Mark terminals are not existence in TC9216P.
Terminal name of TC9216P is shown in parentheses.
Others are common terminals.

PIN FUNCTION

PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
1	XT	Crystal Oscillator Terminal	Crystal resonator of 7.2MHz or 4.5MHz shall be connected to this terminal to generate reference frequency and internal clock.	
2	$\overline{XT}$			
3	DATA	Serial Data Input / Output	Serial I/O port. Serial data transfer is performed between controller and these terminals to control universal counter and I/O port, and sets frequency dividing numbers and frequency dividing mode.	 DATA  CLOCK, PERIOD
4	CLOCK	Clock Signal Input		
5	PERIOD	Period Signal Input		
6	OT-1	General Purpose Output Port	These terminals are CMOS structure and used as output of control signal etc. They are set to "L" level at power "ON". (OT-4 of TC9216P can be used by switching DO2.)	
7	OT-2			
8	OT-3			
9 (–)	OT-4			
10 (9)	I/O-5	General Purpose I/O Port	These terminals are CMOS structure and can be used freely as input or output. It becomes input port at power "ON". (Exclusive terminal of I/O port is only I/O-5 in TC9216P.)	
11 (–)	I/O-6			
12 (–)	I/O-7 · SC_{IN}	General Purpose I/O Port / Universal Counter Periodic Measurement Input	This terminal is general purpose I/O port. It can be also used as signal input terminal which performs periodic measurement of low frequency signal by program control. (Note)It is set input mode of I/O port at power "ON".	

PIN No.	SYMBOL	PIN NAME	FUNCTION AND OPERATION	REMARKS
13 (–)	I/O-8 · HFC_{IN}	General Purpose I/O port / Universal Counter Frequency Measurement Input	These terminals are general purpose I/O ports. They can be also used as input terminals for frequency measurement of universal counter by program control. Frequency measurement is available for intermediate frequency measurement etc. It is with built-in amp. and can operate small amplitude signal with capacitor coupling. (TC9216P does not have HFC_{IN} input.) (Note)It is set input mode of I/O port at power "ON".	
14 (10)	I/O-9 · LFC_{IN} (I/O-6 · LFC_{IN})			
15 (11)	AM_{IN}	Programmable Counter Input	The local oscillator signal of each FM/AM band is input to these terminals. It is with built-in amp. and can operate small amplitude signal with capacitor coupling.	
16 (12)	FM_{IN}			
18 (14)	DO1	Phase Comparator Output (General Purpose Output Port)	These terminals are tristate outputs of phase comparator. DO1 and DO2 are parallel output. (DO2 of TC9216P can be also used as general purpose output port by program control.)	
19 (15)	DO2 (DO2 · OT-4)			
17 (13)	GND	Power Supply Terminal	Power supply voltage of 5.0V ± 10% is applied to this terminal.	—
20 (16)	V_{DD}			

(*) No.1~8 pins are common terminals of TC9216P, TC9217P, TC9217F.
(*) Terminal name and number of TC9216P are shown in parentheses.

OPERATING DESCRIPTION

○ Serial I/O port

Each function is controlled by the data setting to a pair of 24bit registers, total of 48 bits. Each data of these registers is exchanged with controller side by 3 terminals of DATA, CLOCK and PERIOD through serial port.
Address 8 bits and data 24 bits, total of 32 bits, are transferred in serial at the same time.
Since all functions are controlled in the unit of register, so here explanations of address 8 bits and each register function are described chiefly. These registers are constituted in unit of 24 bits and selected by address of 8 bits. Address assignment table of each register is shown as the allocation of register in next page.

REGISTER	ADDRESS	CONSTITUTION OF 24BIT	NUMBER OF BIT
Input Register-1	D0H	Setting of PLL frequency dividing number. Selection of reference frequency. Setting of PLL input and operation mode. Selection of crystal oscillation frequency. Out-control OC.	16 4 2 1 1 (Total of 24)
Input Register-2	D2H	Control of universal counter (Control of PLL lock detection bit is included.) Test bit I/O port control Output data	9 1 5 9 (Total of 24)
Output Register	D1H (OC = 1)	Data of Register-1 (Mode B)	24 (Total of 24)
	D1H (OC = 0)	Count data of universal counter PLL lock detection data Unused (Mode A)	18 2 4 (Total of 24)
Output Register	D3H	Data of Register-2 Input data	19 5 (Total of 24)

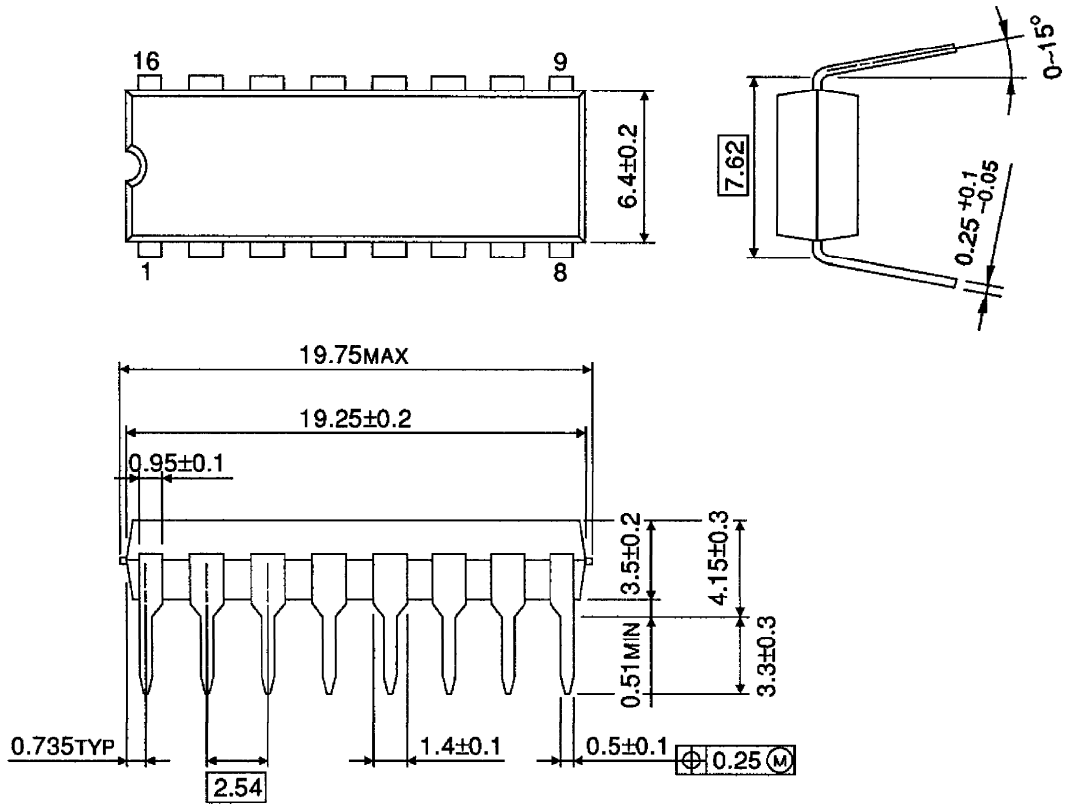
Input data is latched to register-1 or -2 at the fall timing of PERIOD signal and each function is operated.
Each output data is latched to output register in parallel at the fall timing of the 9th of CLOCK signal and output from DATA terminal serially. Serial data of DATA, CLOCK and PERIOD is synchronized with crystal oscillation clock and taken into the internal circuit of LSI. By this reason if crystal oscillation is stopped, serial data can not be input.

(Note) When power is turned on, some internal circuits have undefined states to set internal circuit states, execute a dummy data transfer at least once before performing regular data transfer.

OUTLINE DRAWING

DIP16-P-300-2.54A

Unit : mm

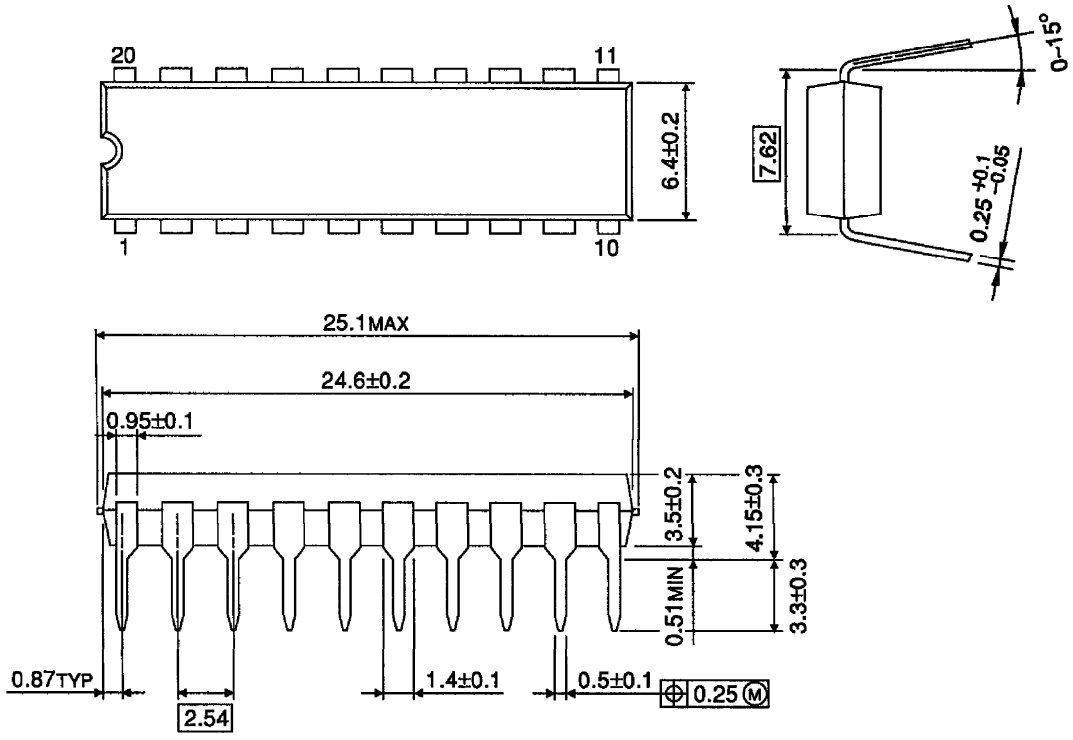


Weight : 1.0g (Typ.)

OUTLINE DRAWING

DIP20-P-300-2.54A

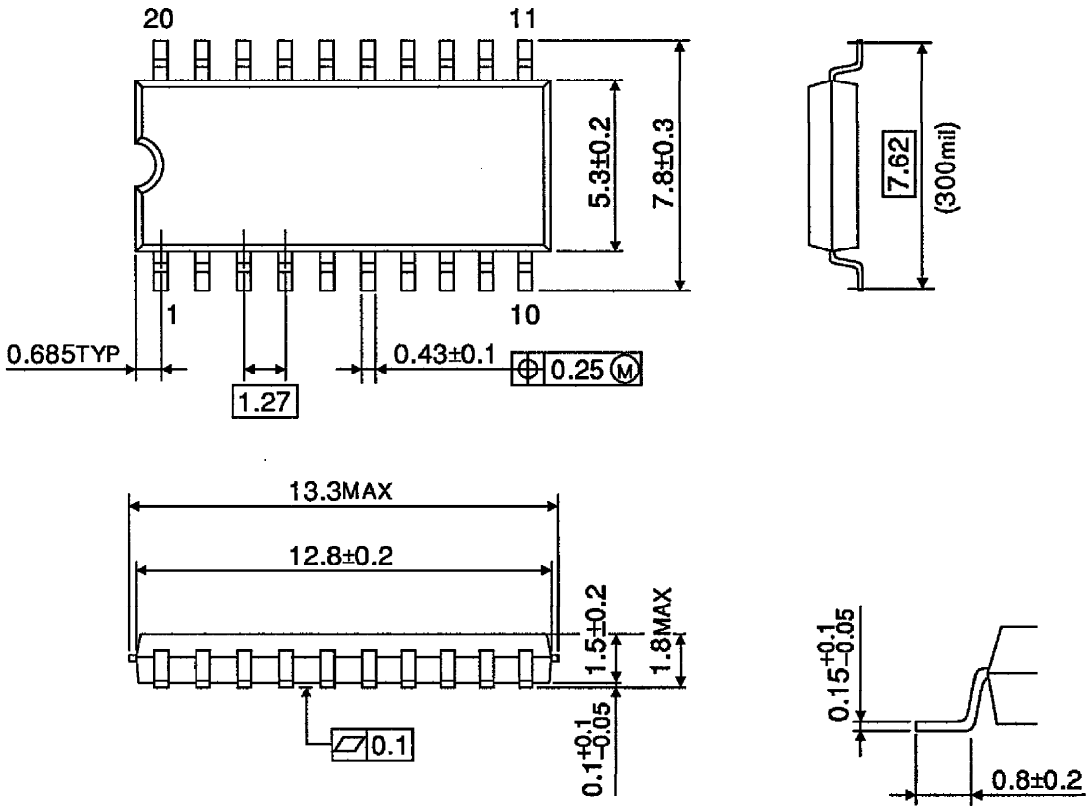
Unit : mm



Weight : 1.4g (Typ.)

OUTLINE DRAWING

SOP20-P-300-1.27 Unit : mm



Weight : 0.48g (Typ.)