

TOSHIBA BIPOLAR DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TD62383P

8CH LOW INPUT ACTIVE SINK DRIVER

The TD62383P is non-inverting transistor array which is comprised of eight Low saturation output stages and PNP input stages.

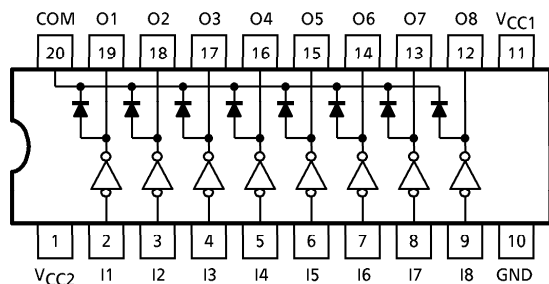
This device is low level input active driver and is suitable for operation with TTL, 5V CMOS and 5V Microprocessor which have sink current output drivers.

Applications include relay, hammer, lamp and LED display drivers.

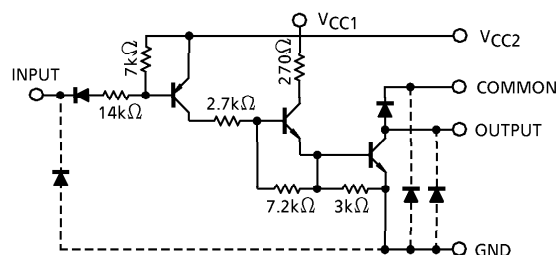
FEATURES

- Low saturation output 0.4V (Max.) @ $I_{OUT} = 350\text{mA}$
- Output rating 10V (Min.) / 500mA (Max.)
- Input compatible with TTL and 5V CMOS
- Low level active inputs
- Standard supply voltage
- Output clamp diodes
- Package type-P : DIP-20pin

PIN CONNECTION (TOP VIEW)



SCHEMATICS (EACH DRIVER)



(Note) The input and output parasitic diodes cannot be used as clamp diodes.

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MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V _{CC1, 2}	− 0.5~7.0	V
Output Sustaining Voltage	V _{CE (SUS)}	− 0.5~10.0	V
Output Current	I _{OUT}	500	mA / ch
Input Voltage	V _{IN}	− 22~V _{CC} + 0.5	V
Input Current	I _{IN}	10	mA
Power Dissipation	P _D (Note)	1.47	W
Operating Temperature	T _{opr}	− 40~85	°C
Storage Temperature	T _{stg}	− 55~150	°C

(Note) Delated above 25°C in the proportion of 11.7mW/°C.

RECOMMENDED OPERATING CONDITIONS (Ta = − 40~80°C)

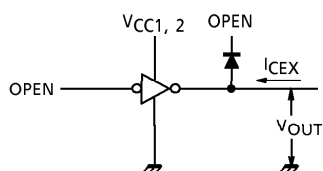
CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V _{CC1, 2}	—	4.5	5.0	5.5	V
Output Sustaining Voltage	V _{OUT}	—	0	—	10	V
Output Current	I _{OUT}	—	—	—	350	mA / ch
Input Voltage	V _{IN}	—	0	—	5.5	V
Power Dissipation	P _D	—	—	—	0.52	W

ELECTRICAL CHARACTERISTIC (Ta = 25°C)

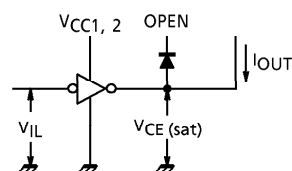
CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Leakage Current	I _{CEX}	1	V _{CC} = V _{CC2} = 5.5V, V _{OUT} = 10V I _{IN} = 0, Ta = 85°C	—	—	100	μA
Output Saturation Voltage	V _{CE (sat)}	2	V _{CC1} = V _{CC2} = 4.5V I _{OUT} = 350mA, V _{IN} = V _{IL} MAX.	—	—	0.4	V
Input Current	I _{IN (ON)}	3	V _{CC1} = V _{CC2} = 5.5V, V _{IN} = 0.4V	—	− 0.32	− 0.45	mA
Input Voltage	V _{IL}	—	I _{OUT} = 350mA	—	—	V _{CC} − 3.7	V
Clamp Diode Forward Voltage	V _F	4	I _F = 350mA	0	—	2.0	V
Clamp Diode Reverse Current	I _R	5	V _R = 10V, Ta = 25°C	—	—	50	μA
			V _R = 10V, Ta = 85°C	—	—	100	
Turn-On Delay	t _{ON}	6	V _{CC1} = V _{CC2} = 5V, V _{OUT} = 10V R _L = 28Ω, C _L = 15pF	—	0.2	—	μs
Turn-Off Delay	t _{OFF}			—	3.0	—	

TEST CIRCUIT

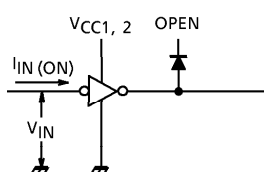
1. I_{CEX}



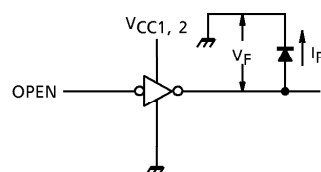
2. $V_{CE(sat)}$



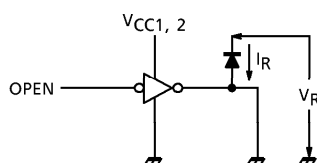
3. $I_{IN(ON)}$



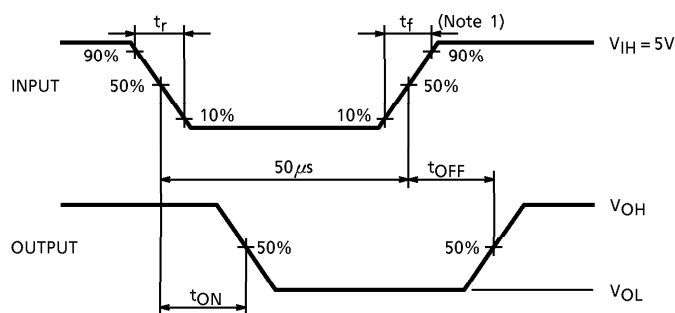
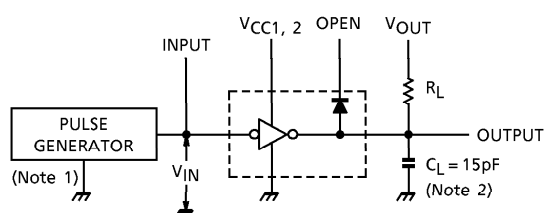
4. V_F



5. I_R



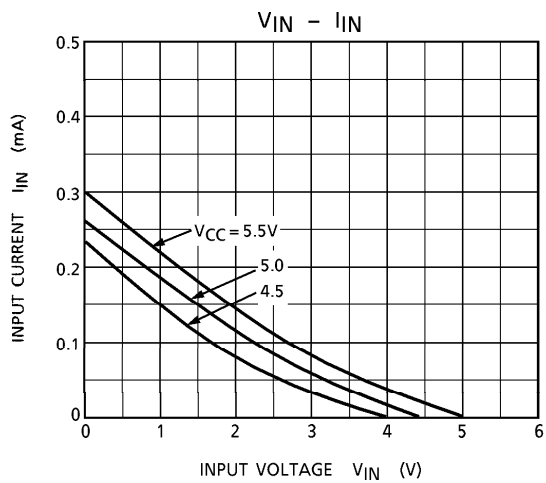
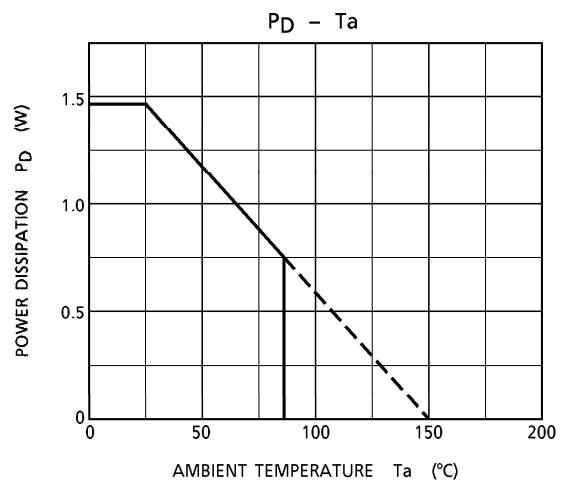
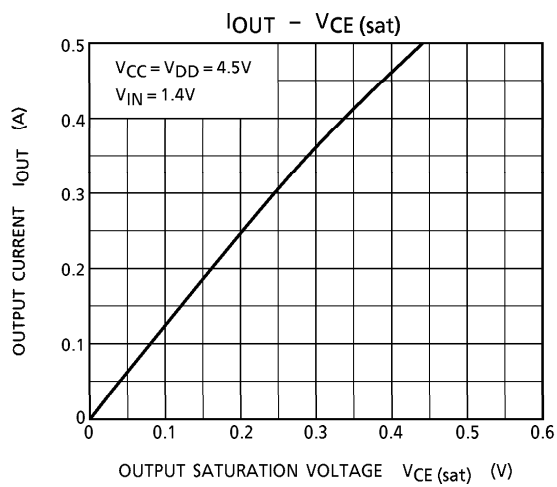
6. t_{ON} , t_{OFF}



- (Note 1) Pulse Width $50\mu s$, Duty Cycle 10%
Output Impedance 50Ω , $t_r \leq 5ns$, $t_f \leq 10ns$
(Note 2) C_L includes probe and jig capacitance.

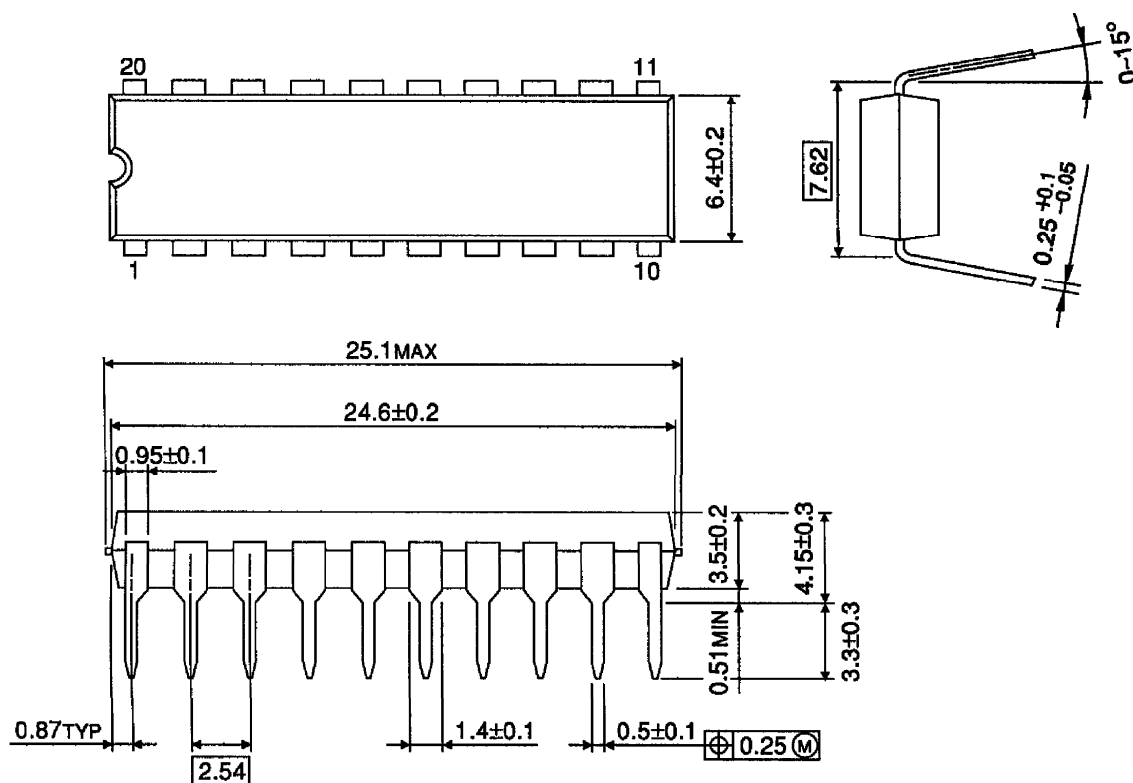
PRECAUTIONS for USING

Utmost care is necessary in the design of the output line, V_{CC} (V_{CC1} , V_{CC2}) and GND line since IC may be destroyed due to short-circuit between outputs, air contamination fault, or fault by improper grounding.



OUTLINE DRAWING
DIP20-P-300-2.54A

Unit : mm



Weight : 2.25g (Typ.)