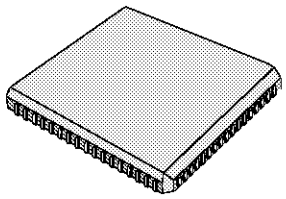
SGS-THOMSON MICROELECTRONICS

TS68483A

HMOS2 ADVANCED GRAPHIC AND ALPHANUMERIC CONTROLLER

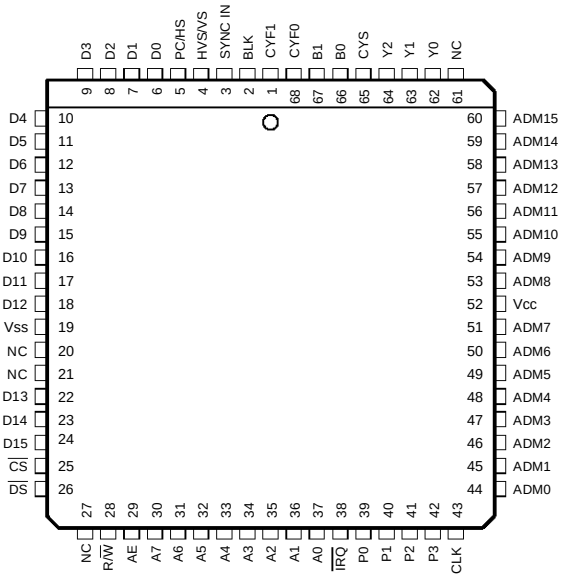
- FULLY PROGRAMMABLE TIMING GENERATOR
- ALPHANUMERIC AND GRAPHIC DRAWING CAPABILITY
- EASY TO USE AND POWERFUL COMMAND SET :
  - VECTOR, ARC, CIRCLE WITH DOT OR PEN CONCEPT AND PROGRAMMABLE LINE STYLE,
  - FLEXIBLE AREA FILL COMMAND WITH TILING PATTERN,
  - VERY FAST BLOCK MOVE OPERATION,
  - CHARACTER DRAWING COMMAND, ANY SIZE AND FONTS AVAILABLE
- LARGE FRAME BUFFER ADDRESSING SPACE (8 megabytes) UP TO 16 PLANES OF 2048 x 2048
- UP TO 256 COLOR CAPABILITIES
- MASK BIT PLANES FOR GENERAL CLIPPING PURPOSE
- FRAME BUFFER CAN BE BUILT WITH STANDARD 64 K OR 256 K DRAM OR DUAL-PORT-MEMORIES (video-RAM)
- EXTERNAL SYNCHRONIZATION CAPABILITY
- ON CHIP VIDEO SHIFT REGISTERS FOR DOT RATE UP TO 18 MEGADOTS/S
- 8 OR 16-BIT BUS INTERFACE COMPATIBLE WITH MARKET STANDARD MICROPROCESSORS
- HMOS 2 TECHNOLOGY
- 68 - PIN PLCC PACKAGE
- FOR DETAILED INFORMATION, REFER TO TS68483 USER'S MANUAL



PLCC68
(Plastic Chip Carrier)

ORDER CODE : TS68483A

PIN CONNECTIONS



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DESCRIPTION

The TS68483 is an advanced color graphic processor that drastically reduces the CPU software overhead for all graphic tasks in medium and high range graphic applications such as business and personal computer, industrial monitoring system and CAD systems.

PIN DESCRIPTION

Name	Type	Function	Description
MICROPROCESSOR INTERFACE			
D (0 : 15)	I/O	Data Bus	These sixteen bidirectional pins provide communication with either an 8 or 16-bit host microprocessor data bus.
A (0 : 7)	I	Address Bus	These eigth pins select the internal register to be accessed. The address can be latched by AE for direct connection to address/data multiplexed microprocessor busses.
AE	I	Address Enable	When TS68483 is connected to a non-multiplexed microprocessor bus, this input must be wired to VCC. For direct connection to a multiplexed microprocessor bus, the falling edge of AE latches the address on A (0 : 7) pins and the CS input. With an Intel type microprocessor, AE is connected to the processor Address Latch Enable (ALE) signal.
$\overline{DS}$	I	Data Strobe	Active Low - In non-multiplexed bus mode, $\overline{DS}$ low enables the bidirectionnal data buffers and latches the A (0 : 7) lines on its high to low transition. Data to be written are latched on the rising edge of this signal. - In multiplexed bus mode, this signal low enables the output data buffers during a read cycle. With intel microprocessors, this pin is connected to the RD signal.
R/$\overline{W}$	I	Read/Write	- In non-multiplexed bus mode, this signal controls the direction of data flow through the bidirectional data buffers. - In multiplexed bus mode, this signal low enables the input data buffers. The entering data are latched on its rising edge. With Intel microprocessors, this pin is connected to the WR signal.
$\overline{CS}$	I	Chip Select	This input selects the TS68483 registers for the current bus cycle. A low level corresponds to an asserted chip select. In multiplexed mode, this input is strobed by AE.
$\overline{IRQ}$	O	Interrupt Request	This active-low open drain output acts to interrupt the microprocessor.
MEMORY INTERFACE			
ADM (0 : 15)	I/O	Address/Data Memory	These multiplexed pins act as address and data bus for display memory interface.
CYS	O	Memory Cycle Start	The falling edge of this output indicates the beginning of a memory cycle.
Y (0 : 2)	O	Memory Address	These outputs provide the least significant bits of the Y logical address.
B (0 : 1)	O	Bank Number	These outputs provide the number of the memory bank to be accessed during the current memory cycle.
CYF (0 : 1)	O	Memory Cycle Status	These outputs indicate the nature of the current memory cycle (Read, Write, Refresh, Display).
VIDEO INTERFACE			
P (0 : 3)	O	Video Shift Register Outputs	These four pins correspond to the outputs of the internal video shift registers.
PC/HS	O	Phase Comparator/ Horizontal Sync.	This output can be programmed to provide either the phase comparator output or the horizontal sync. signal.
HVS/VS	O	Composite or Vertical Sync.	This output can be programmed to provide either the composite sync. signal or the vertical sync. signal.
SYNC IN	I	External Sync Input	This input receives an external composite sync. signal to synchronize TS68483. This input must be grounded if not used.
BLK	O	Blanking	This output provides the blanking interval information.
OTHER PINS			
V_{CC}	S	Power Supply	+ 5 V Supply
V_{SS}	S	Ground	Ground
CLK	I	Clock	Clock Input

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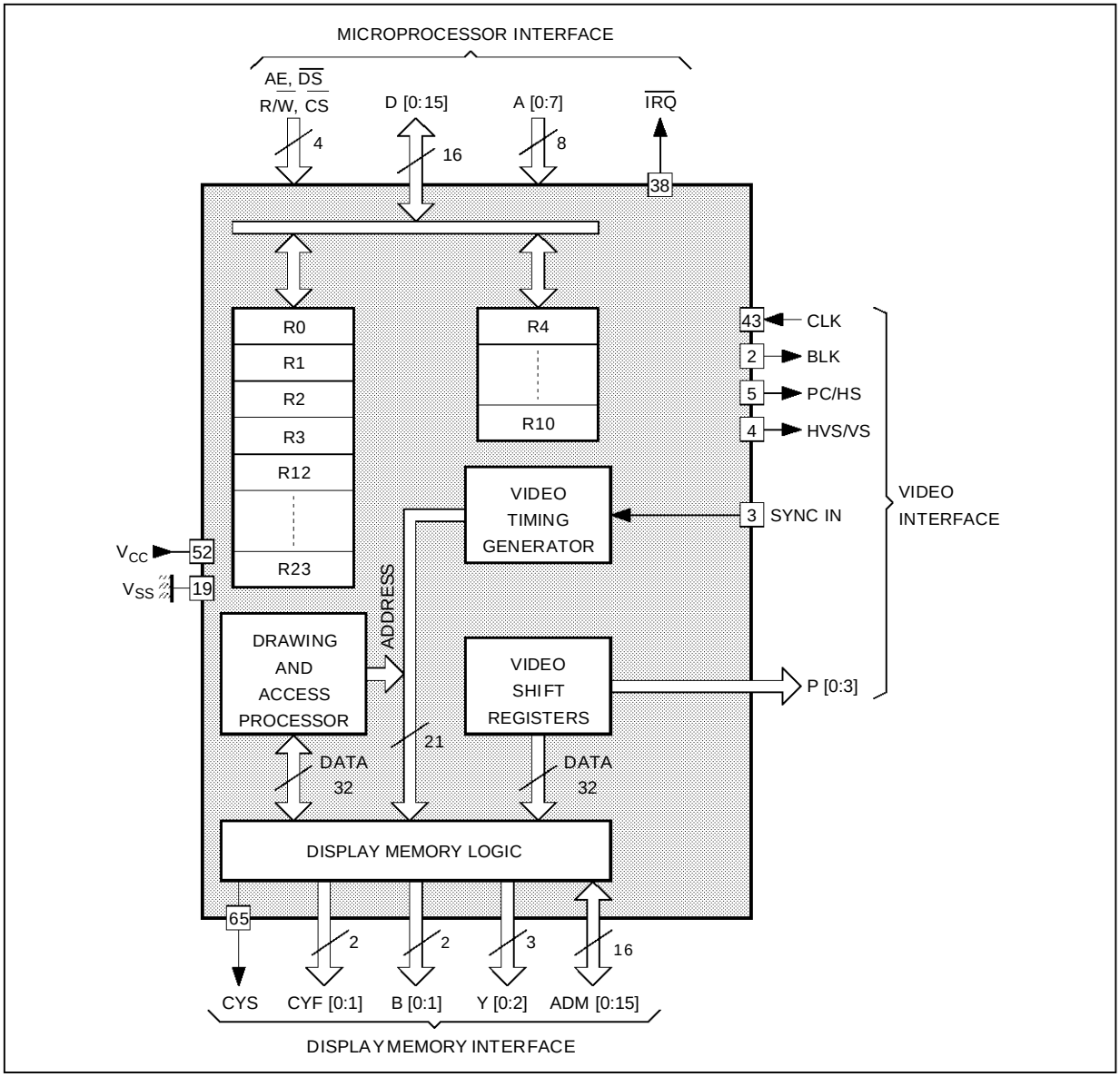
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC*}	Supply Voltage	– 0.3, 7.0	V
V_{in*}	Input Voltage	– 0.3, 7.0	V
T_A	Operating Temperature Range	0, 70	°C
T_{stg}	Storage Temperature Range	– 55, 150	°C
P_{Dm}	Max Power Dissipation	1.5	W

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* With respect to V_{SS}.

Stresses above those hereby listed may cause permanent damage to the device. The ratings are stress ones only and functional operation of the device at these or any conditions beyond those indicated in the operational sections of this specifications is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Standard MOS circuits handling procedure should be used to avoid possible damage to the device.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0 V ± 5 %, V_{SS} = 0, $T_A = T_L$ to T_H) (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IL}	Input Low Voltage	– 0.3		0.8	V
V_{IH}	Input High Voltage	2		V_{CC}	V
Iin	Input Leakage Current			10	µA
V_{OH}	Output High Voltage (I_{load} = – 500 µA)	2.4			V
V_{OL}	Output Low Voltage I_{load} = 4 mA ; ADM (0 : 15), I_{load} = 1 mA ; other Outputs			0.4	V
P_D	Power Dissipation		700		mW
C_{in}	Input Capacitance			15	pF
I_{TSI}	Three State (off state) Input Current			10	µA

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I - GENERAL OPERATION

I.1 - Introduction

The TS68483 is an advanced color graphics controller chip. It is directly compatible with most popular 8 or 16-bit microprocessors.
Its display memory, containing the frame buffer and the character generators, may be assembled from standard dynamic RAM components.
On-chip video shift registers and fully programmable Video Timing Generator allow the TS68483 to be used in a wide range of terminals or computer design.
Additional information on applications can be found in the TS68483 User's Manual.

I.2 - Typical Application Building Blocks

In a typical using TS68483, a host processor drives a display unit which drives in turn a color CRT monitor.

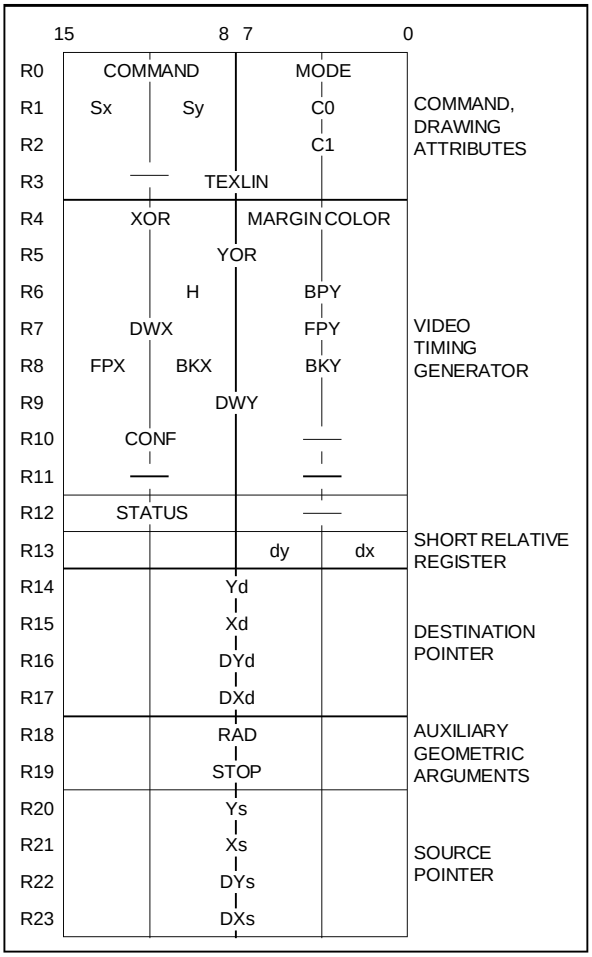
The display unit consists of four hardware building blocks :
- an TS68483 advanced graphics controller,
- a display memory (dynamic RAM),
- a display memory interface, comprising a few TTL parts,
- a CRT interface of CRT drivers.

For enhanced graphics, the CRT interface may include a color look-up table circuit. For high pixel rate (over 18 Mpixels/s), the CRT interface must include high speed video shift registers.
The display memory interface and organization are discussed in full details in the User's Manual.

I.3 - TS68483 Functions

All the TS68483 functions are under the control of the host microprocessor via 24 directly accessible 16-bit registers. These registers are referred to by their decimal index (R0-R23) (see Figure 1).

Figure 1 : Register Map



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I.3.1 - VIDEO TIMING AND DISPLAY PROCESSOR (R4 to R10).

The video timing generator is fully programmable : any popular horizontal scanning period from 20 µs to 64 µs may be freely combined with any number

of lines per field (up to 1024). The address of the display viewport (this part of the display memory to be actually displayed on the screen) is fully programmable. The display processor provides the display dynamic RAM refresh (see video timing generator section for details).

I.3.2 - DRAWING AND ACCESS COMMANDS (R0 to R3, R12 to R23).

The 16 remaining registers are used to specify a comprehensive set of commands. The highly orthogonal drawing command set allows the user to "draw" in the display memory such basic patterns as lines, arcs, polylines, polyarcs, rectangles and characters. Efficient procedures are available for either area filling and tiling or line drawing and texturing. Lines may be drawn with a PEN in order to get thick strokes. Any drawing is specified in a $2^{13} \times 2^{13}$ drawing coordinate system.

To access the display memory, the host microprocessor has an indirect, sequential access to any "window". Access commands can be used to load the character generators as well as to load or save arbitrary windows stored in the frame buffer.

I.4 - Data Type Definitions

PIXEL : this is the smallest color spot displayable on the CRT.

PEL : a Picture Element is the coding of a PIXEL in the display memory. The TS68483 can handle 4 different PEL formats :
- 4 color bits - short
- 4 color bits + 1 mask bit - short masked
- 8 color bits - long
- 8 color bits + 1 mask bit - long masked

DRAWING COORDINATES : (see Figure 2)
The drawing commands are specified and computed in a $2^{13} \times 2^{13}$ cyclical coordinate system. The drawing coordinates are clipped and mapped into the $2^{11} \times 2^{11}$ display memory addressing space. Further clipping to the actual frame buffer size may be performed by the user designed memory interface.

DISPLAY MEMORY :
This is the dedicated memory to the display unit. This memory is addressed as four banks of 4-bit plane each.

BIT PLANE :
Each bit plane has a maximum capacity of $2^{11} \times 2^{11}$ bits. A byte wide organization of each bit plane is required.

MEMORY ADDRESS : (see Figure 3).
In order to address one bit in the display memory, the user must specify :
- A bank number (2 bits) B = 0 to 3
- A bit plane number (2 bits) Z = 0 to 3
- A Y address (11 bits) Y = 0 to 2047
- An X address (11 bits) X = 0 to 2047

MEMORY WORD : (see Figure 3)
A 32-bit memory word can be either read or written during each memory cycle (8 CLK periods), one byte at a time in each bit plane in the addressed bank. The memory bandwidth is in the 6 to 8Mbytes/s range.

VIEWPORT :
This is any rectangular array of pels located in the display memory.

FRAME BUFFER :
This is the biggest viewport which can be held in the display memory. The frame buffer maps a window at the origin of the drawing coordinates. A short pel frame buffer may be located in any bank. A long pel frame buffer must be located in the "bank 0, bank 1" pair.

DISPLAY VIEWPORT :
This is the viewport which is displayed on screen.

MASK BIT PLANE :
When masked pels are used, a mask bit plane must be associated to a frame buffer. Mask bit planes may be located in any plane of bank 3.

CELL :
A CELL is any pattern stored in the display memory as a rectangular array of bit mapped elements. The drawing of any CELL may be specified with a scaling factor.

CHARACTER :
This is a one bit per element CELL. It may be stored in any bit plane, then colored and drawn in a frame buffer by use of PRINT CHARACTER command.

OBJECT :
This is a one short pel per element CELL. It may be drawn or loaded in a frame buffer. A source mask bit may be associated to each element. An OBJECT may then be printed in another location by use of a PRINT OBJECT command.

PEN :
This is the pattern which is repeatedly drawn along the coordinates defined by either a LINE or an ARC command.

The PEN may be a DOT (single pel), a CHARACTER or an OBJECT.

Figure 2 : Cyclical Drawing Coordinates to Display Memory Mapping

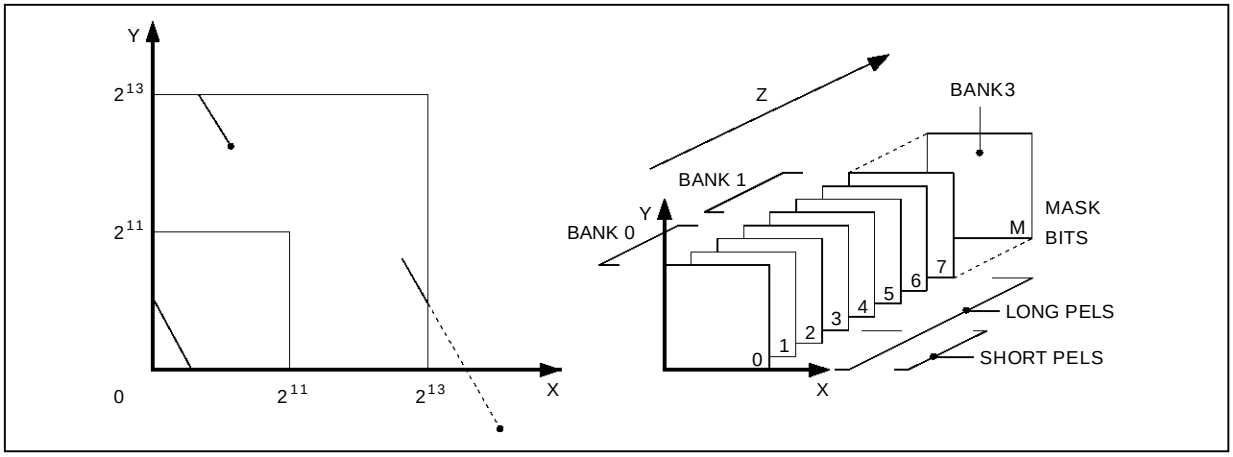
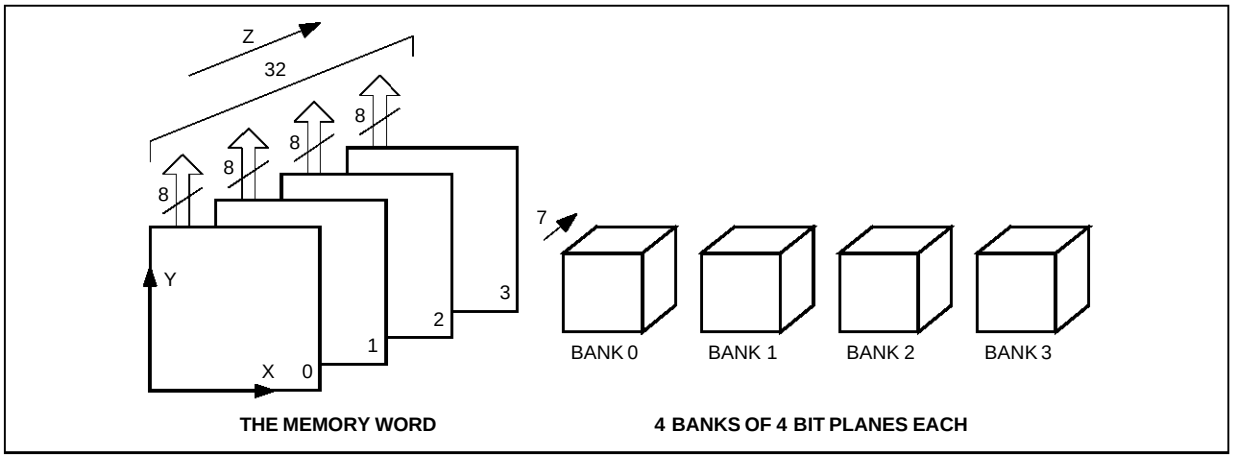


Figure 3 : The Display Memory Addressing Space



II - COMMANDS

II.1 - Introduction

The command set is strongly organized in five subset or command types.

DRAWING COMMANDS :
- LINEAR (line, arc)
- AREA (rectangle, trapezium, polygon, polyarc)
- PRINT CELL (print character, print object)

ACCESS COMMANDS

CONTROL COMMANDS (move cursor, abort)

The commands are parametered ; this means that any command can be executed with options freely selected out of a given option set. This option set is common for any command of a given type. For example, any drawing command may be parametered for destination mask bit use.

The command code also defines the command type and its parameters. A command is completely defined when a value has been set for each of its arguments.

These arguments are :
- the geometric arguments given in the drawing coordinate system for every drawing command. They are automatically mapped into the destination frame buffer ;
- the parametric values are the values required by the selected parameters ;
- the attribute values are the other values required by a drawing command ; colors or scaling factors for example ;
- the display memory addresses.

The command code is specified in register R0. Before initiating a command execution, each argument must be specified in its dedicated register : - an Xd, Yd drawing coordinate pair for example, is always located in registers R14, R15.

The monitoring of a command execution is done by reading the status register R12 or using the IRQ signal.

Table 1 : Command Set Structure

Command	Drawing Mode	Type	Group
Line Arc	Up to the Pen	Linear	Drawing
Rectangle Trapezium Polygon Polyarc	Monochrome	Area	
Print Char Print Object	Bichrome Polychrome	Cell	
Load Viewport Save Viewport Modify Viewport		Access	Management
Move Cursor Abort		Control	

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II.2 - Pointers and Geometric Arguments (see Figure 4)

Pointers are used to specify main geometric arguments and display memory addresses.

II.2.1 - DISPLAY MEMORY ADDRESS

A bit in the display memory is addressed by :

- a bank number B = 0 to 3
- a plane number Z = 0 to 3
- an X address X = 0 to 2047
- a Y addres Y = 0 to 2047

II.2.2 - DESTINATION POINTER : Registers R14 to R17

This pointer gives the coordinate (Xd, Yd) and dimension (DXd, DYd) of either a line or a window in the drawing coordinate system. These drawing coordinates are easily mapped into a PEL DISPLAY MEMORY address.

(X, Y) coordinates are clipped to 11 bits in order to get the Xd, Yd destination pel addresses.

A bank number Bd must be explicitly provided to address a destination frame buffer. When long pels are used, Bd must be even.

When masked pels are used, the destination mask plane number Zd (implicitly in bank 3) must also be provided.

II.2.3 - SOURCE POINTER : Registers R20 to R23.

A source cell such as a character, a pen or an object, is addressed by the source pointer in the display memory.

A source pointer specifies :

- a bank number Bs = 0 to 3
- a Ys address Ys = 0 to 2047
- an Xs address ; this address is a byte address so that the 3 LSBs are not specified Xs = 0 to 255
- a cell dimension DXs, DYs
- a bit plane address Zs.

When a character is addressed, Zs gives the plane number into the bank Bs. When an object is addressed Zs gives the source mask plane number in the bank B3.

II.2.4 - NOTES :

1. The TRAPEZIUM command makes a special use of R21. In this case, R21 holds an X1 drawing coordinate which has the same format as Xd.
2. The ARC and POLYARC commands require two extra geometric parameters (RAD and STOP). They are specified in the drawing coordinates system and stored in registers R18, R19.
3. Any drawing command may be parametered to use short incremental dimensions, DXY in register R13 instead of the standard DXd, DYd in the "R16, R17" register pair (see Figure 5).
4. The access commands use the destination pointer location as a data buffer. The memory addresses and dimension of the access viewport are then specified in the source pointer, independently of the data transfer.
5. DXd, DYd and DYs may specify a negative value. In this case, they must be coded by a sign (0 = positive, 1 = negative) and an 11-bit absolute value.

Figure 4 : Pointers

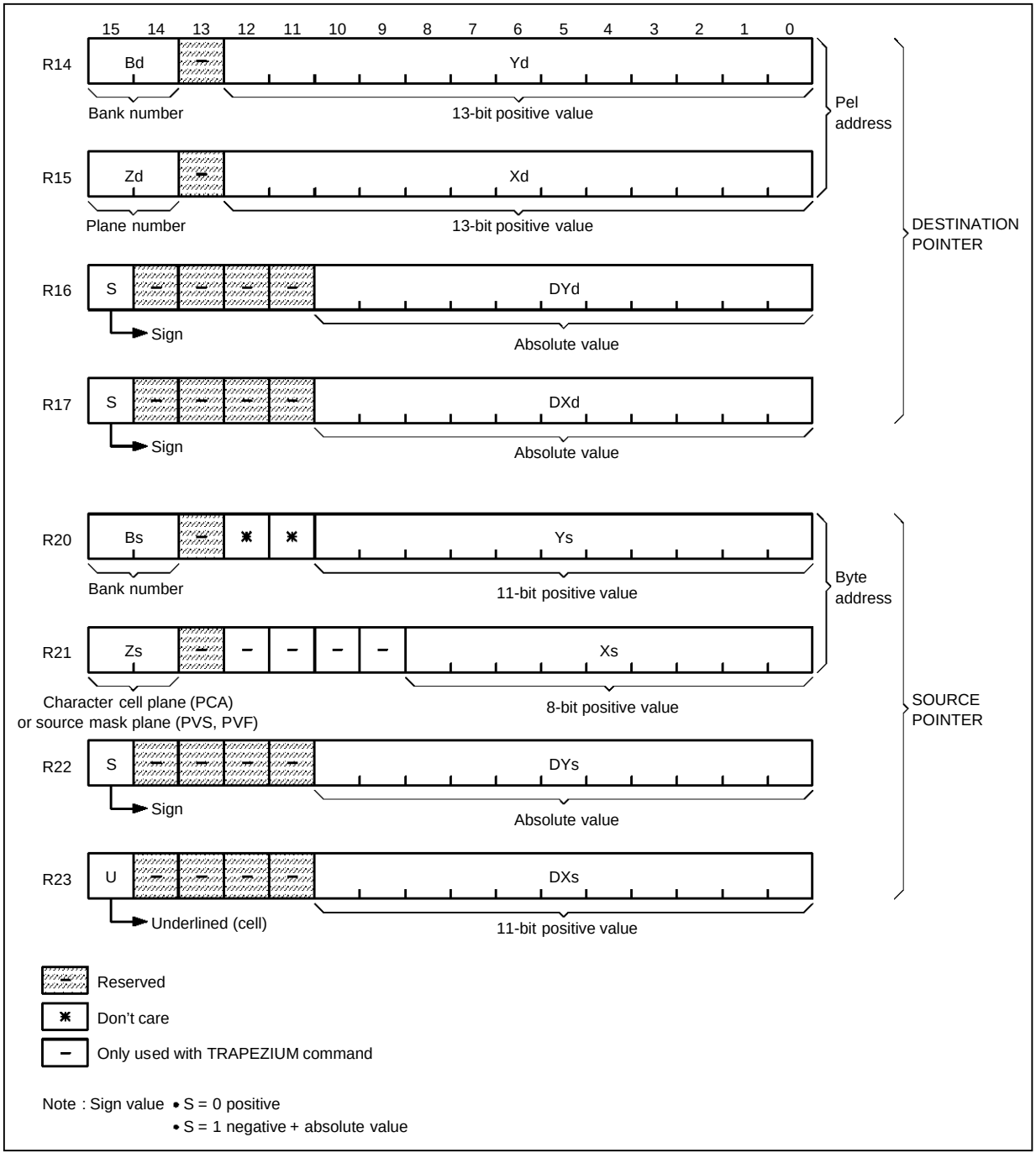
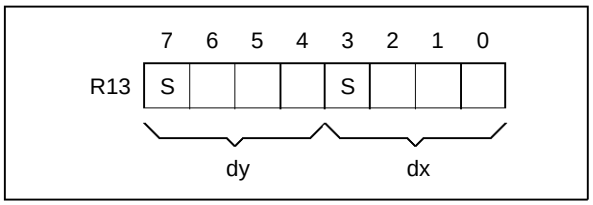


Figure 5 : Short Dimension Register R13



II.3 - Destination Mask and Source Mask

A mask bit may be associated to any pel stored in the display memory.

II.3.1 - DESTINATION MASK USE (DMU)

Any drawing command may be parametered for destination mask use. In this case, any destination pel cannot be modified when its mask bit is reset.

In other words :
- When the destination mask use (DMU) parameter is set :
  - a pel may be modified when its mask bit is set
  - a pel cannot be modified when its mask bit is reset.
- When the destination mask use (DMU) parameter is cleared :
  - a pel may be modified, independently of its mask bit value.

This provides a very flexible clipping mechanism not restricted to rectangular windows. (See destination pointer section for destination mask bit addressing).

II.3.2 - SOURCE MASK USE (SMU)

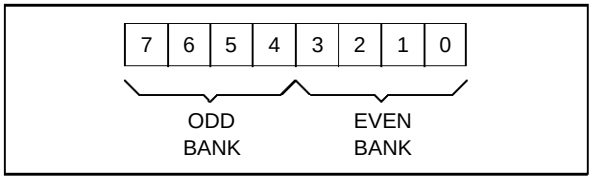
A PRINT OBJECT command may be parametered for source mask use. In this case, the source mask bit associated with any source pel is read first. When its mask bit is cleared, a source pel is considered as transparent. (See source pointer section for source mask bit addressing).

In other words :
- When the SMU parameter is set, the color of a destination pel, mapped by a given source pel, may take this source color value only when this source bit mask is set. The destination pel keeps its own color value when the source bit mask is cleared.
- When the SMU parameter is cleared, a source pel color may be mapped into destination pel color independently of the source bit mask value.

The source bit mask acts as a TRANSPARENCY/OPACITY flag which is enabled by SMU. A PRINT OBJECT command may be independently parametered by both SMU and DMU. This provides a very powerful tiling, print object or move mechanism.

II.4 - Drawing Attributes

Figure 6 : Color Register



The general drawing attributes are the colors, the drawing mode, and the scaling factor.

II.4.1. COLORS : Registers R1 and R2

Two 8-bit color values, C0 and C1, may be specified in registers R1 and R2. The low order 4-bit nibble of a color value is drawn in an even bank. The high order color nibble is drawn in an odd bank. When long pels are used, banks 0 and 1 are generally addressed as the frame buffer. When short pels are used, any bank may hold a frame buffer. In this case, the bank parity selects the color nibble used. (See destination pointer section for bank addressing).

II.4.2. DRAWING MODE : Register R0

The drawing mode defines the transforms to be applied to the pels designated by the drawing commands. There are three drawing modes.

II.4.3. MONOCHROME MODE

Any AREA drawing command, RECTANGLE for instance, defines through its geometric arguments an active set of destination pels, that is to say a set of pels to be modified.

When DMU = 1, this active set is further reduced by the masking mechanism to only these destination pels with a bit mask set.

The active destination pels are then modified according to two elementary transforms coded in R0.

COLOR TRANSFORM :

The color value C of each active pel is modified according to one color transform selected out of four :
- 00 - printed in C0 : $C \leftarrow C0$
- 01 - printed in C1 : $C \leftarrow C1$
- 10 - printed in "transparent" : $C \leftarrow C$
- 11 - complemented : $C \leftarrow \overline{C}$

This yields to a reversible marker mode.

MASK BIT TRANSFORM :

The destination mask bit of each active pel is modified according to one mask transform selected out of four :
- 00 - reset bit mask : $M \leftarrow 0$
- 01 - set bit mask : $M \leftarrow 1$
- 10 - no modification : $M \leftarrow M$
- 11 - complement bit mask : $M \leftarrow \overline{M}$

This scheme allows the color bits and the mask bit of any pel belonging to the active set to be modified independently. The color transform is performed first.

II.4.4 - BICHROME MODE

A PRINT CHARACTER command is more complex because it involves two different active sets : FOREGROUND and BACK GROUND.

The FOREGROUND is that set of destination pels printed from set elements in the character cell. The BACKGROUND is made of all the remaining pels belonging to the destination window.

When DMU = 1, the FOREGROUND and BACK GROUND are further reduced by the destination masking mechanism (see Figure 8).

A bichrome drawing mode is defined by 4 elementary and independent transforms (see Figure 7) :
- a color transform and a mask transform for the FOREGROUND PELS

- a color transform and a mask transform for the BACKGROUND PELS

II4.5 - POLYCHROME MODE

A print object command defines a source window through the source pointer :

When SMU = 0, any pel of this window is active, mapped and clipped to the destination window dimension.

When SMU = 1, only pels which have a source mask bit set are active, mapped and clipped to the destination window dimension.

In both cases, when DMU = 1, the active source pels are further reduced by the destination masking mechanism.

Both mask transforms must be programmed at "NO MODIFICATION" for correct operations (see Figure 7).

II.4.6 - THE LINEAR DRAWING COMMAND CASE

A LINE or ARC drawing command may be executed in any drawing mode depending on the PEN.

When the pen is a DOT, this pel is printed at each active coordinate according to monochrome mode.

When the pen is a CELL, this cell is printed at each active coordinate. In the bichrome mode when the cell is a character, and in the polychrome mode when the cell is an object.

For each active coordinates, the active destination set is defined by the cell dimensions (DXs, DYs).

Note : when the cell is an object, SMU is not programmable and is implicitly set. A calculated coordinate is active when the rotated LSB linear texture bit in (R3) is set.

Figure 7 : Drawing Mode Register R0

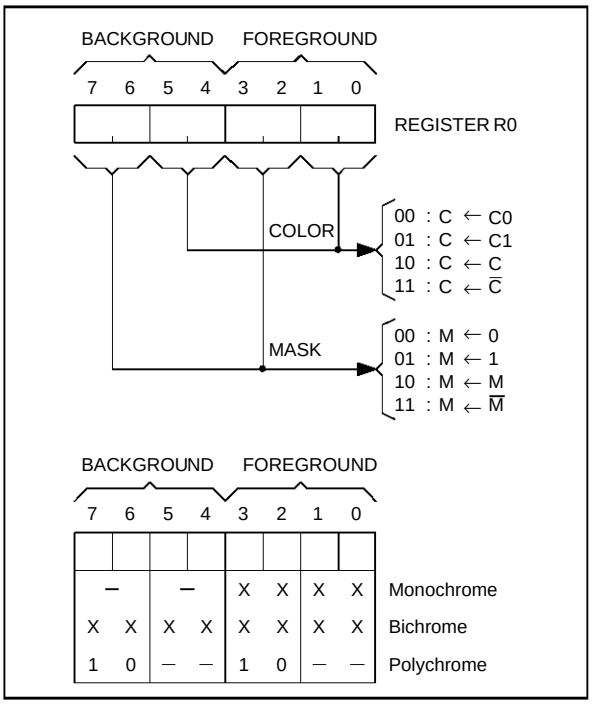
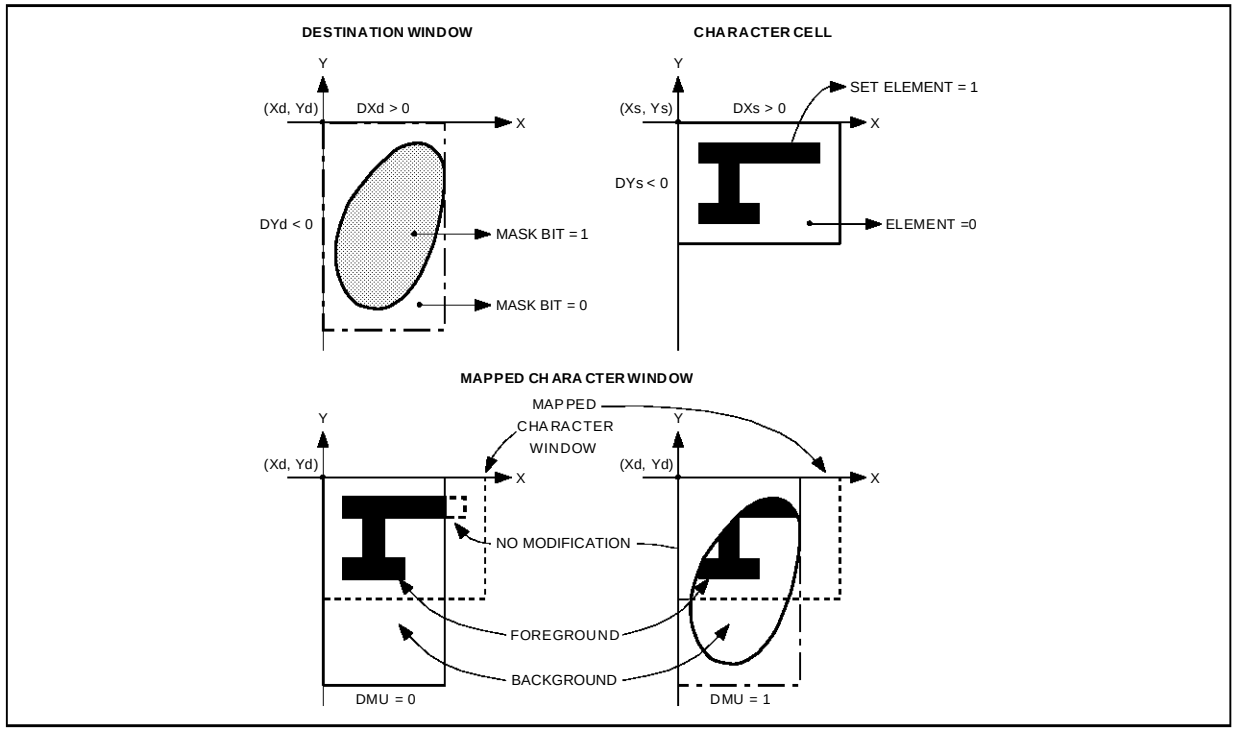
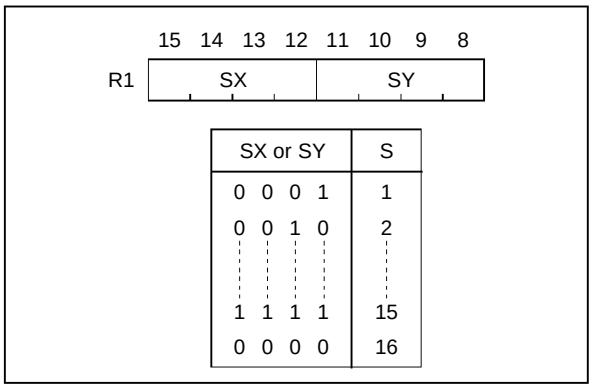


Figure 8 : Print Character Command



II.4.7 - SCALING FACTOR AND CELL MAPPING : (see Figures 9 and 10)

Figure 9 : Scaling Factor



SX or SY	S
0 0 0 1	1
0 0 1 0	2
...	...
1 1 1 1	15
0 0 0 0	16

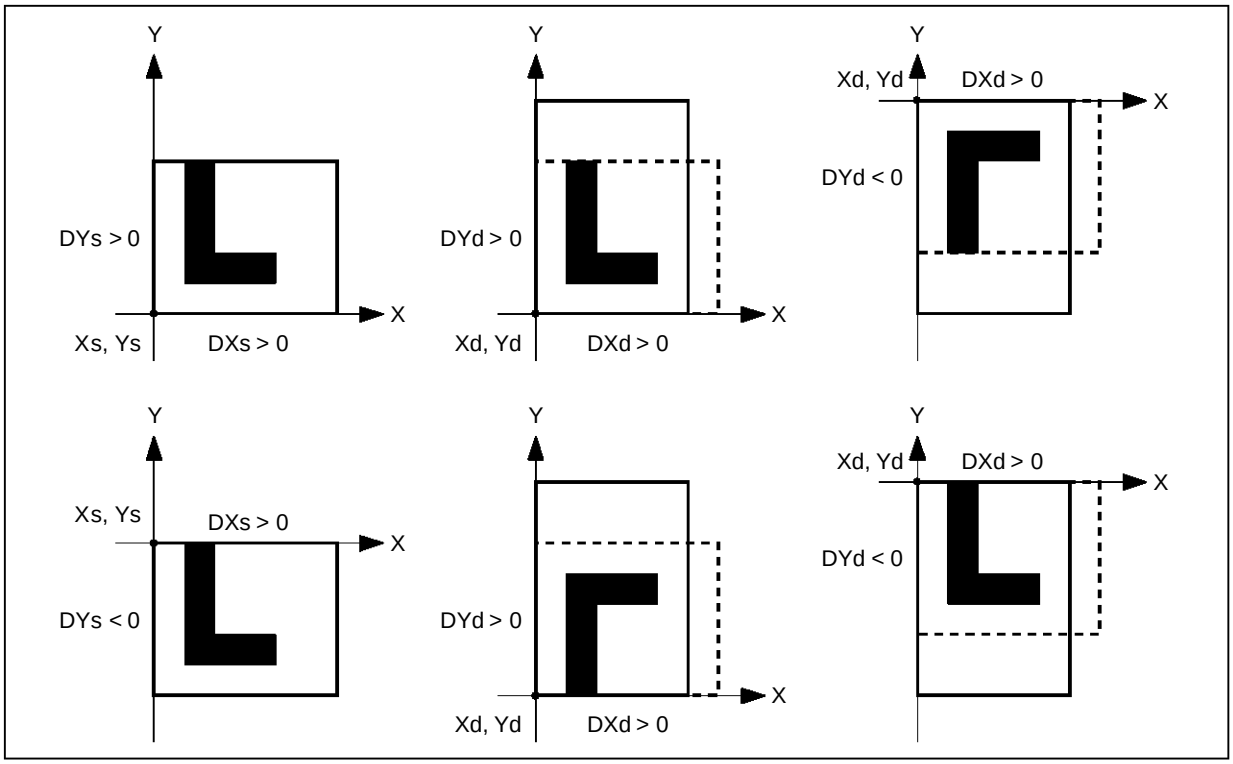
Any cell may be printed with a scaling factor. This scaling factor is an integer pair Sx, Sy = 1 to 16. This scaling factor is interpreted with the PRINT CHARACTER, PRINT OBJECT and LINEAR commands when the pen is a cell. The AREA or ACCESS or LINEAR (DOT) commands are never scaled.

The LINEAR (PEN) command should be used with a scaling factor of 1 because the pen is clipped at DXs, DYs.

The scaling factor is first applied to the source cell before mapping and drawing. The drawing and mapping is processed with sign bit of DYd and DYs values (see Figure 10).

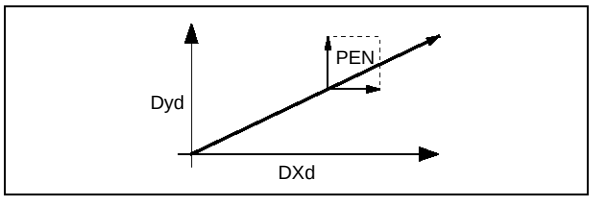
Notes :
- DXs is always positive
- The DYs sign mirrors the cell
- DXd must be positive with a PRINT CELL command
- DXd and DYd may get any sign with a LINEAR DRAWING command. If a pen is used, these signs are then irrelevant to the pen drawing. The pen is mapped with positive increment values.

Figure 10 : Cell Mapping versus DYd, DYs SIGN



II.5 - Command Set Overwiew

Figure 11



II.5.1 - LINEAR DRAWING
LINE (Xd, Yd, DXd, DYd). ARC (Xd, Yd, DXd, DYd, RAD, STOP).
The curve may be drawn with any pen and with any linear texture (register R3). For each set of computed coordinates, R3 is right rotated and the pen is printed when the shifted bit is set.

II.5.2 - AREA DRAWING
- RECT (Xd, Yd, DXd, DYd)
- TRAPEZIUM (Xd, Yd, DXd, DYd, X1)
- POLYGON (Xd, Yd, DXd, DYd)
- POLYARC (Xd, Yd, DXd, DYd, RAD, STOP)

Either RECT or TRAPEZIUM allows to draw directly all the pels inside the boundary.

Any other closed boundaries may be filled by a 3-step process :

1. The mask bits inside a boundary box must be reset by a RECT command.
2. A sequence of mixed POLYGON and POLYARC commands describing the closed boundary sets the mask bits of the pels inside this boundary.
3. This area may then be painted by a RECTANGLE command defined for a bounding box, with destination masking. It may also be tiled by use of a PRINT CELL command.

Note : the mask bit of any pel lying on the boundary itself is not guaranteed to be set by step 2.

II.5.3 - PRINT CELL COMMANDS
PRINT CELL (Xd, Yd, DXd, DYd ; Xs, Ys, DXs, DYs).
The cell addressed by Xs, Ys, DXs, DYs is scaled then printed at location Xd, Yd and clipped at the dXd, dYd dimensions.

When dXd, dYd is much larger than DXs, DYs the command may be parametered for repeat drawing.

These commands may also be parametered for destination mask use.

Further more the PRINT OBJECT command may be parametered for source mask use.

These commands have a wide range of applications : text drawing, area tiling, print or move objects, scale and move viewports.

Note : an underlined cell is drawn when the MSB of R23 is set.

II.5.4 - ACCESS COMMANDS
- LOAD VIEWPORT (Xs, Ys, DXs, DYs)
- SAVE VIEWPORT (Xs, Ys, DXs, DYs)
- MODIFY VIEWPORT (Xs, Ys, DXs, DYs)

These commands provide sequential access to a viewport in a frame buffer from the microprocessor data base.

Data are transferred to/from the display memory, word sequentially.

The R14 to R17 registers are used as a two memory word FIFO (memory word is 8 short pels, i.e. 4 bytes).

The source pointer (R20-R23) is used to address the viewport for all access commands.

When long pels are used, the command must be executed once more when the bank number in R20 has been updated.

II.5.5 - COMMAND EXECUTION
Each on-chip 16-bit register has four addresses. One address is used for plain read or write. The other addresses are used to initiate command execution automatically on completion of the register access.

This scheme allows the command code and its arguments to be loaded or modified in any other. An incremental line drawing command, for example, may be executed again and again with successive incremental dimensions and whithout need to reload the command code itself.

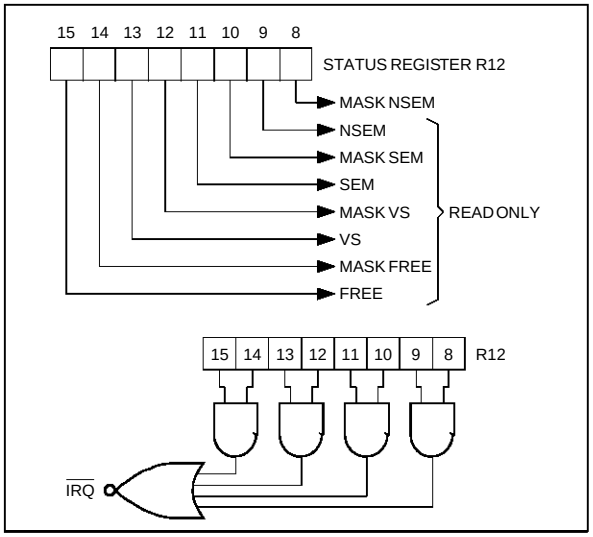
As soon as a command execution is started, the FREE bit is cleared in the STATUS register. This bit is automatically set when the execution is completed.

The commands are generally executed only during retrace intervals. However full time execution is possible when either the display is disabled or video RAM components are used.

II.5.6 - STATUS REGISTER (see Figure 12)
This register holds four read-only status bits :
- FREE : this status bit is set when no execution is pending
- VS : vertical synchronization state
- SEM : this status bit is set when the FIFO memory word is inacessible to the microprocessor during a viewport transfer
- NSEM : this status bit is set when the FIFO memory word is accessible to the microprocessor during a viewport transfer.

Each of these status bits is maskable. The masked status bits are NORed to the $\overline{IRQ}$ output pin.

Figure 12 : Status Register



III - MICROPROCESSOR INTERFACE

III.1 - Introduction

The TS68483 is directly compatible with any popular 8 or 16-bit host microprocessor ; either Motorola type (6809, 68008, 68000) or Intel type (8088, 8086).

The host microprocessor has direct access to any of the twenty four 16-bit on-chip registers through the microprocessor interface pins :

- D(0:15) : 16 bidirectional data pins.
- A(0:7) : 8 address inputs
- AE, DS, R/ W, CS : 4 control inputs.

The twenty four registers are mapped in the host addressing space as 256 byte addresses (see Figure 13)

- A(1:5) select one out of 24 registers.
- A0 selects the low order byte (A0 = 1) or the high order byte (A0 = 0) of the selected register.
- A(6:7) provide the command execution condition.

The host microprocessor bus may be either 8 or 16-bits wide and may be address/data multiplexed or not.

The two flags MB and BW in the CONFIGURATION register R10 allow the data bus size and multiplexed/non-mutiplexed organization to be specified (see Table 2).

Figure 13 : On-chip Address and Byte Packing

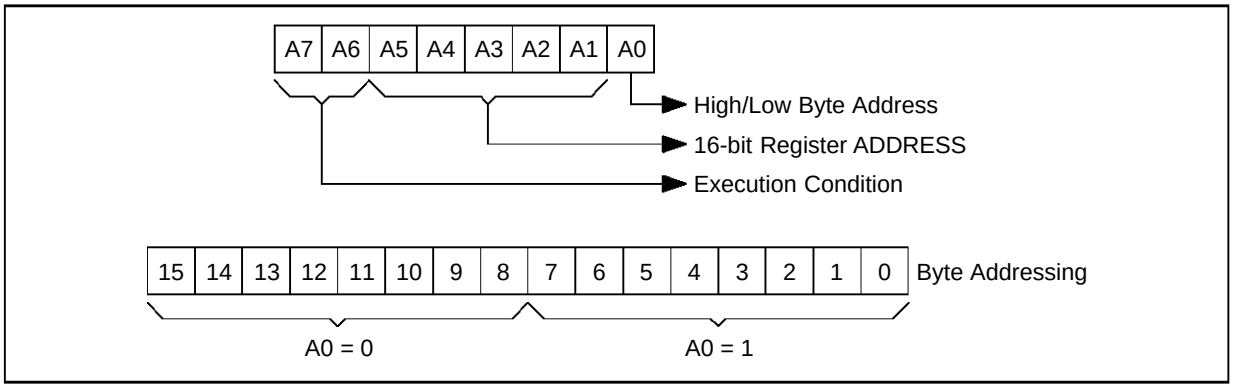


Table 2 : MPU Selection

Type of MPU Bus		Conf. Reg.		TS68483 Pins					
		BW	MB	AE	$\overline{DS}$	R/$\overline{W}$	AO	A (1 : 7)	D (8 : 15)
Non Mux	16-bit (68000)	0	0	1	$\overline{UDS}$ or $\overline{LDS}$	R/$\overline{W}$	O	A (1 : 7)	D (8 : 15)
	8-bit (68008)	1	0	1	$\overline{DS}$	R/$\overline{W}$	AO	A (1 : 7)	D (0 : 7)
Mux	16-bit (8086)	0	1	ALE	$\overline{RD}$	$\overline{WR}$	O	AD (1 : 7)	AD (8 : 15)
	8-bit (8088)	1	1	ALE	$\overline{RD}$	$\overline{WR}$	$\overline{ADO}$	AD (1 : 7)	AD (0 : 7)

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Figure 14 : Interface with TS68000/68008 MPU

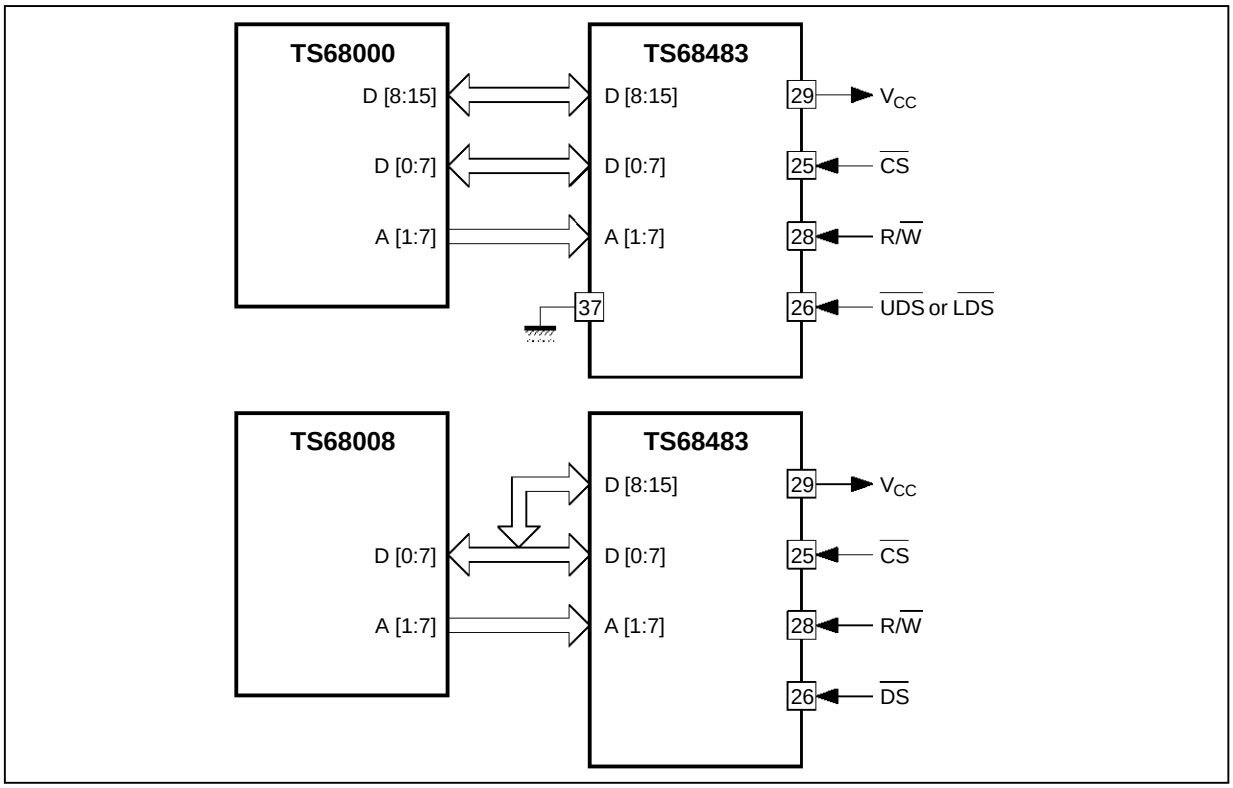
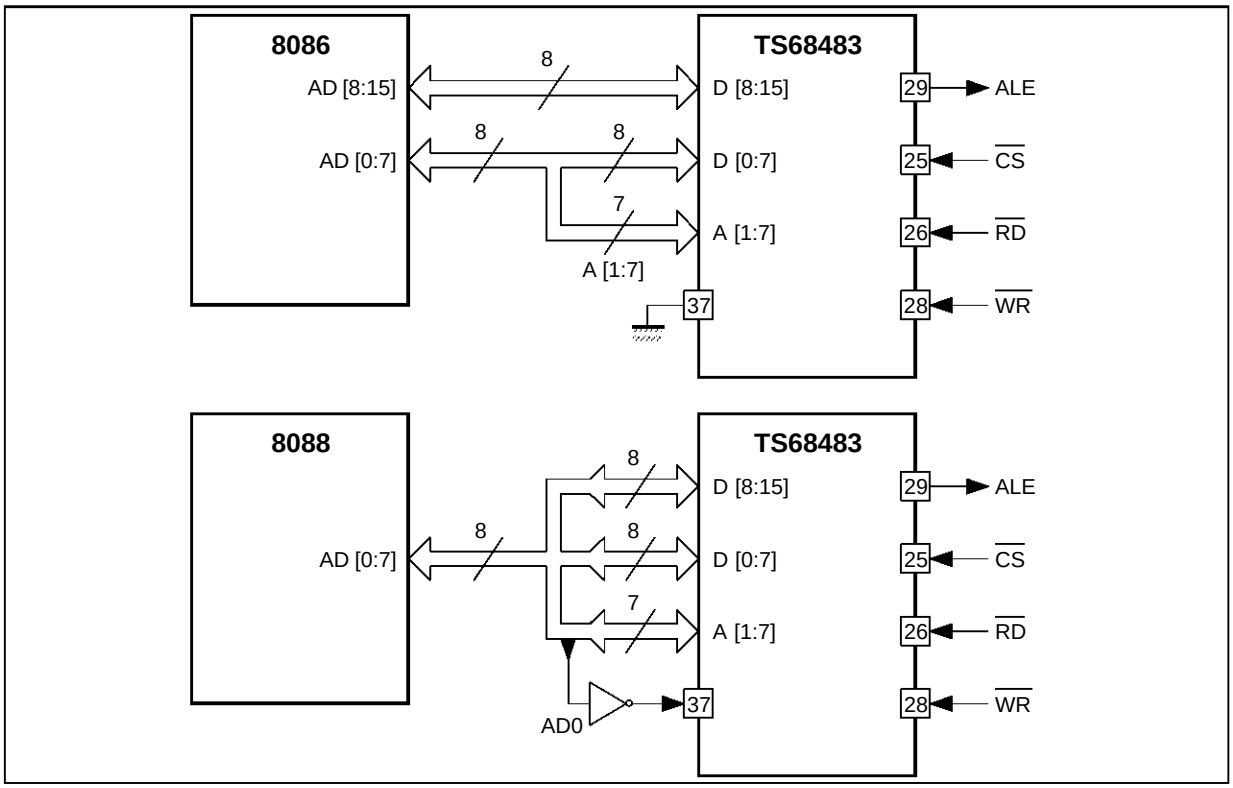


Figure 15 : Interface with 8086/8008 MPU



III.2 - Hardware Recommendations

(see Figures 21, 22, 23 and 24)

A0-PIN :

1. When using a 16-bit data bus, the A0 input pin must be grounded. No single byte access can be performed.
2. In order to conform with the high byte/low byte on-chip packing, the A0 input pin must be inverted when using an 8-bit bus Intel type microprocessor (8088 for example).

A(1:7), D(0:7), D(8:15) pins :

1. With any 8-bit data bus, the D(0:7) and D(8:15) pins must be paired in order to demultiplex the low order data bytes and the high order data bytes.
2. When using address/data multiplexed bus, the D(0:7) pins are paired with A(0:7) in order to demultiplex data from address.

$\overline{AE}$, $\overline{DS}$, R/$\overline{W}$, $\overline{CS}$: See pin description.

III.3 - SOFTWARE RECOMMENDATIONS

1. The CONFIGURATION register R10 must be first initialized.
   The BW 15 flag is interpreted by the bus interface to recognize an 8-bit/16-bit data bus.
   The MB and BW 15 flags are used to decide when to initiate a command execution.
2. Each register byte has 4 addresses in the microprocessor memory map. These 4 addresses differ only by A(6:7). This scheme allows a 68008 programmer to read or write any data type (byte, word, long word) and automatically initiate or not a command execution at the end of this transfer. The transfer lasts one, two or four bus cycles.

A 68000 programmer is restricted to only word and long word data types (see Table 3).

Table 3 : Command Execution Condition

Address		Execution Condition	Data Type Transfer	
A7	A6		8-bit Data Bus	16-bit Data Bus
0	0	no Exec	Any Type	Any Type
0	1	Exec after a Bus Cycle	1 Byte	1 Word
1	0	Exec After 2 Bus Cycles	1 Word	1 Long Word
1	1	Exec after 4 Bus Cycles	1 Long Word*	ILLEGAL

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Notes : Word transfer must respect word boundary.
Long word transfer must respect long word boundary.
* Not available with 8088 MPU type.

IV - THE VIDEO TIMING GENERATOR RAM REFRESH AND DISPLAY PROCESS

IV.1 - Introduction

The Video Timing Generator is completely synchronous with the CLK input, which provides a pixel shift frequency (up to 18MHz). The Video Timing Generator :

- delivers the blanking signal (BLK), the horizontal (HS) and vertical (VS) synchronization signals on respective output pins,
- schedules the memory time allocated to the display process, dynamic RAM refresh and command execution,
- is fully programmable
- can be synchronized with an external composite video sync signal connected to the SYNC IN input.

IV.2 - Scan Parameters (see Table 4 and Figure 26)

IV.2.1 - TIMING UNITS

The time unit of any vertical parameter is the scan line.

The time unit of any horizontal parameter is the memory cycle, which is 8 periods of the CLK input signal.

These two parameters are internally programmed :

- Horizontal sync pulse duration = 7 cycles
- Vertical sync pulse duration = 2.5 lines.

IV.2.2 - BLANKING INTERVAL

The blanking interval starts :

- at the leading edge of the vertical sync pulse. Vertical blanking interval actual duration is 2.5 lines more than the programmed value.
- two cycles before the leading edge of the horizontal sync pulse. The actual horizontal blanking interval duration is 3 cycles more than the programmed value.

Note : During the programmed blanking interval, the video output pins P(0:3) are forced low.

IV.2.3 - PORCH AND MARGIN COLOR

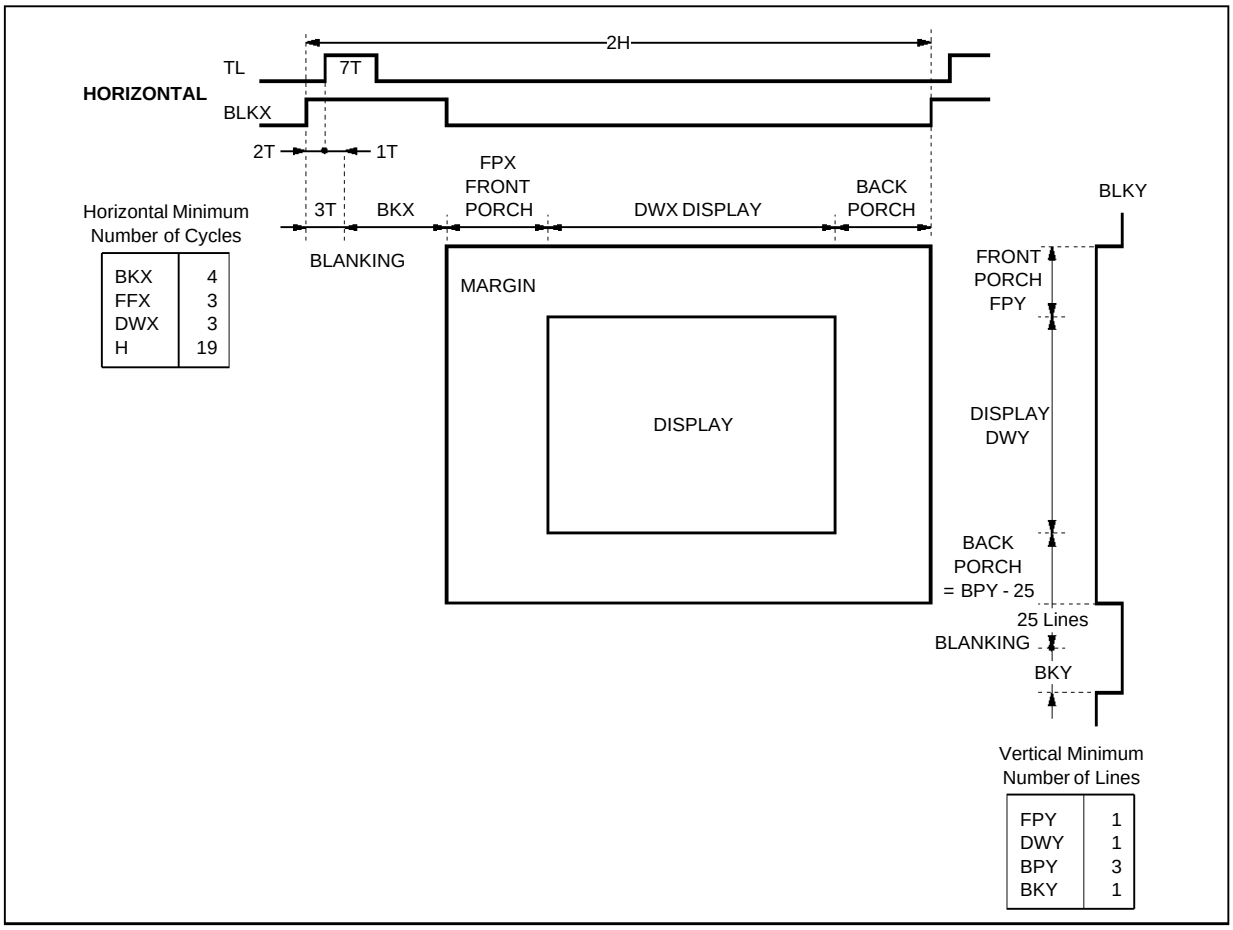
During the porch interval, the programmable margin color is displayed on the P(0:3) outputs.

The display process may be disabled by setting DPD flag. This will be interpreted as a porch extension.

Note : By process, the value of the block porch must be strictly above 0.

IV.2.4. MEMORY TIME SHARING (see Figure 16)

Figure 16 : Video Programming



The Video Timing Generator allocates memory cycles to either the display process, RAM refresh or command execution. In this respect, the scan lines per field are split between : the DWY displayable lines.

When VRE = 0, Video RAMs are not used.
The DWY x DWX cycles in the display interval are allocated to the display process when it is enabled (DPD = 0). When the display process is disabled, these cycles are allocated as for non displayable lines.

When VRE = 1, one cycle per display line is allocated to the display process. Other cycles are allocated as for non displayable lines. The last period of the BLKX signal may be used to load the internal video RAM shift register.

- the non displayable lines. In one out of nine non displayable lines, DWX cycles are allocated to the refresh process when it is enabled (RFD = 0).
- In Float cycle, an external X address must be provided. The Y address is still provided on ADM(0:7) and Y(0:2), while ADM(8:15) are in high impedance state.

IV.2.5. COMMAND ACCESS RATIO

This allocation scheme leaves about 50% of the memory bandwidth for command access when programming a standard TV scan. This ratio drops to the 30% range when a better monitor is in use (32µs out of 43µs displayable per line, 360 lines out of 390 for a 60Hz field rate). The higher resolution means more memory accesses in order to edit a given percentage of the screen area. In this case Video RAMs are very helpful to keep 90% of the memory bandwidth available for command access.

IV.3 - Display Process

The Video Timing Generator allocates memory cycles to the Display Processor in order to read the Display Viewport from memory. The Display Viewport upper left corner address is programmable through DIB, YOR and XOR. The display viewport dimensions are related to the display interval of DWY lines by DWX cycles per field.

IV.3.1 - Y ADDRESSES

When INE = 0, the fields are not interlaced. The Y Display Viewport address is initialized with YOR at the first displayable line then decremented by 1 at each scan line. The Display Viewport is thus DWY pel high.

When INE = 1, the fields are interlaced. The Y Display Viewport address is initialized as shown in the table below. It is then decremented by two at each scan line. The viewport is thus 2 x DWY pel high.

	Even Field	Odd Field
Yor Even	Yor	Yor + 1
Yor Odd	Yor – 1	Yor

Y display Viewport address initialization when INE = 1

IV.3.2 - X ADDRESSES AND MODX FLAGS

The X Display Viewport address is initialized with XOR at the first displayable cycle of each displayable line. It is then incremented at each subsequent cycle according to MODX flags.

MODX1	MODX0	X INCR	Video Shift Register	Memory Cycle Type
0	0	+ 1	Internal	Read
0	1	+ 1	External	Dummy Read
1	0	+ 2	External	Dummy Read
1	1		External	Float

In internal mode, the Display Viewport is 8. DWX pel wide. The on-chip video shift register are used.

In Dummy read, the memory is read but the on-chip video shift registers are not loaded, instead they retain their margin color. External video shift registers are presumed to be loaded by either 8 pels or 16 pels per cycle according to the programmed increment value.

In Float cycle, an external X address must be provided. The Y address is still provided on ADM(0:7) and Y(0:2), while ADM(8:15) are in high impedance state.

Note : See Memory Organization and Memory Timing for further details on the memory cycles.

IV.3.3 - THE VIDEO RAM CASE (VRE = 1)

In this case, the last cycle of the horizontal blanking interval is systematically allocated to the display process for DWY scan lines per field.

This cycle bears the scan line address, the bank number and the X address which is always XOR.

MODX must be programmed to use external shift register (Dummy read).

IV.3.4 - PAN AND TILT

The host can tilt or pan the Display Viewport through the frame buffer by modifying YOR or XOR arguments. Panning is performed on 8 pel boundaries.

IV.4. Dynamic Ram Refresh

No memory cycles are explicity allocated to the RAM refresh when RFD = 1.

When VRE = 0 and DPD = 0, the Display Process is supposed to be able to over-refresh dynamic components. This can be done by careful logical to component address mapping. During the remaining non displayable lines, the Display Viewport address continues to be incremented : Y address on each line according to INE, X address initialized by XOR then incremented according to MODX. This Display viewport address is allowed to address the memory for DWX cycles in only one line out of nine for refresh purposes.

When VRE = 1 or DPD = 1, any line is processed as a non displayable line with respect to the refresh process.

IV.5. Configuration and External Synchronization

The R10 register holds eight configuration flags. Six of these flags are dedicated to the Video Timing Generator.

- SSP : this flag selects the synchronization output pin configuration :
- NPC, NHVS, NBLK : these three flags invert the PC/HS, HVS/VS and BLK outputs respectively. (Ex. : When NBLK = 1 blanking is active high).

The SYNC IN input pin provides an external composite synchronization signal input from which a Vertical Sync In (VSI) signal is extracted. The SYNC IN signal is sampled on-chip at CLK frequency. Its rising sampled edge is compared to the leading edge of HS. A PC comparison signal is externally available (see SSP and NPC flags).

VSIE : this flag enables VSI to reset the internal line count.

HSIE : this flag enables the rising edge of SYNC IN to act directly on the Video Timing Generator. When the leading edge of HS does not match at 1 clock period a rising edge of SYNC IN, one extended cycle is performed (nine clock periods instead of eight).

Flag	Output Pins	
	PC/HS	HVS/VS
SSP = 1	HS	VS
SSP = 0	PC	HVS

Table 4

Name	Number of Bits	Mininmum Values	Register	Description	Function
DWY	10	1	R9	Number of Display lines per Field	Vertical Scan
INE	1		R8	Interlace Enable when INE = 1	
BKY	5	1	R8	Number of Lines in Vertical Blanking – 2.5	
FPY	5	1	R7	Number of Lines in Vertical Front Porch	
BPY	8	3	R6	Number of Lines in Vertical Back Porch + 2.5	
H	6	19	R6	Number of Double Cycles per Line	Horizontal Scan
FPX	4	3	R8	Number of Cycles in Horizontal Front Porch	
BKX	4	4	R8	Number of Cycles in Horizontal Blanking – 3	
DWX	7	3	R7	Number of Cycles of the Display Window	
XOR	8		R4	X, Y, and bank logical address in the display memory of the display viewport upper left corner	Display Process
YOR	11		R5		
DIB	2		R4		
MODX	2		R9	Selection of the X Addressing Mode	
MC	4		R4	Margin Color	
RFD	1		R7	RAM Refresh Disable when RFD = 1	Memory Time Sharing
DPD	1		R7	Display Process Disable when DPD = 1	
VRE	1		R8	Video RAM Enable When VRE = 1	

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Note : one cycle = 8 periods of CLK Clock

V. MEMORY ORGANIZATION

V.1 - Introduction

The display memory is logically organized as four banks of 4-bit planes. Thus a bit address in the display memory is given by the quadruplet :

- B = bank number, from 0 to 3
- Z = plane number, from 0 to 3
- X = bit address into the plane, from 0 to 2047
- Y = bit address into the plane, from 0 to 2047.

In one memory cycle (8 CLK periods), the controller can access a memory word. This 32-bit memory word holds one byte from each plane in a given bank. In order to address this memory word, the controller supplies :

- B(0:1) : binary value of the bank number
- X(3:10) : binary value of the word address
- Y(0:10) : binary value of the word address.

Z and X(0:2) are not supplied. They give only a bit address in a memory word.

V.2 - Memory Cycles

24 pins are dedicated to the memory interface.

- ADM(0:15) : these 16 bidirectional pins are multiplexed three times during a memory cycle (see Figure 25) :
  - TA : address period. Output of the X(3:11) and Y(3:11) address
  - TO : even data period. The even Z bytes are either input or output.
  - T1 : odd data period. The odd Z bytes are either input or output.
  - Y(0:2) : three LSB Y address output pins (non-multiplexed)
  - B(0:1) : two bank address output pins (non-multiplexed)
- CYS : Cycle start strobe output (non-multiplexed). CYS is at CLK/8 frequency. A CYS pulse is delivered only when a command, display or refresh cycle is performed.
- CYF(0:1) : Two cycle status outputs (non-multiplexed). Four cycle types are defined : Command Read, Command Write, RAM Refresh, Display Access.

Because several options may be selected for RAM refresh and display access by the MODX and VRE flags (see Video Timing Section), there are more than four memory cycle types (see Figure 25 and Table 5).

V.3 - Display Memory Desing Overview

The display memory implementation is application dependant. The basic parameters are :

- the number of pixels to be displayed Nx.Ny
- the number of bits per pel
- the vertical scanning frequency, which must be picked in the 40Hz to 80Hz range (non interlaced) or in the 60Hz to 80Hz range (interlaced).

This yields a rough estimate of the pixel frequency. When the pixel frequency is in the 15 to 18MHz range and 4 bits per pixel or least are required, the on-chip video registers and standard dynamic RAM components may be used. When higher pixel rates

or up to 8 bits per pixel are required, the designer must provide external shift registers. Video RAM components may also be considered.

In either case, the user must design :

- A memory block. This is the hardware memory building block. It includes the video shift registers if on-chip VSR cannot be used. It implies a RAM component choice.
- An Address Mapper, which maps the logical address into hardware address : block selection, Row Address (RAD), Column Address (CAD).
- A memory cycle controller. This controller monitors the CYF and CYS output pins from TS68483 and block address from the Mapper. It provides :
  - The CLK signal to the TS68483 and a shift clock SCLK when external video shift registers are used
  - $\overline{RAS}$, $\overline{CAS}$, $\overline{OE}$, R/$\overline{W}$ signals to the memory blocks
  - RAD and CAD Enable signals to the Mapper.

V.3.1 - FRAME BUFFER (see Table 6)
A byte wide organization of each bit plane is required. Obviously a bit plane must contain the Display Viewport size. A straight organization implements only one bit plane per block.

It may be cost effective to implement several bit planes per block. Two basic schemes may be used :

- One block, one Z : several bit planes, belonging to different banks, but addressed by the same Z, share a given block. There is little time constraint if any.
- One block, two Z : two bit planes, belonging to the same bank share a given block. In this case, this block must be accessed twice during a memory cycle. This can be solved by two successive page mode accesses.

Table 5 : Memory Cycle Types

Output Pins		Function	Modx Flags		Multiplexed ADM			Cycle Type
CYF1	CYF0		1	0	TA	TO	T1	
1	0	Command Read			Y,X	Z0,Z2	Z1,Z3	Read
1	1	Command Write			Y,X	Z0,Z2	Z1,Z3	Write
0	1	Display	0 0	0 1	Y,X Y,X	Z0,Z2	Z1,Z3	Read Dummy Read + 1
0	0	Refresh	1 1	0 1	Y,X Y,Hi-Z			Dummy Read + 2 Float X

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Refresh : dummy read cycle is performed.

Table 6 : Frame Buffer Organization

Typical Block Size	16 k x 8	32 k x 8	64 k x 8	256 k x 8
One Block-one Bit Planes	512 x 256	512 x 512	1024 x 512	2048 x 1024
One Block-two Bit Planes	256 x 256	512 x 256	512 x 512	

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COMPONENTS : 64K BITS : 16K x 4 or 64K x 1
256K BITS : 32K x 8, 64K x 4, 256K x 1
VIDEO RAM : 64K x 1, 64K x 4

Table 7 : The Multiplexing Scheme

HIGHER BYTES

ADMS Multiplexed Pins	15	14	13	12	11	10	9	8
TA : Address Period	10			X				3
T0 : Even Z Byte Period	7			Z = 2				0
T1 : Odd Z Byte Period	7			Z = 3				0

LOWER BYTES

ADMS Multiplexed Pins	7	6	5	4	3	2	1	0
TA : Address Period	10			Y				3
T0 : Even Z Byte Period	7			Z = 0				0
T1 : Odd Z Byte Period	7			Z = 1				0

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Figure 17 : One Block - One Z

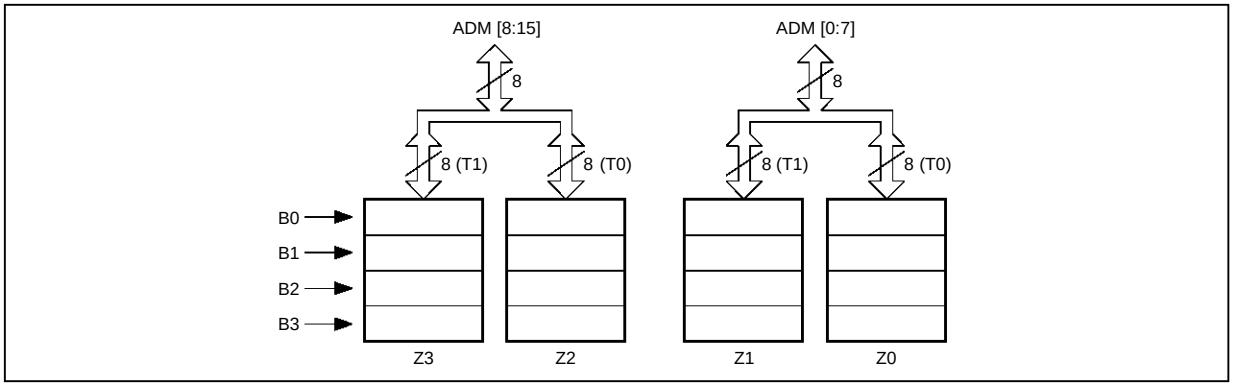


Figure 18 : One Block - Two Z

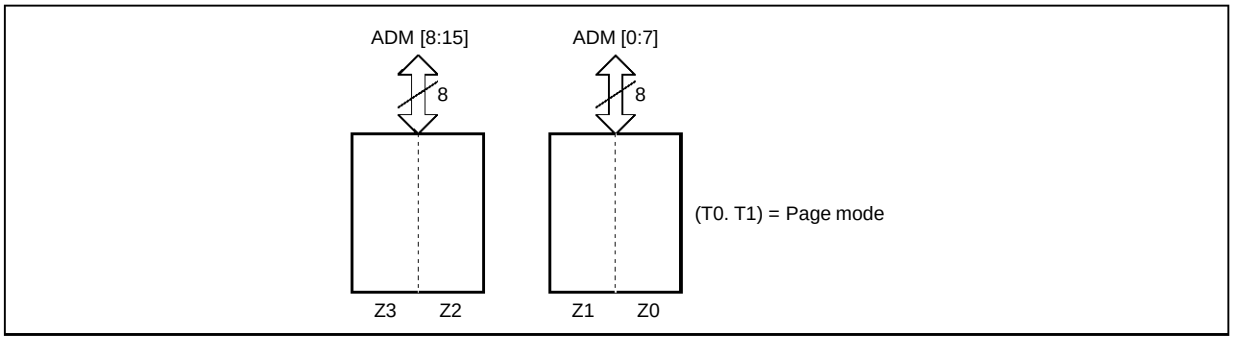
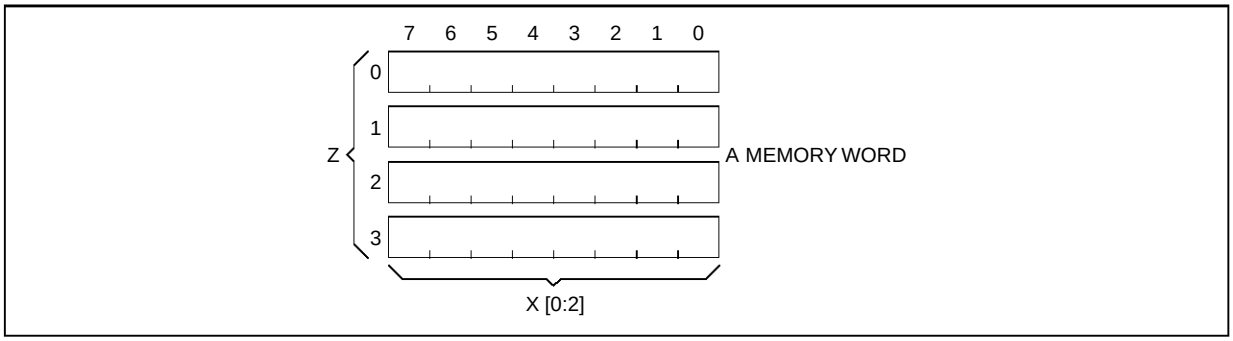


Figure 19



V.3.2 - MASKING PLANES
Masking planes are very useful for general purpose area filling or clipping. It may be practical to use one or two planes smaller than the color bit plane if they cyclically cover a frame buffer.

The masking planes must be in bank 3.

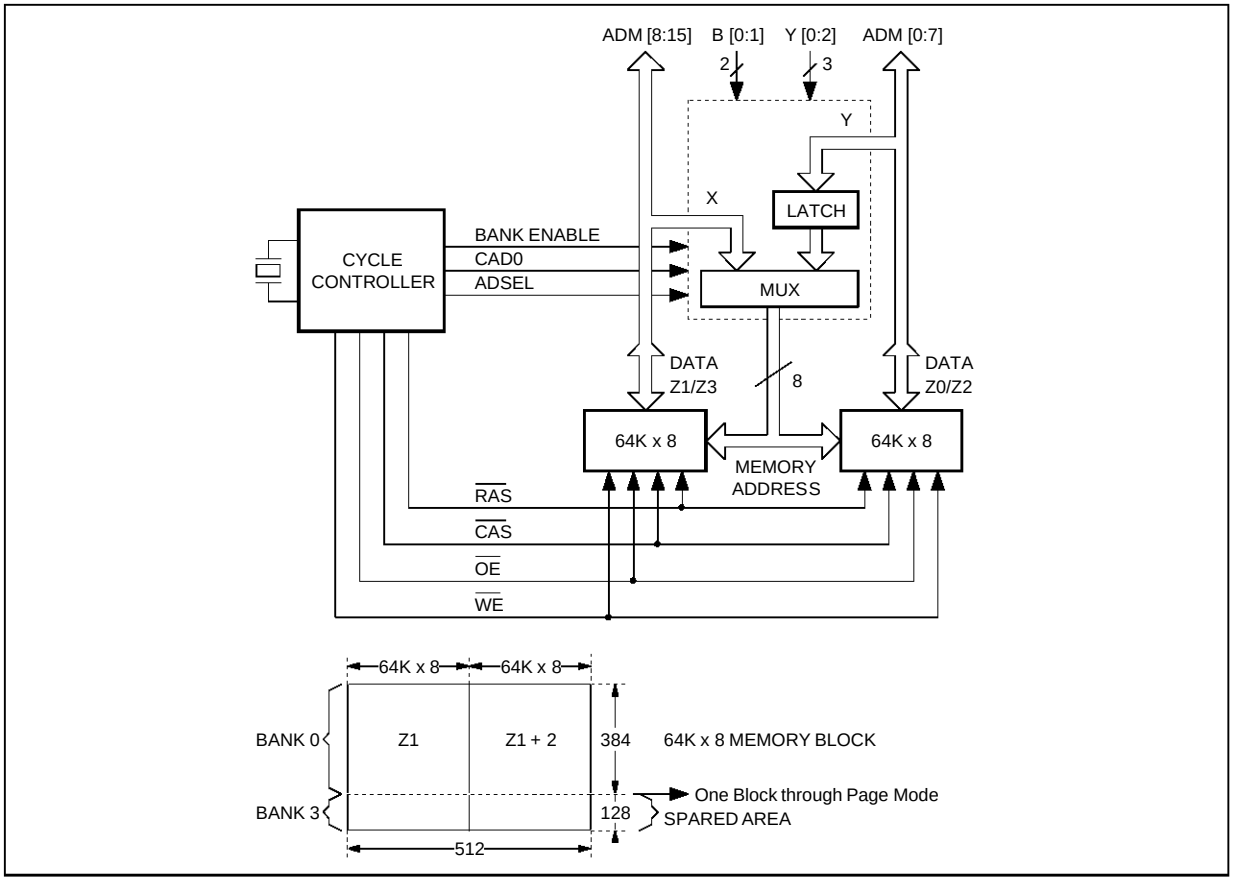
V.3.3 - OBJECTS AND CHARACTERS
Objects may be located in unused parts of the frame buffer.

Character generators can be implemented in any plane of any bank. They can also be implemented in ROM. In this case, plane Z = 1 or 3 offer relaxed access time requirements.

V.4 - Examples

Figure 20. gives the schematic for a 512 x 384 non interlaced application. A CLK signal in the 15 to 18 MHz range should produce a 50 to 60Hz refresh rate. The on-chip video shift registers may be used if no more than four bits per pixel are required. One 64 K x 8 memory block may be implemented using either eight 64 K x 1 or two 64 K x 4 components. One memory block holds two 512 x 384 color bit planes.

Figure 20 : Memory Organization for 512 x 384 Application



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VI - TIMING DIAGRAM

VI.1 - Microprocessor Interface

TS68483 has an eight bit address bus and a sixteen bit data bus. Little external logic is needed to adapt bus control signals from most of the common multiplexed or non-multiplexed bus microprocessors.

UNMUX MODE

Microprocessor Interface Timing : A(0:7), D(0:15), AE, $\overline{DS}$, $\overline{CS}$, R/$\overline{W}$

V_{CC} = 5.0V ± 5%, $T_A = T_L$ to T_H, C_L = 100pF on D(0:15)

Reference levels : V_{IL} = 0.8V and V_{IH} = 2V on all inputs, V_{OL} = 0.4V and V_{OH} = 2.4V on all outputs

Indent Number	Parameter	Min.	Max.	Unit
1	Address Set up Time from $\overline{CS}$	0		ns
2	Data Strobe Width (high)	65		ns
3	$\overline{AS}$ Set up Time from $\overline{CS}$	0		ns
4	Data Strobe Width-low (read cycle)	160		ns
5	Address Hold Time from $\overline{DS}$	0		ns
6	Data Access time from $\overline{CS}$ (read cycle)		130	ns
7	$\overline{DS}$ Inactive to High Impedance State (read cycle)	10	80	ns
8	R/$\overline{W}$ Set up Time from $\overline{DS}$	20		ns
9	$\overline{DS}$ Width-low (write cycle)	80		ns
10	$\overline{CS}$ Set up Time from $\overline{DS}$ Active (write Cycle)	0		ns
11	Data in Set up Time from $\overline{DS}$ active (write cycle)	10		ns
12	Data in Hold Time from $\overline{DS}$ Inactive (write cycle)	15		ns

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Figure 21 : Read Cycle

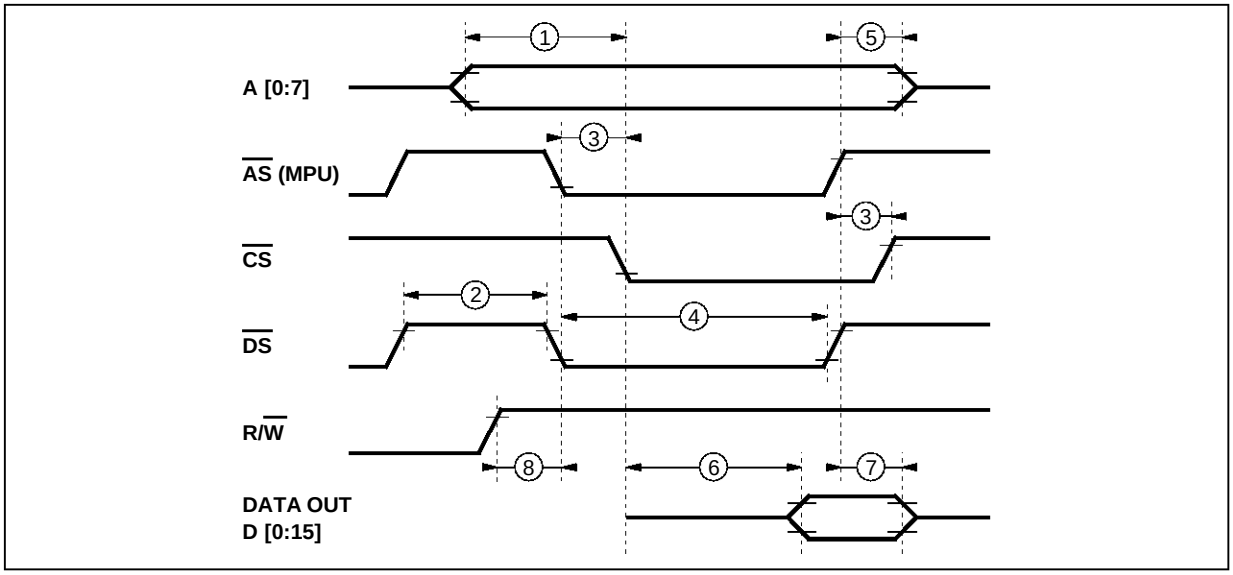
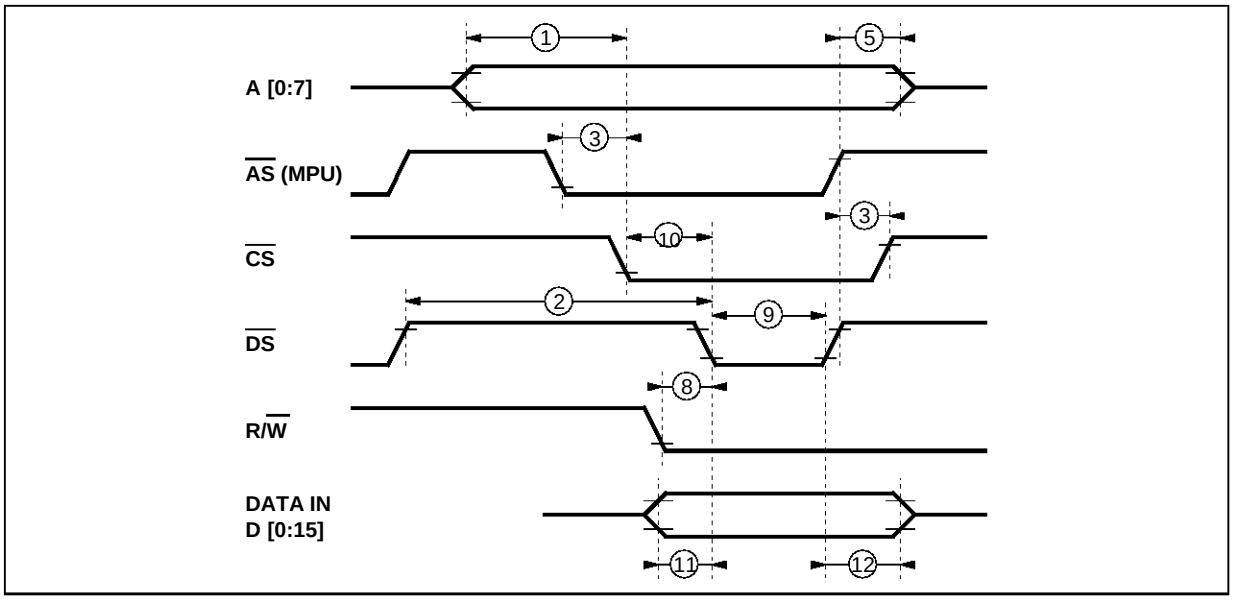


Figure 22 : Write Cycle



MUX MODE

Microprocessor Interface Timing : A (0 : 7), D (0 : 15), AE, $\overline{DS}$, $\overline{CS}$, R/$\overline{W}$

V_{CC} = 5.0V ± 5 %, T_A = T_L to T_H, C_L = 10 pF on D (0 : 15)

Reference Levels : V_{IL} = 0.8V and V_{IH} = 2V on All Inputs, V_{OL} = 0.4V and V_{OH} = 2.4V on All Outputs

Indent Number	Parameter	Min.	Max.	Unit
1	AE Width High	90		ns
2	Address Set up Time to AE Inactive	55		ns
3	Address and $\overline{CS}$ Hold Time to AE Inactive	55		ns
4	$\overline{CS}$ Set up Time to AE Inactive	40		ns
5	$\overline{DS}$ and R/$\overline{W}$ High	150		ns
6	$\overline{DS}$ Width-low (read)	240		ns
7	R/$\overline{W}$ Width-low (write)	110		ns
8	Data Access Time From $\overline{DS}$ (read)		210	ns
9	Data in Set up time from R/$\overline{W}$ Inactive (write)	150		ns
10	$\overline{DS}$ Inactive to High Impedance State (read)	10	100	ns
11	Data in Hold Time from R/$\overline{W}$ Inactive (write)	30		ns
12	AE Inactive to $\overline{DS}$ Active	20		ns
13	AE Inactive to R/$\overline{W}$ Active	20		ns
14	$\overline{DS}$ Inactive to AE Active	10		ns
15	R/$\overline{W}$ Inactive to AE Active	10		ns
16	R/$\overline{W}$ Inactive to Next Address Valid	100		ns
17	$\overline{DS}$ Inactive to Next Address Active	100		ns
18	Data in Set up Time from R/$\overline{W}$ Active (fast write cycle)	10		ns

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Figure 23 : Read Cycle

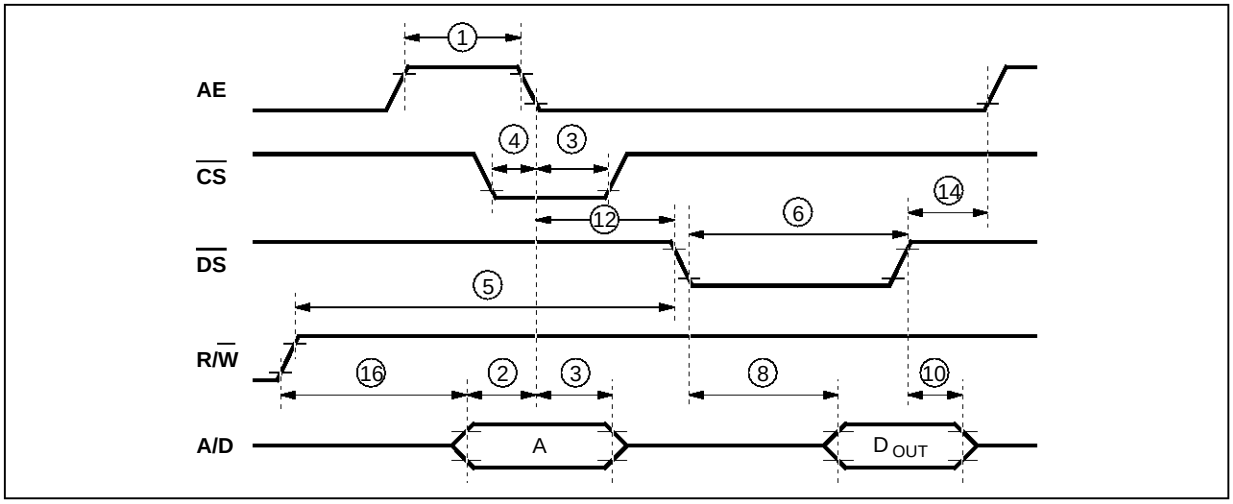
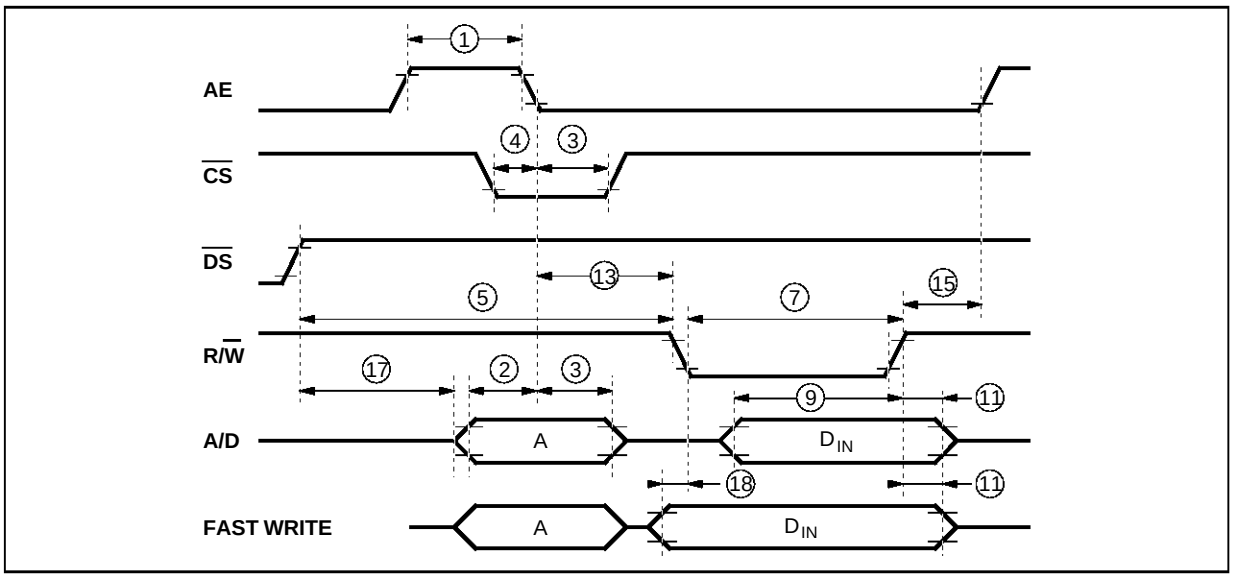


Figure 24 : Write Cycle



VI.2 - Memory Interface

ADM (0 : 15), B (0 : 1), CYF (0 : 1), Y (0 : 2), CYS
V_{CC} = 5.0V ± 5 %, $T_A = T_L$ to T_H, CLK Duty Cycle = 50 %, Period T
Reference Levels : V_{IL} = 0.8V and V_{IH} = 2V, V_{OL} = 0.4V and V_{OH} = 2.4V

Indent Number	Parameter	Min.	Max.	Unit
1	TCLK Clock Period	55	166	ns
2	Memory Cycle Time (T = 8 X T_{CLK})			ns
3	Output Delay Time from CLK		35	ns
4	Output Data HI-Z Time from CLK		35	ns
5	Output Hold Time from CLK	10		ns
6	Input Data Hold Time from CLK (read cycle)	6		ns
7	Input Data Set up Time from CLK (read cycle)	10		ns
8	Input Data HI-Z Time from CLK		T_{CLK}	ns

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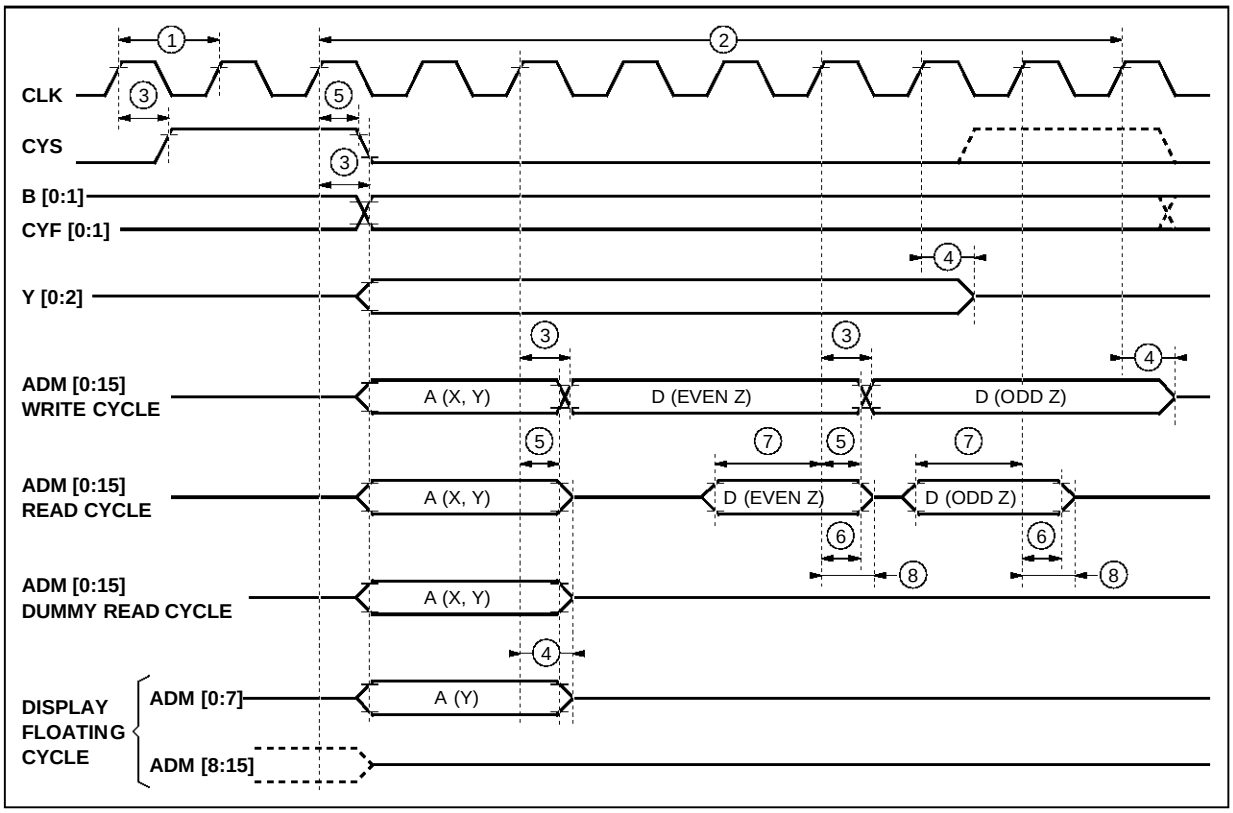
Note : All timing is referenced to the rising edge of CLK (see timing diagram 3).

Figure 25 : Memory Interface



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VI.3 - Video Interface

P0, P1, P2, P3, BLK, HVS/VS, PC/HS

V_{CC} = 5.0V ± 5 %, T_A = T_L to T_H, CLK duty cycle = 50%

Reference levels : V_{IL} = 0.8V and V_{IH} = 2V, V_{OL} = 0.4V and V_{OH} = 2.4V, C_L = 50pF

Indent Number	Parameter	Min.	Max.	Unit
1	TCLK : CLK Period	55	166	ns
2	CLK High Pulse Width	23		ns
3	Output Delay from CLK Rising Edge		30	ns
4	CLK Low Pulse Width	23		ns
5	Output Hold Time	10		ns

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Figure 26 : Timing Diagram

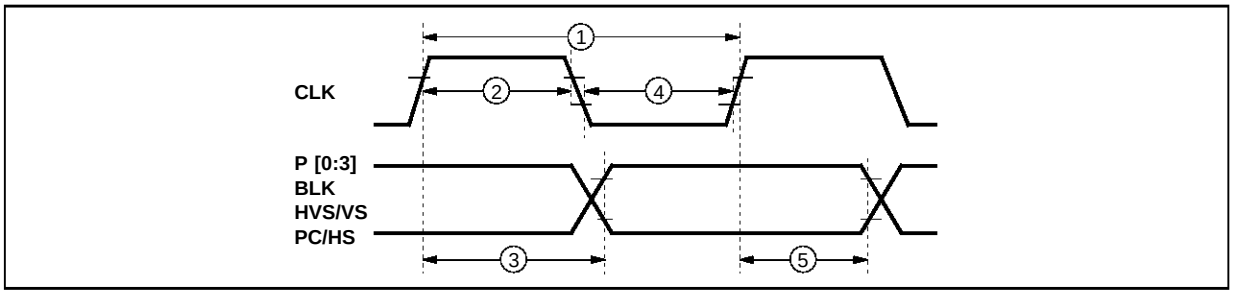

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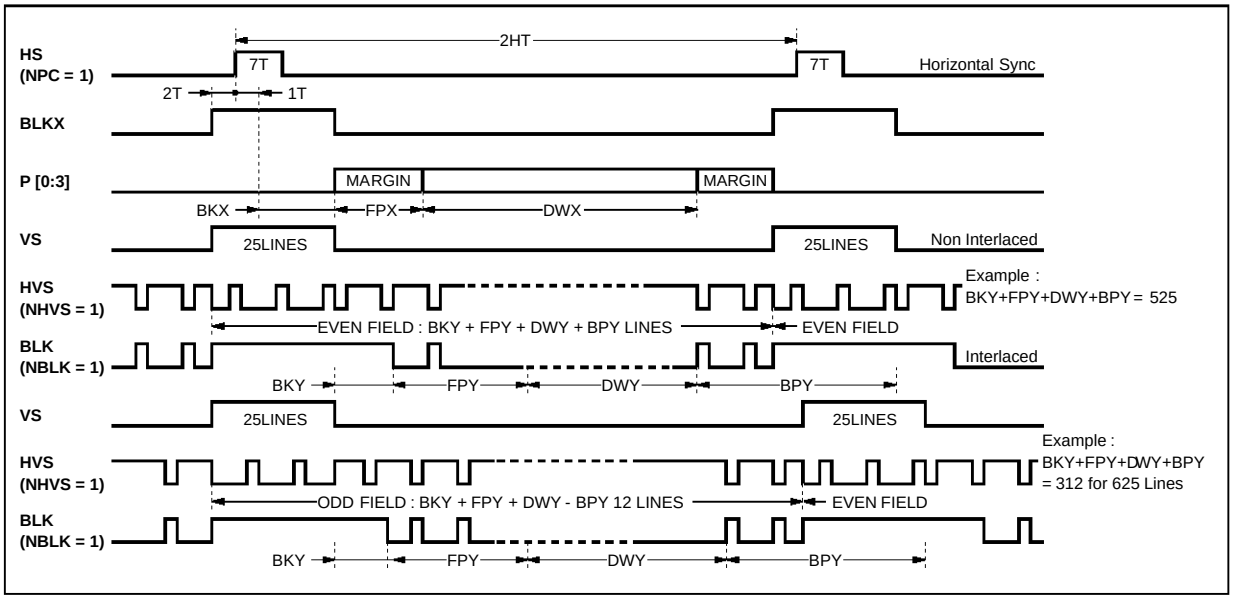
Figure 27 : Synchronization Signal Outputs



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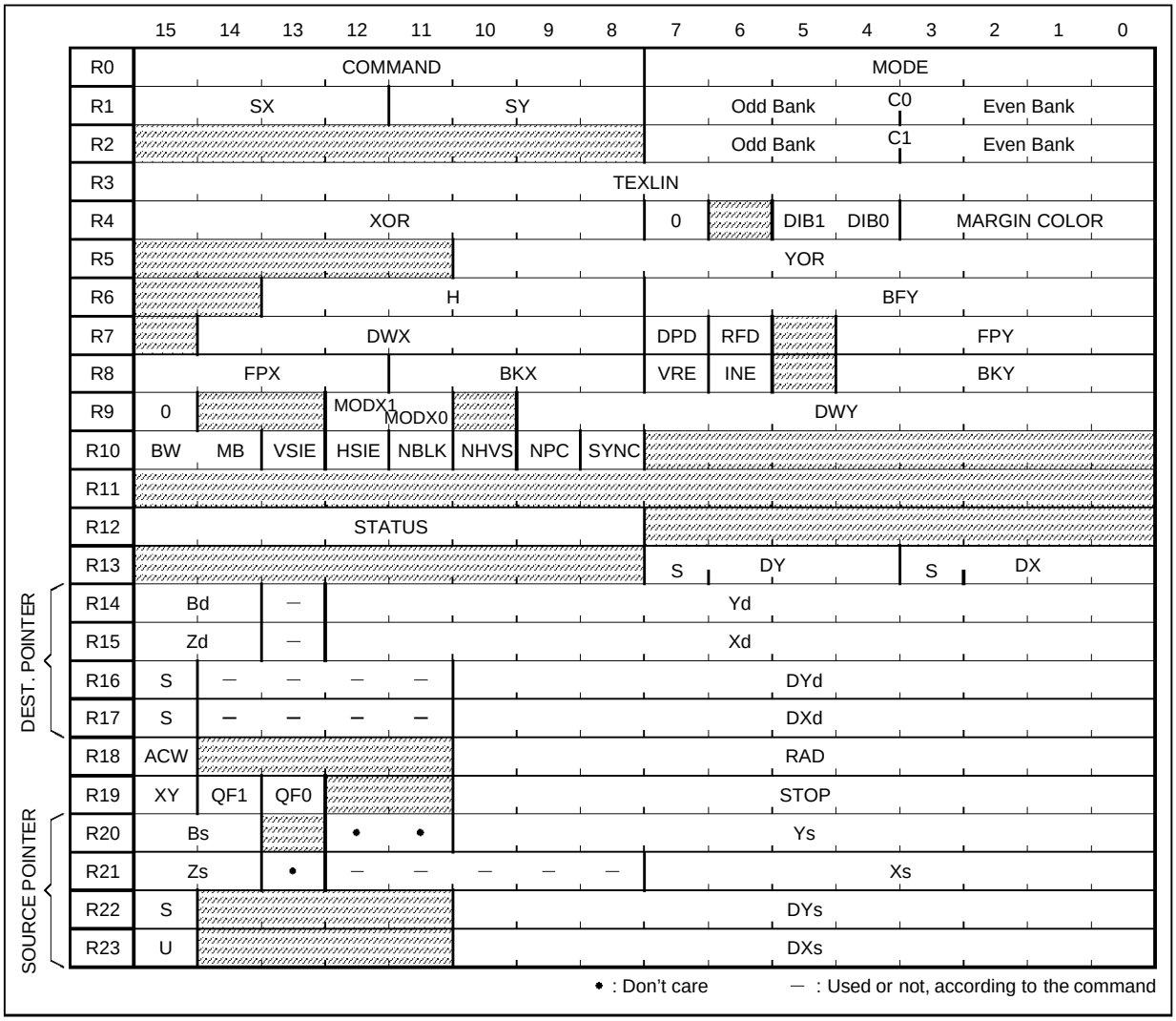
VII - TABLES

VII.1 - Register Map and Command Table

Figure 28



TYPE			MNEM	CODE			PARAMETERS					ARGUMENTS								POINTERS								END COMMAND CURSOR POSITION		EXECUTION TIME		
				7	6	5	4	3	2	1	0	R0	R1	R2	R3	R13	R18	R19	R14	R15	R16	R17	R20	R21	R22	R23			INIT	LOOP	Per
DRAWING	LINEPAR	DOT LINE	DLI	0	0	0	0	0	DMU	SP	SRU	X	X	X	X	X			X	X	X	X					Xd + DXd	Yd + DYd	5T	4T	DOT
		PEN LINE	PLI	0	0	0	POL	PEN	DMU	SP	SRU	X	X	X	X	X			X	X	X	X	X	X	X	X	Xd + DXd	Yd + DYd	5T	CELL + 4T	CELL
		DOT ARC	DAR	0	0	1	0	0	DMU	SP	SRU	X	X	X	X	X	X	X	X	X	X	X					XF	YF	15T	10T	DOT
		PEN ARC	PAR	0	0	1	POL	PEN	DMU	SP	SRU	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	XF	YF	15T	CELL + 10T	CELL
	AREA	RECTANGLE	REC	1	1	1	1	0	DMU	SP	SRU	X	X	X		X			X	X	X	X					Xd	Yd + DYd	10T	4T	AREA MEMORY WORD
		TRAPEZIUM	TRA	0	1	0	1	0	DMU	SP	SRU	X	X	X		X			X	X	X	X		X			Xd + DXd	Yd + DYd	10T	4T (see Note 1)	
		POLYGON	FLL	0	1	0	1	0	DMU	SP	SRU	X	X	X		X			X	X	X	X					Xd + DXd	Yd + DYd	10T		
		POLYARC	FLA	0	1	1	0	BEG	DMU	SP	SRU	X	X	X		X	X	X	X	X	X	X					XF	YF	15T		
	CELL	PRINT CHARACTER	PCA	1	0	1	0	BEG	DMU	SP	SRU	X	X	X		X			X	X	X	X	X	X	X	X	Xd + DXd	Yd	4T	6T	MEMORY WORD
		PRINT OBJECT	PVS	1	0	0	1	REP	DMU	SP	SRU	X	X			X			X	X	X	X	X	X	X	X	Xd + DXd	Yd			
			PVF	1	0	1	SMU	REP	DMU	1	SRU	X	X			X			X	X	X	X	X	X	X	X	Xd + DXd	Yd			
ACCESS		LOAD VIEWPORT	LDV	1	1	1	0	REP	DMU	1	SRU								X	X	X	X	X	X	X	X	Xs	Ys	2T	5T	MEMORY WORD
		SAVE VIEWPORT	SAV	1	1	1	0	XFT	0	0	INC								X	X	X	X	X	X	X	X	Xs	Ys	2T	4T	
		MODIFY VIEWPORT	RMV	1	1	1	0	XFT	0	1	INC								X	X	X	X	X	X	X	X	Xs	Ys	2T	10T	
CURSOR		UP-DOWN MOVE	UDM	1	1	0	0	XFT	1	0	INC					X			X	X	X						Xd	Yd + DYd	3T		
		LEFT-RIGHT MOVE	LRM	1	1	0	0	0	1	DWN	SRU					X			X	X		X					Xd + DXd	Yd	3T		
		DIAGONAL MOVE	CDM	1	1	0	1	LEF	0	0	SRU					X			X	X	X	X					Xd + DXd	Yd + DYd	4T		
CONTROL		NO OPERATION	NOP	1	1	0	0	0	0	0	0																		1T		
		ABORT	BRT	1	1	1	1	1	1	1	1																		1T		

DMU = 1 : Destination mask use.

SP = 1 : Short pel ; long pel when SP = 0.

SRU = 1 : Short relative register use (R13).

PEN =0 : The pen is a single pel.

PEN = 1 : POL = 0 : the pen is the character cell addressed by the source ponter.
POL = 1 : the pen is the object associated with a source mask addressed by the source pointer.

BEG = 1 : Initate a polygon or polyarc filling.
This parameter should be reset only when the second drawing is not identical to the first one (Ex : first polygon, the polyarc).

INC = 0 : The source pointer is not auto-incremented, X direction first.

INC = 1 : XFT = 1 : the source pointer is auto-incremented, X direction first.
XFT = 0 : the source pointer is auto-incremented or auto-decremented, Y direction first.

REP = 1 : The cell is stepped and repeated through the destination window.
When REP = 0, only one cell is printed.

SMU = 1 : The source mask is used.

DWN = 1 : The cursor is mved down (up if DWN = 0).

LEFT = 1 : The cursor is mved left (right if LEF = 0).

Note : With PVF command, any pel with color different from 0 has its source mask implicity set and used.
In other words, pels with color value 0 are transparent.
- DXd, DYd and DYs are signed values.
- DXs is always positive.
- T = memory cycle = 8 CLK clock periods.
- For execution time, add to the short pel loop in the table :
  - 1T if DMU = 1
  - 1T if SMU = 1
  - 2T if long pen are used
  - 2T if mask printing is required.

Command execution is performed only out of the display periods.

Note 1 : For FLL and FLA commands, add 4T and 8T respectively per pel belonging to the boundary.

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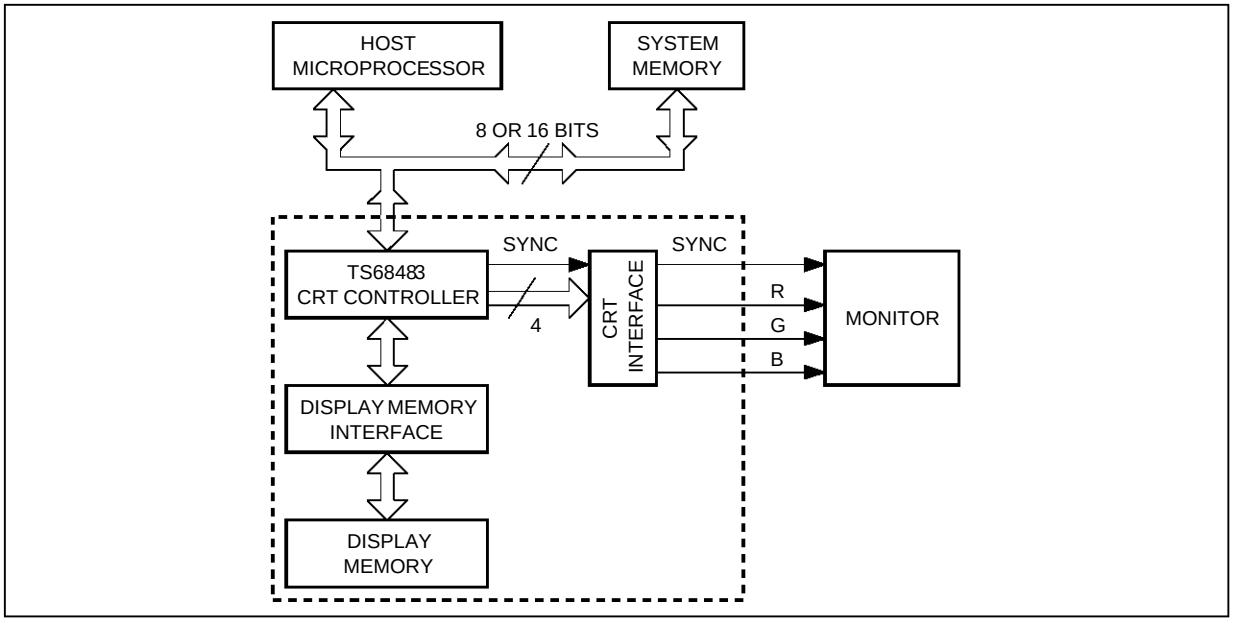
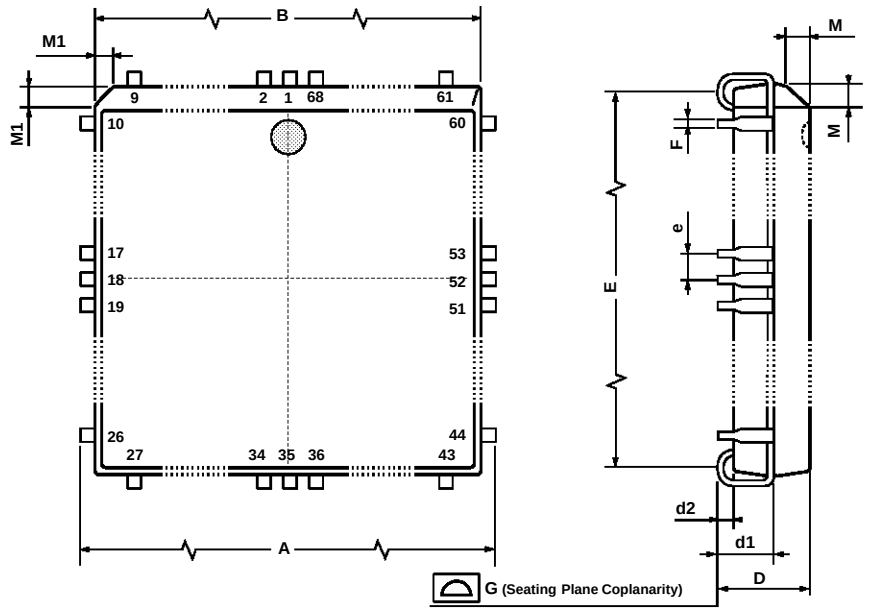
Figure 29 : Typical Application



PACKAGE MECHANICAL DATA

68 PINS - PLASTIC CHIP CARRIER



PMPLCC68.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	25.02		25.27	0.985		0.995
B	24.13		24.33	0.950		0.958
D	4.2		5.08	0.165		0.200
d1		2.54			0.100	
d2		0.56			0.022	
E	22.61		23.62	0.890		0.930
e		1.27			0.050	
F		0.38			0.015	
G			0.101			0.004
M		1.27			0.050	
M1		1.14			0.045	

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