

PROGRAMMABLE TIMER/COUNTER

The μ PD71054 is a high-performance programmable timer/counter designed for timing control applications in microcomputer systems. The μ PD71054 is fabricated by CMOS technology in order to realize low power consumption.

The μ PD71054-10 is the latest and the fastest version, which can be directly configured with top-of-line processors such as the μ PD70108-10 and the μ PD70116-10.

FEATURES

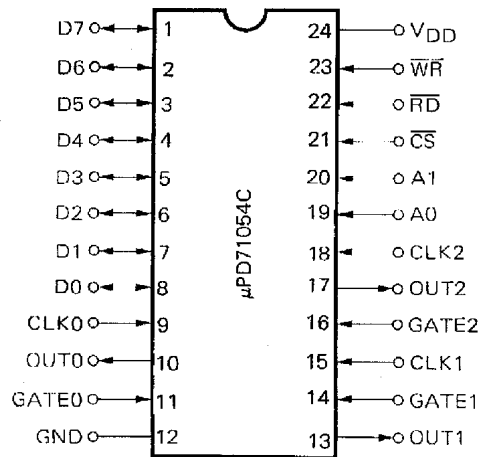
- Compatible with μ PD70108 (V20TM), μ PD70116 (V30TM), μ PD70208 (V40TM), & μ PD70216 (V50TM)
- Three independently-operated 16-bit counters
- Six count modes available for each counter
- Binary/BDC count operation
- Multiple latch command for easy monitoring
- Count rate: 0 (DC) to 8 MHz; μ PD71054
0 (DC) to 10 MHz; μ PD71054-10
- CMOS
- +5 V single power supply

ORDERING INFORMATION

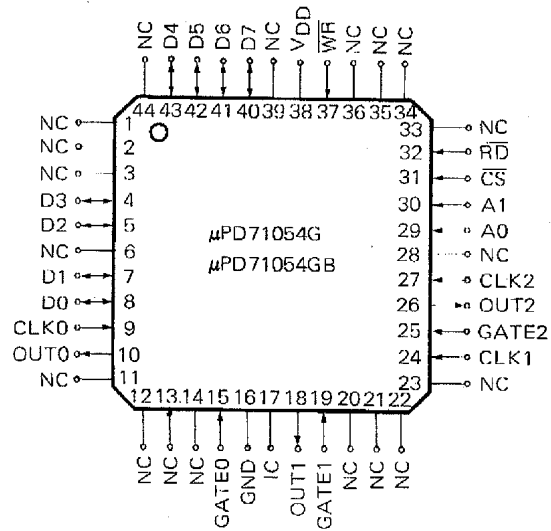
Ordering Code	Package	Speed
μ PD71054C	24-pin plastic DIP (600 mil)	8 MHz
μ PD71054C-10	24-pin plastic DIP (600 mil)	10 MHz
μ PD71054G	44-pin plastic QFP (1.45 mm thick)	8 MHz
μ PD71054GB-3B4	44-pin plastic QFP (2.70 mm thick)	8 MHz
μ PD71054GB-10-3B4	44-pin plastic QFP (2.70 mm thick)	10 MHz
μ PD71054L	28-pin PLCC	8 MHz
μ PD71054L-10	28-pin PLCC	10 MHz

PIN CONFIGURATION (Top View)

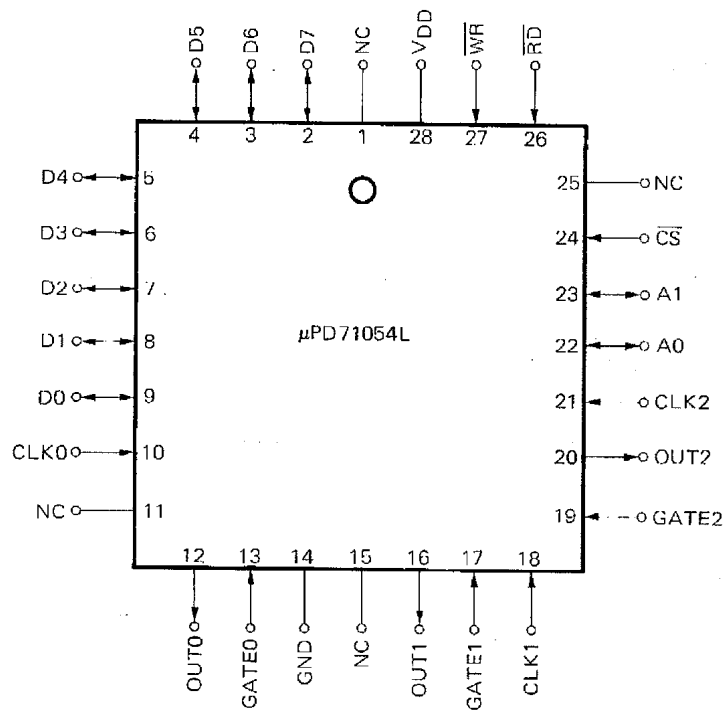
24-pin plastic DIP



44-pin plastic QFP



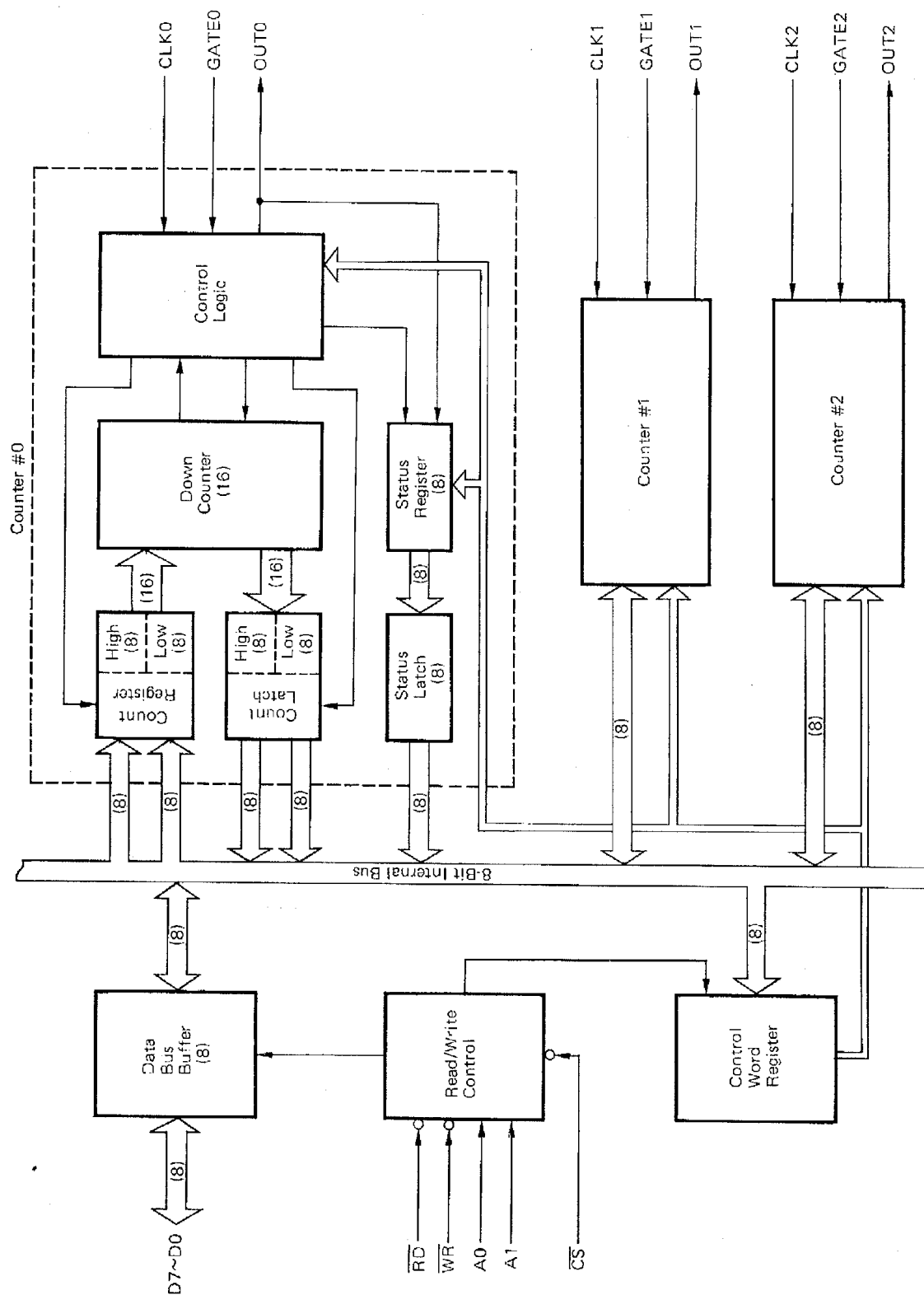
28-pin PLCC



PIN IDENTIFICATION

- D7 to D0 : Data Bus (8 bits)
- CLK_n : Counter Clock Input
- OUT_n : Counter Output
- GATE_n : Counter Gate Input
- A1, A0 : Address
- $\overline{CS}$: Chip Select
- $\overline{RD}$: Read Strobe
- $\overline{WR}$: Write Strobe
- VDD : Power
- GND : Ground

BLOCK DIAGRAM



NOTE:

The internal architecture of counters #1 and #2 is the same as counter #0's.

6. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings ($T_a = 25^\circ\text{C}$)

Power Supply Voltage	V_{DD}	-0.5 to +7.0	V
Input Voltage	V_I	-0.5 to $V_{DD} + 0.3$	V
Output Voltage	V_O	-0.5 to $V_{DD} + 0.3$	V
Operating Temperature	T_{opt}	-40 to +85	$^\circ\text{C}$
Storage Temperature	T_{stg}	-65 to +150	$^\circ\text{C}$

DC Characteristics ($T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{DD} = +5\text{ V} \pm 10\%$)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Condition
Input High Voltage	V_{IH}	2.2		$V_{DD} + 0.3$	V	
Input Low Voltage	V_{IL}	-0.5		0.8	V	
Output High Voltage	V_{OH}	$0.7 \times V_{DD}$			V	$I_{OH} = -400\ \mu\text{A}$
Output Low Voltage	V_{OL}			0.4	V	$I_{OL} = 2.5\text{ mA}$
Input Leakage High	I_{LIH}			10	μA	$V_I = V_{DD}$
Input Leakage Low	I_{LIL}			-10	μA	$V_I = 0\text{ V}$
Output Leakage High	I_{LOH}			10	μA	$V_O = V_{DD}$
Output Leakage Low	I_{LOL}			-10	μA	$V_O = 0\text{ V}$
Supply Current	I_{DD1}			30	mA	$\mu\text{PD71054}$ (at 8 MHz)
			10	20		$\mu\text{PD71054-10}$ (at 10 MHz)
	I_{DD2}		2	50	μA	Standby Mode: Input Pins; $V_{IH} = V_{DD} - 0.1\text{ V}$ $V_{IL} = 0.1\text{ V}$ Output Pins; Open

Capacitance ($T_a = 25^\circ\text{C}$, $V_{DD} = 0\text{ V}$)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Condition
Input Capacitance	C_{IN}			10	pF	$f_c = 1\text{ MHz}$
I/O Capacitance	$C_{I/O}$			20	pF	Unmeasured pins returned to 0 V

AC Characteristics ($T_a = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{DD} = 5\text{V} \pm 10\%$)

Read Cycle

Parameter	Symbol	μPD71054		μPD71054-10		Unit	Condition
		MIN.	MAX.	MIN.	MAX.		
Address Setup Time (Against $\overline{\text{RD}}\downarrow$)	t_{SAR}	30		20		ns	
Address Hold Time (Against $\overline{\text{RD}}\uparrow$)	t_{HRA}	10		0		ns	
$\overline{\text{CS}}$ Setup Time (Against $\overline{\text{RD}}\downarrow$)	t_{SCR}	0		0		ns	
$\overline{\text{RD}}$ Pulse Width	t_{RRL}	150		95		ns	
Data Delay Time (From $\overline{\text{RD}}\downarrow$)	t_{DRD}		120		85	ns	$C_L = 150\text{ pF}$
Data Float Time (From $\overline{\text{RD}}\uparrow$)	t_{FRD}	10	85	10	65	ns	$C_L = 20\text{ pF}$, $R_L = 2\text{ k}\Omega$
Data Delay Time (From Address)	t_{DAD}		220		185	ns	$C_L = 150\text{ pF}$
Read Recovery Time	t_{RV}	200		165			

Write Cycle

Parameter	Symbol	μPD71054		μPD71054-10		Unit	Condition
		MIN.	MAX.	MIN.	MAX.		
Address Setup Time (Against $\overline{\text{WR}}\downarrow$)	t_{SAW}	0		0		ns	
Address Hold Time (Against $\overline{\text{WR}}\uparrow$)	t_{HWA}	0		0		ns	
$\overline{\text{CS}}$ Setup Time (Against $\overline{\text{WR}}\downarrow$)	t_{SCW}	0		0		ns	
$\overline{\text{WR}}$ Pulse Width	t_{WWL}	160		95		ns	
Data Setup Time (Against $\overline{\text{WR}}\uparrow$)	t_{SDW}	120		95		ns	
Data Hold Time (Against $\overline{\text{WR}}\uparrow$)	t_{HWD}	0		0		ns	
Write Recovery Time	t_{RV}	200		165		ns	

AC Characteristics (Continued)

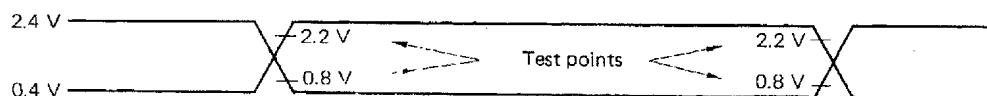
CLK & GATE Timing

Parameter	Symbol	μ PD71054		μ PD71054-10		Unit	Condition
		MIN.	MAX.	MIN.	MAX.		
Clock Cycle Time	t_{CLK}	125	DC	100	DC	ns	
CLK High Level	t_{KKH}	60		30		ns	
CLK Low Level	t_{KKL}	60		45		ns	
CLK Rise Time	t_{KR}		25		25	ns	
CLK Fall Time	t_{KF}		25		25	ns	
GATE High Level	t_{GGH}	50		50		ns	
GATE Low Level	t_{GGL}	50		50		ns	
GATE Setup Time (Against CLK $\uparrow$)	t_{SGK}	50		40		ns	
GATE Hold Time (Against CLK $\uparrow$)	t_{HKG}	50		50		ns	
CLK Delay Time (From $\overline{WR}\uparrow$): For Count Value Write	t_{DWK}	100		40		ns	$t_{KKH} \geq 125$ ns
		225- t_{KKH}					$t_{KKH} \leq 125$ ns
CLK Setup Time (Against $\overline{WR}\uparrow$): For Latch Command Write	t_{SKW}	85		60		ns	$C_L = 150$ pF
GATE Delay Time (From $\overline{WR}\uparrow$)	t_{DWG}	0		0		ns	
OUT Delay Time (From GATE $\downarrow$)	t_{DGO}		120		100	ns	
OUT Delay Time (From CLK $\downarrow$)	t_{DKO}		150		100	ns	
OUT Delay Time (From $\overline{WR}\uparrow$): Initial OUT	t_{DWO}		295		240	ns	

Note: AC timing test points for output

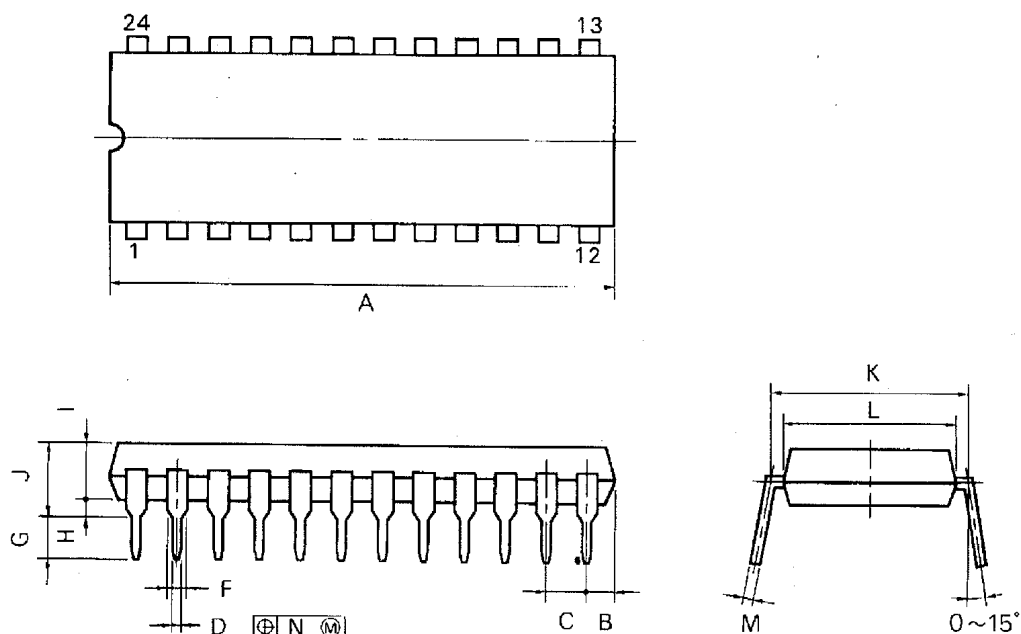
$$V_{OH} = 2.2 \text{ V}, V_{OL} = 0.8 \text{ V}$$

AC Test Input Waveforms



7. PACKAGE DIMENSIONS

24-pin Plastic DIP (600 mil)



P24C-100-600

NOTES

- 1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.
- 2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	33.02 MAX.	1.300 MAX.
B	2.54 MAX.	0.100 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	0.50 ± 0.10	0.020 $\begin{smallmatrix} +0.004 \\ -0.005 \end{smallmatrix}$
F	1.2 MIN.	0.047 MIN.
G	3.5 ± 0.3	0.138 ± 0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.72 MAX.	0.226 MAX.
K	15.24 (T.P.)	0.600 (T.P.)
L	13.2	0.520
M	0.25 $\begin{smallmatrix} +0.10 \\ -0.05 \end{smallmatrix}$	0.010 $\begin{smallmatrix} +0.004 \\ -0.003 \end{smallmatrix}$
N	0.25	0.01