

100315 Low Skew Quad Clock Driver

General Description

The 100315 contains four low skew differential drivers, designed for generation of multiple, minimum skew differential clocks from a single differential input. This device also has the capability to select a secondary single-ended clock source for use in lower frequency system level testing. The 100315 is a 300 Series redesign of the 100115 clock driver.

Features

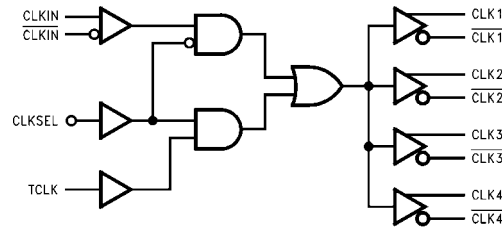
- Low output-to-output skew (≤ 50 ps)
- Differential inputs and outputs
- Secondary clock available for system level testing
- 2000V ESD protection
- Voltage compensated operating range: $-4.2V$ to $-5.7V$

Ordering Code:

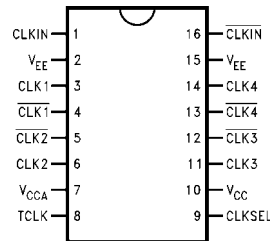
Order Number	Package Number	Package Descriptions
100315SC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Diagram



Connection Diagram



Pin Descriptions

Pin Names	Description
CLKIN, \overline{CLKIN}	Differential Clock Inputs
CLK ₁₋₄ , \overline{CLK}_{1-4}	Differential Clock Outputs
TCLK	Test Clock Input (Note 1)
CLKSEL	Clock Input Select (Note 1)

Note 1: TCLK and CLKSEL are single-ended inputs, with internal 50 k Ω pull-down resistors.

Truth Table

CLKSEL	CLKIN	\overline{CLKIN}	TCLK	CLK _n	\overline{CLK}_n
L	L	H	X	L	H
L	H	L	X	H	L
H	X	X	L	L	H
H	X	X	H	H	L

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care

Absolute Maximum Ratings (Note 2)

Storage Temperature	-65°C to +150°C
Maximum Junction Temperature (T _J)	+150°C
Case Temperature under Bias (T _C)	0°C to +85°C
V _{EE} Pin Potential to Ground Pin	-7.0V to +0.5V
Input Voltage (DC)	V _{CC} to +0.5V
Output Current (DC Output HIGH)	-50 mA
Operating Range (Note 2)	-5.7V to -4.2V
ESD (Note 3)	≥2000V

Recommended Operating Conditions

Case Temperature (T _C)	0°C to +85°C
Supply Voltage (V _{EE})	-5.7V to -4.2V

Note 2: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 3: ESD testing conforms to MIL-STD-883, Method 3015.

DC Electrical Characteristics (Note 4)

V_{EE} = -4.2V to -5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V _{OH}	Output HIGH Voltage	-1025	-955	-870	mV	V _{IN} = V _{IH(Max)} or V _{IL(Min)} Loading with 50Ω to -2.0V
V _{OL}	Output LOW Voltage	-1830	-1705	-1620		
V _{OHC}	Output HIGH Voltage	-1035			mV	V _{IN} = V _{IH(Min)} or V _{IL(Max)} Loading with 50Ω to -2.0V
V _{OLC}	Output LOW Voltage			-1610		
V _{IH}	Single-Ended Input HIGH Voltage	-1165		-870	mV	Guaranteed HIGH Signal for All Inputs
V _{IL}	Single-Ended Input LOW Voltage	-1830		-1475	mV	Guaranteed LOW Signal for All Inputs
I _{IL}	Input LOW Current	0.50			μA	V _{IN} = V _{IL(Min)}
I _{IH}	Input HIGH Current CLKIN, CLKIN TCLK CLKSEL			150 250 250	μA μA μA	V _{IN} = V _{IH(Max)}
V _{DIFF}	Input Voltage Differential	150			mV	Required for Full Output Swing
V _{CM}	Common Mode Voltage	V _{CC} - 2V		V _{CC} - 0.5V	V	
I _{CBO}	Input Leakage Current	-10			μA	V _{IN} = V _{EE}
I _{EE}	Power Supply Current	-67		-35	mA	

Note 4: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

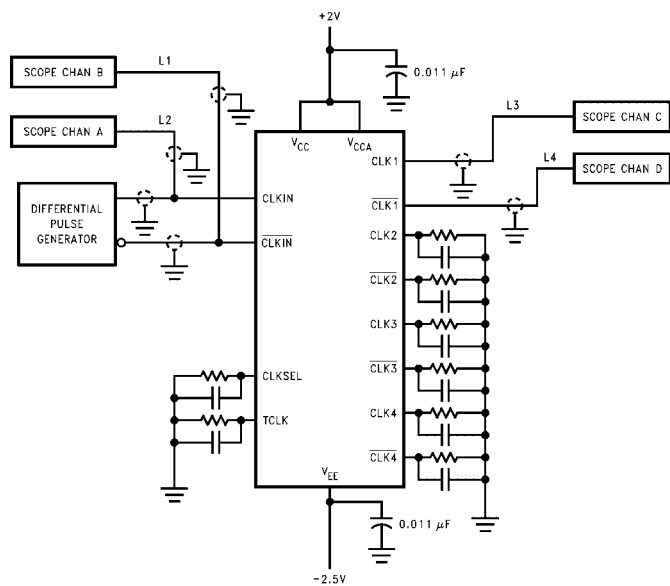
AC Electrical Characteristics

V_{EE} = -4.2V to -4.8, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T _C = 0°C		T _C = +25°C		T _C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f _{MAX}	Maximum Clock Frequency	750		750		750		MHz	
t _{PLH} t _{PHL}	Propagation Delay CLKIN, CLKIN to CLK ₍₁₋₄₎ , CLK ₍₁₋₄₎							ns	Figures 1, 3
	Differential	0.59	0.79	0.62	0.82	0.67	0.87		
	Single-Ended	0.59	0.99	0.62	1.02	0.67	1.07		
t _{PLH} t _{PHL}	Propagation Delay, TCLK to CLK ₍₁₋₄₎ , CLK ₍₁₋₄₎	0.50	1.20	0.50	1.20	0.50	1.20	ns	Figures 1, 2
t _{PLH} t _{PHL}	Propagation Delay, CLKSEL to CLK ₍₁₋₄₎ , CLK ₍₁₋₄₎	0.80	1.60	0.80	1.60	0.80	1.60	ns	Figures 1, 2
t _{TLH} t _{THL}	Transition Time 20% to 80%, 80% to 20%	0.30	0.80	0.30	0.80	0.30	0.80	ns	Figures 1, 4
t _{OST} DIFF	Maximum Skew Opposite Edge Output-to-Output Variation Data to Output Path		50		50		50	ps	(Note 5)

Note 5: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH-to-LOW (t_{OSHL}), or LOW-to-HIGH (t_{OSLH}), or in opposite directions both HL and LH (t_{OST}). Parameters t_{OST} and t_{PS} guaranteed by design.

Test Circuit



Note:
 Shown for testing CLKIN to CLK1 in the differential mode.
 L1, L2, L3 and L4 = equal length 50Ω impedance lines.
 All unused inputs and outputs are loaded with 50Ω in parallel with ≤3 pF to GND.
 Scope should have 50Ω input terminator internally.

FIGURE 1. AC Test Circuit

Switching Waveforms

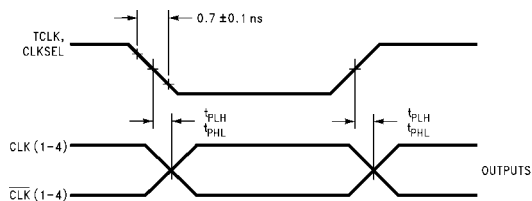


FIGURE 2. Propagation Delay, TCLK, CLKSEL to Outputs

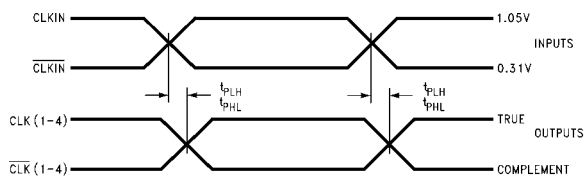


FIGURE 3. Propagation Delay, CLKIN/CLKIN to Outputs

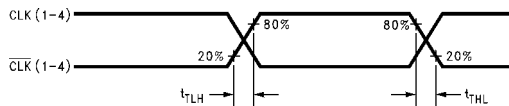
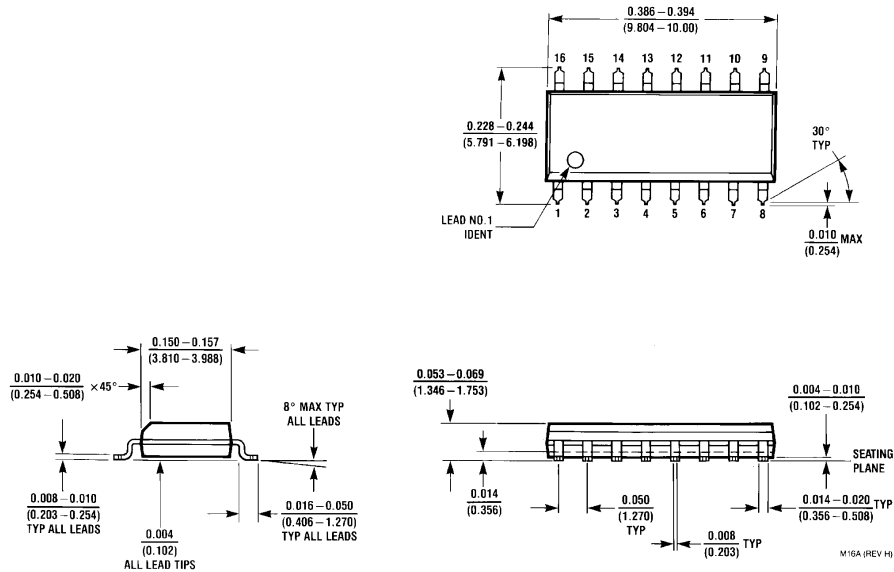


FIGURE 4. Transition Times

Physical Dimensions inches (millimeters) unless otherwise noted



**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
Package Number M16A**

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