

100322

Low Power 9-Bit Buffer

General Description

The 100322 is a monolithic 9-bit buffer. The device contains nine non-inverting buffer gates with single input and output. All inputs have 50 kΩ pull-down resistors and all outputs are buffered.

Features

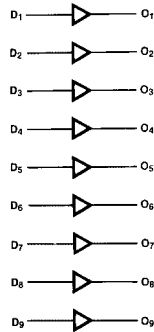
- 30% power reduction of the 100122
- 2000V ESD protection
- Pin/function compatible with 100122
- Voltage compensated operating range = -4.2V to -5.7V
- Available to MIL-STD-883
- Available to industrial grade temperature range (PLCC package only)

Ordering Code:

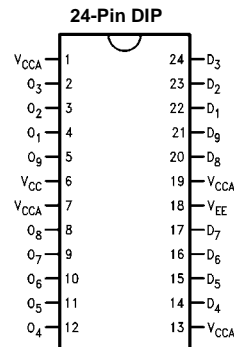
Order Number	Package Number	Package Description
100322PC	N24E	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-011, 0.400 Wide
100322QC	V28A	28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square
100322QI	V28A	28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square Industrial Temperature Range (-40°C to +85°C)

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol



Connection Diagrams



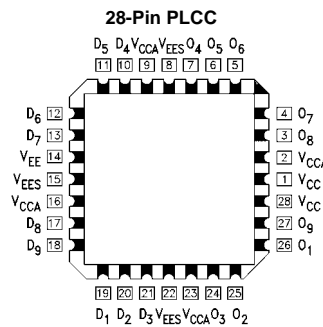
Pin Descriptions

Pin Names	Description
D ₁ , D ₉	Data Inputs
O ₁ , O ₉	Data Outputs

Truth Table

Inputs	Outputs
D ₁ - D ₉	O ₁ - O ₉
L	L
H	H

H = HIGH Voltage Level L = LOW Voltage Level



Absolute Maximum Ratings (Note 1)

Storage Temperature (T_{STG})	-65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
V_{EE} Pin Potential to Ground Pin	-7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	-50 mA
ESD (Note 2)	$\geq 2000V$

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Industrial	-40°C to +85°C
Supply Voltage (V_{EE})	-5.7V to -4.2V

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Commercial Version**DC Electrical Characteristics** (Note 3)

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $T_C = 0^\circ C$ to $+85^\circ C$

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH Voltage	-1025	-955	-870	mV	$V_{IN} = V_{IH} (Max)$ Loading with 50Ω to -2.0V
V_{OL}	Output LOW Voltage	-1830	-1705	-1620		
V_{OHC}	Output HIGH Voltage	-1035			mV	$V_{IN} = V_{IH} (Min)$ Loading with 50Ω to -2.0V
V_{OLC}	Output LOW Voltage			-1610		
V_{IH}	Input HIGH Voltage	-1165		-870	mV	Guaranteed HIGH Signal for All Inputs
V_{IL}	Input LOW Voltage	-1830		-1475	mV	Guaranteed LOW Signal for All Inputs
I_{IL}	Input LOW Current	0.50			μA	$V_{IN} = V_{IL} (Min)$
I_{IH}	Input HIGH Current			240	μA	$V_{IN} = V_{IH} (Max)$
I_{EE}	Power Supply Current	-65		-30	mA	Inputs OPEN

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DIP AC Electrical Characteristics

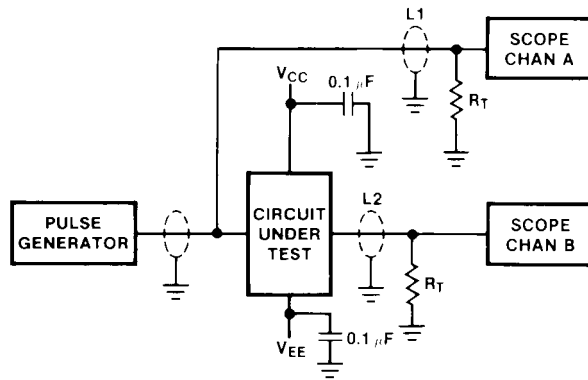
$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	0.45	1.45	0.45	1.45	0.45	1.55	ns	Figures 1, 2
t_{PHL}	Data to Output								(Note 4)
t_{TLH}	Transition Time	0.35	1.20	0.35	1.20	0.35	1.20	ns	Figures 1, 2
t_{THL}	20% to 80%, 80% to 20%								

Note 4: The propagation delay specified is for single output switching. Delays may vary up to 200 ps with multiple outputs switching.

Commercial Version (Continued)									
PLCC AC Electrical Characteristics									
$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$									
Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.45	1.25	0.45	1.25	0.45	1.35	ns	Figures 1, 2 (Note 5)
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.10	0.35	1.10	0.35	1.10	ns	Figures 1, 2
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		200		200		200	ps	(Note 6)
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		200		200		200	ps	(Note 6)
t_{OST}	Maximum Skew Opposite Edge Output-to-Output Variation Data to Output Path		260		260		260	ps	(Note 6)
t_{PS}	Maximum Skew Pin (Signal) Transition Variation Data to Output Path		200		200		200	ps	(Note 6)
<p>Note 5: The propagation delay specified is for single output switching. Delays may vary up to 200 ps with multiple outputs switching.</p> <p>Note 6: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH-to-LOW (t_{OSHL}), or LOW-to-HIGH (t_{OSLH}), or in opposite directions both HL and LH (t_{OST}). Parameters t_{OST} and t_{PS} guaranteed by design.</p>									
Industrial Version									
PLCC DC Electrical Characteristics (Note 7)									
$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $T_C = -40^\circ C$ to $+85^\circ C$									
Symbol	Parameter	$T_C = -40^\circ C$		$T_C = 0^\circ C$ to $+85^\circ C$		Units	Conditions		
		Min	Max	Min	Max				
V_{OH}	Output HIGH Voltage	-1085	-870	-1025	-870	mV	$V_{IN} = V_{IH (Max)}$ or $V_{IL (Min)}$	Loading with 50Ω to -2.0V	
V_{OL}	Output LOW Voltage	-1830	-1575	-1830	-1620				
V_{OHC}	Output HIGH Voltage	-1095		-1035		mV	$V_{IN} = V_{IH (Min)}$ or $V_{IL (Max)}$	Loading with 50Ω to -2.0V	
V_{OLC}	Output LOW Voltage		-1565		-1610				
V_{IH}	Input HIGH Voltage	-1170	-870	-1165	-870	mV	Guaranteed HIGH Signal for All Inputs		
V_{IL}	Input LOW Voltage	-1830	-1480	-1830	-1475	mV	Guaranteed LOW Signal for All Inputs		
I_{IL}	Input LOW Current	0.50		0.50		μA	$V_{IN} = V_{IL (Min)}$		
I_{IH}	Input HIGH Current		300		240	μA	$V_{IN} = V_{IH (Max)}$		
I_{EE}	Power Supply Current	-65	-30	-65	-30	mA	Inputs OPEN		
<p>Note 7: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.</p>									
PLCC AC Electrical Characteristics									
$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$									
Symbol	Parameter	$T_C = -40^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.45	1.25	0.45	1.25	0.45	1.35	ns	Figures 1, 2 (Note 8)
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.30	1.20	0.35	1.10	0.35	1.10	ns	Figures 1 Figure 2
<p>Note 8: The propagation delay specified is for single output switching. Delays may vary up to 200 ps with multiple outputs switching.</p>									

Test Circuit



Notes:

$V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V$

L1 and L2 = equal length 50Ω impedance lines

$R_T = 50\Omega$ terminator internal to scope

Decoupling 0.1 μF from GND to V_{CC} and V_{EE}

All unused outputs are loaded with 50Ω to GND

$C_L =$ Fixture and stray capacitance ≤ 3 pF

FIGURE 1. AC Test Circuit

Switching Waveforms

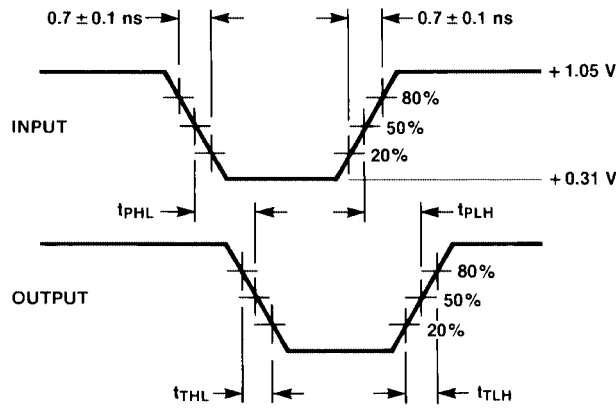
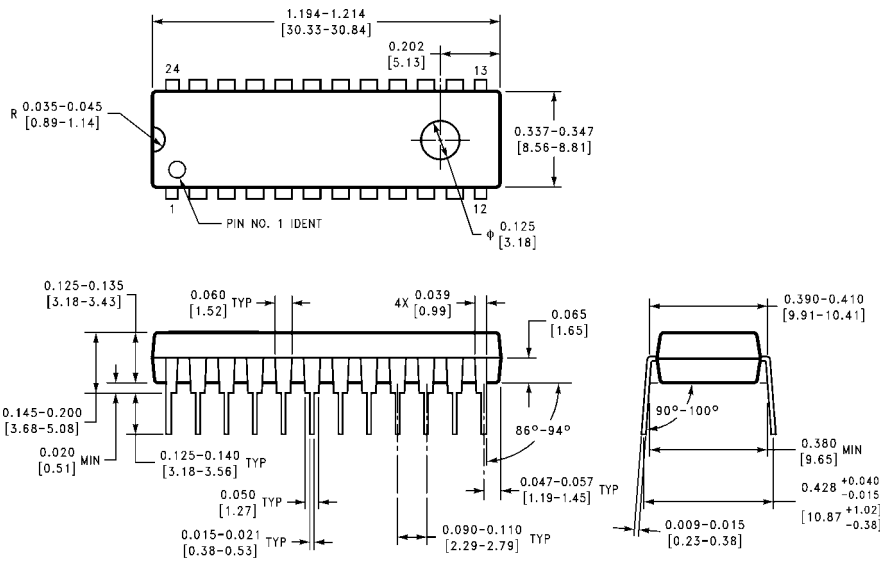


FIGURE 2. Propagation Delay and Transition Times

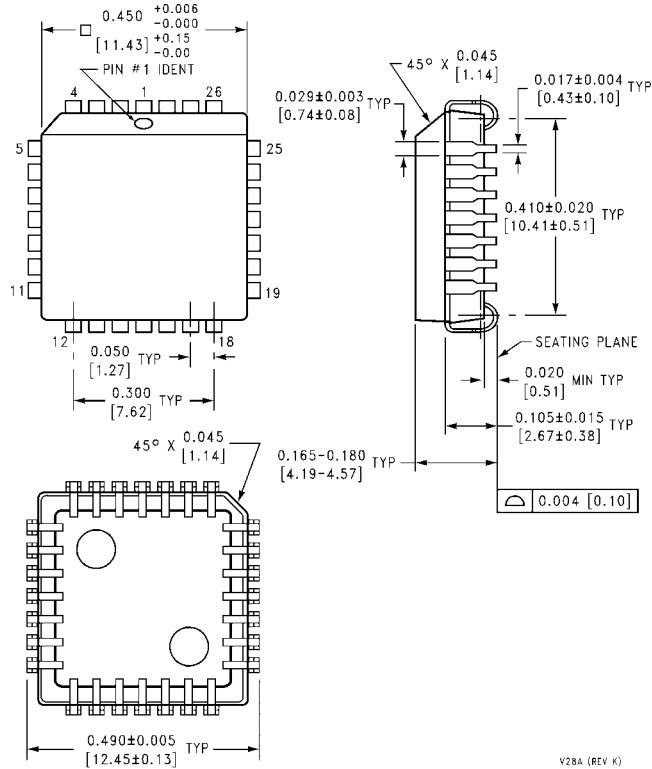
Physical Dimensions inches (millimeters) unless otherwise noted



**24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-011, 0.400 Wide
Package Number N24E**

N24E (REV A)

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square Package Number V28A

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