

# 100352

## Low Power 8-Bit Buffer with Cut-Off Drivers

### General Description

The 100352 contains an 8-bit buffer, individual inputs ( $D_n$ ), outputs ( $Q_n$ ), and a data output enable pin ( $\overline{OEN}$ ). A Q output follows its D input when the  $\overline{OEN}$  pin is LOW. A HIGH on  $\overline{OEN}$  holds the outputs in a cut-off state. The cut-off state is designed to be more negative than a normal ECL LOW level. This allows the output emitter-followers to turn off when the termination supply is  $-2.0V$ , presenting a high impedance to the data bus. This high impedance reduces termination power and prevents loss of low state noise margin when several loads share the bus.

The 100352 outputs are designed to drive a doubly terminated  $50\Omega$  transmission line ( $25\Omega$  load impedance). All inputs have  $50\text{ k}\Omega$  pull-down resistors.

### Features

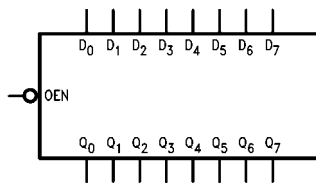
- Cut-off drivers
- Drives  $25\Omega$  load
- Low power operation
- 2000V ESD protection
- Voltage compensated operating range =  $-4.2V$  to  $-5.7V$
- Available to industrial grade temperature range

### Ordering Code:

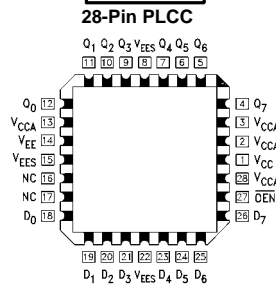
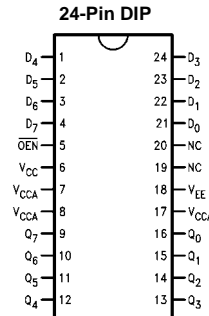
Order Number	Package Number	Package Description
100352PC	N24E	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-011, 0.400 Wide
100352QC	V28A	28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square
100352QI	V28A	28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square Industrial Temperature Range ( $-40^\circ\text{C}$ to $+85^\circ\text{C}$ )

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

### Logic Symbol



### Connection Diagrams



### Pin Descriptions

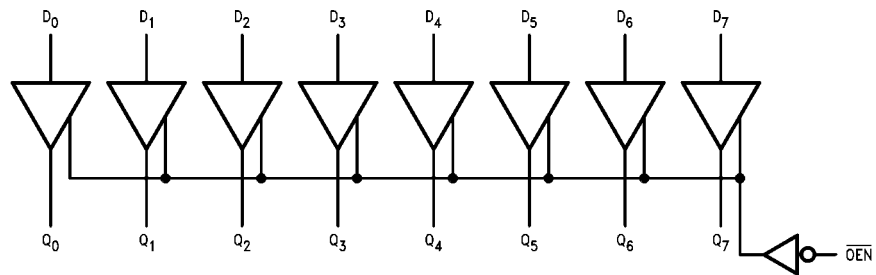
Pin Names	Description
$D_0$ – $D_7$	Data Inputs
$\overline{OEN}$	Output Enable Input
$Q_0$ – $Q_7$	Data Outputs
NC	No Connect

## Truth Table

Inputs		Outputs
$D_n$	$\overline{OEN}$	$Q_n$
L	L	L
H	L	H
X	H	Cutoff

H = HIGH Voltage Level  
L = LOW Voltage Level  
Cutoff = Lower-than-LOW State  
X = Don't Care

## Logic Diagram



**Absolute Maximum Ratings**(Note 1)

Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
Maximum Junction Temperature ( $T_J$ )	+150°C
$V_{EE}$ Pin Potential to Ground Pin	-7.0V to +0.5V
Input Voltage (DC)	$V_{EE}$ to +0.5V
Output Current (DC Output HIGH)	-100 mA
ESD (Note 2)	≥2000V

**Recommended Operating Conditions**

Case Temperature ( $T_C$ )	Commercial	0°C to +85°C
	Industrial	-40°C to +85°C
Supply Voltage ( $V_{EE}$ )		-5.7V to -4.2V

**Note 1:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Note 2:** ESD testing conforms to MIL-STD-883, Method 3015.

**Commercial Version****DC Electrical Characteristics** (Note 3)

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $T_C = 0°C$  to  $+85°C$

Symbol	Parameter	Min	Typ	Max	Units	Conditions
$V_{OH}$	Output HIGH Voltage	-1025	-955	-870	mV	$V_{IN} = V_{IH} (Max)$ or $V_{IL} (Min)$ Loading with 25Ω to -2.0V
$V_{OL}$	Output LOW Voltage	-1830	-1705	-1620		
$V_{OHC}$	Output HIGH Voltage	-1035			mV	$V_{IN} = V_{IH} (Min)$ or $V_{IL} (Max)$ Loading with 25Ω to -2.0V
$V_{OLC}$	Output LOW Voltage			-1610		
$V_{OLZ}$	Cut-Off LOW Voltage			-1950	mV	$V_{IN} = V_{IH} (Min)$ or $V_{IL} (Max)$ OEN = HIGH
$V_{IH}$	Input HIGH Voltage	-1165		-870	mV	Guaranteed HIGH Signal for All Inputs
$V_{IL}$	Input LOW Voltage	-1830		-1475	mV	Guaranteed LOW Signal for All Inputs
$I_{IL}$	Input LOW Current	0.50			μA	$V_{IN} = V_{IL} (Min)$
$I_{IH}$	Input HIGH Current			240	μA	$V_{IN} = V_{IH} (Max)$
$I_{EE}$	Power Supply Current	-138 -143		-70 -70	mA	Inputs Open $V_{EE} = -4.2V$ to $-4.8V$ $V_{EE} = -4.2V$ to $-5.7V$

**Note 3:** The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

**DIP AC Electrical Characteristics**

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = 0°C$		$T_C = +25°C$		$T_C = +85°C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
$t_{PLH}$	Propagation Delay	0.70	2.00	0.70	2.00	0.70	2.20	ns	Figures 1, 2 (Note 4)
$t_{PHL}$	Dn to Output								
$t_{PZH}$	Propagation Delay	1.60	4.20	1.60	4.20	1.60	4.20	ns	Figures 1, 2 (Note 4)
$t_{PHZ}$	OEN to Output								
$t_{TLH}$	Transition Time	0.45	2.00	0.45	2.00	0.45	2.00	ns	Figures 1, 2
$t_{THL}$	20% to 80%, 80% to 20%								

**Note 4:** The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

## Commercial Version (Continued) PLCC AC Electrical Characteristics

$V_{EE} = 4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay Dn to Output	0.70	1.80	0.70	1.80	0.70	2.00	ns	Figures 1, 2 (Note 5)
$t_{PZH}$ $t_{PHZ}$	Propagation Delay OEN to Output	1.60	4.00	1.60	4.00	1.60	4.00	ns	Figures 1, 2 (Note 5)
$t_{TLH}$ $t_{THL}$	Transition Time 20% to 80%, 80% to 20%	0.45	1.90	0.45	1.90	0.45	1.90	ns	Figures 1, 2
$t_{OSHL}$	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		230		230		230	ps	PLCC only (Note 6)
$t_{OSLH}$	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		240		240		240	ps	PLCC only (Note 6)
$t_{OST}$	Maximum Skew Opposite Edge Output-to-Output Variation Data to Output Path		350		350		350	ps	PLCC only (Note 6)
$t_{PS}$	Maximum Skew Pin (Signal) Transition Variation Data to Output Path		350		350		350	ps	PLCC only (Note 6)

**Note 5:** The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

**Note 6:** Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH-to-LOW ( $t_{OSHL}$ ), or LOW-to-HIGH ( $t_{OSLH}$ ), or in opposite directions both HL and LH ( $t_{OST}$ ). Parameters  $t_{OST}$  and  $t_{PS}$  guaranteed by design.

**Industrial Version****PLCC DC Electrical Characteristics** (Note 7)
 $V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $T_C = -40^{\circ}C$  to  $+85^{\circ}C$ 

Symbol	Parameter	$T_C = -40^{\circ}C$		$T_C = 0^{\circ}C$ to $+85^{\circ}C$		Units	Conditions
		Min	Max	Min	Max		
$V_{OH}$	Output HIGH Voltage	-1085	-870	-1025	-870	mV	$V_{IN} = V_{IH(Max)}$ or $V_{IL(Min)}$
$V_{OL}$	Output LOW Voltage	-1830	-1575	-1830	-1620		
$V_{OHC}$	Output HIGH Voltage	-1095		-1035		mV	$V_{IN} = V_{IH(Min)}$ or $V_{IL(Max)}$
$V_{OLC}$	Output LOW Voltage		-1565		-1610		
$V_{OLZ}$	Cut-Off LOW Voltage		-1950		-1950	mV	$V_{IN} = V_{IH(Min)}$ or $V_{IL (Max)}$
$V_{IH}$	Input HIGH Voltage	-1170	-870	-1165	-870	mV	Guaranteed HIGH Signal for All Inputs
$V_{IL}$	Input LOW Voltage	-1830	-1480	-1830	-1475	mV	Guaranteed LOW Signal for All Inputs
$I_{IL}$	Input LOW Current	0.50		0.50		$\mu A$	$V_{IN} = V_{IL(Min)}$
$I_{IH}$	Input HIGH Current		340		240	$\mu A$	$V_{IN} = V_{IH(Max)}$
$I_{EE}$	Power Supply Current	-138 -143	-60 -60	-138 -143	-70 -70	mA	Inputs OPEN $V_{EE} = -4.2V$ to $-4.8V$ $V_{EE} = -4.2V$ to $-5.7V$

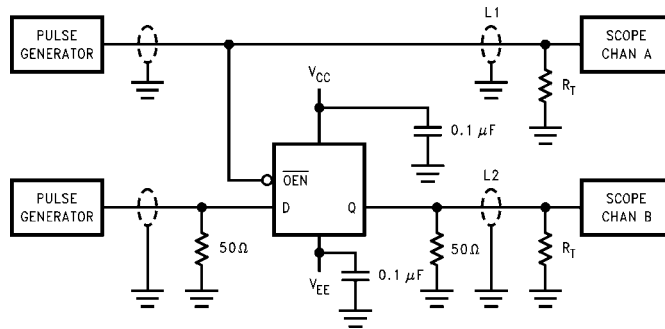
**Note 7:** The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

**PLCC AC Electrical Characteristics**
 $V_{EE} = 4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$ 

Symbol	Parameter	$T_C = -40^{\circ}C$		$T_C = +25^{\circ}C$		$T_C = +85^{\circ}C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
$t_{PLH}$	Propagation Delay	0.60	1.80	0.70	1.80	0.70	2.00	ns	Figures 1, 2 (Note 8)
$t_{PHL}$	Dn to Output								
$t_{PZH}$	Propagation Delay	1.40	4.40	1.60	4.00	1.60	4.00	ns	Figures 1, 2 (Note 8)
$t_{PHZ}$	OEN to Output								
$t_{TLH}$	Transition Time	0.40	2.50	0.45	1.90	0.45	1.90	ns	Figures 1Figure 2
$t_{THL}$	20% to 80%, 80% to 20%								

**Note 8:** The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

### Test Circuitry



**Notes:**

$V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V$

L1 and L2 = equal length 50Ω impedance lines

$R_T = 50\Omega$  terminator internal to scope

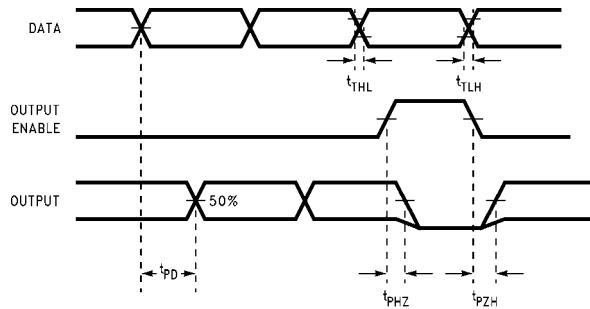
Decoupling 0.1 μF from GND to  $V_{CC}$  and  $V_{EE}$

All unused outputs are loaded with 25Ω to GND

$C_L$  = Fixture and stray capacitance  $\leq 3$  pF

FIGURE 1. AC Test Circuit

### Switching Waveforms

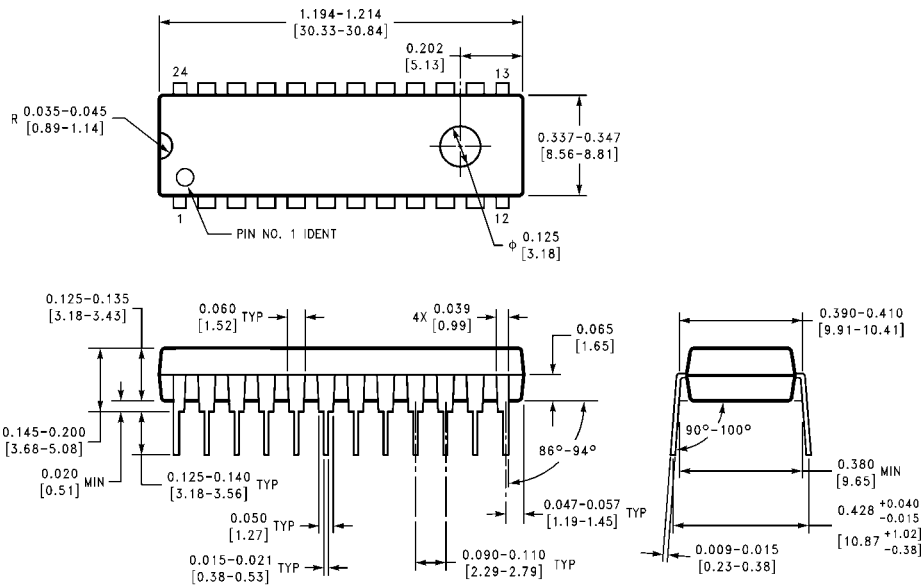


**Note:**

The output AC measurement point for cut-off propagation delay testing = the 50% voltage point between active  $V_{OL}$  and  $V_{OH}$ .

FIGURE 2. Propagation Delay, Cut-Off and Transition Times

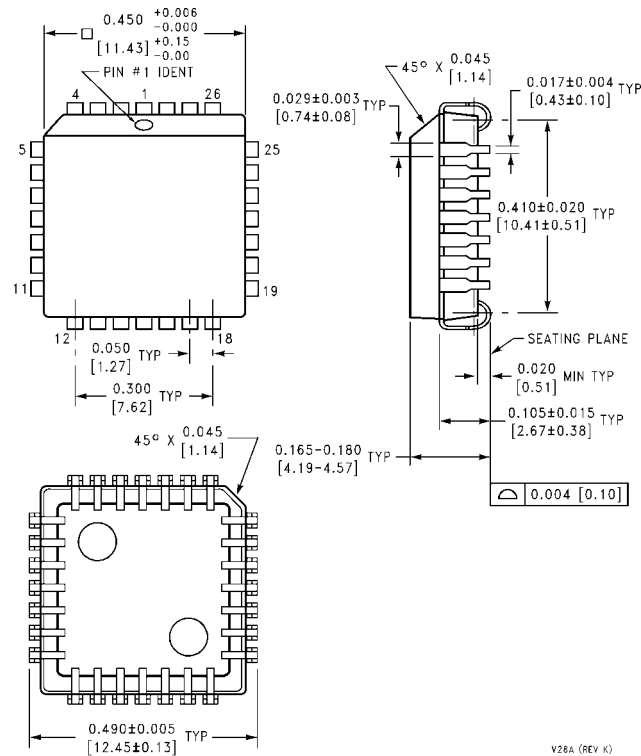
**Physical Dimensions** inches (millimeters) unless otherwise noted



**24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-011, 0.400 Wide Package Number N24E**

N24E (REV A)

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square Package Number V28A**

V28A (REV K)

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