FAIRCHILD SEMICONDUCTOR™

March 1998

100354
Low Power 8-Bit Register with Cut-Off Drivers

General Description

The 100354 contains eight D-Type edge triggered, master/slave flip-flops with individual inputs (D_n), true outputs (Q_n), a clock input (CP), an output enable pin ($\overline{OEN}$), and a common clock enable pin ($\overline{CEN}$). Data enters the master when CP is LOW and transfers to the slave when CP goes HIGH. When the $\overline{CEN}$ input goes HIGH it overrides all other inputs, disables the clock, and the Q outputs maintain the last state.

A Q output follows its D input when the $\overline{OEN}$ pin is LOW. A HIGH on $\overline{OEN}$ holds the outputs in a cut-off state. The cut-off state is designed to be more negative than a normal ECL LOW level. This allows the output emitter-followers to turn off when the termination supply is −2.0V, presenting a high impedance to the data bus. This high impedance reduces termination power and prevents loss of low state noise margin when several loads share the bus.

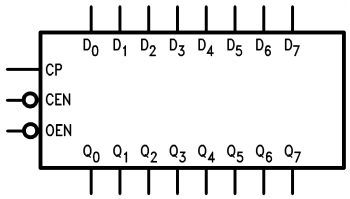
The 100354 outputs are designed to drive a doubly terminated 50Ω transmission line (25Ω load impedance). All inputs have 50 kΩ pull-down resistors.

Features

- Cut-off drivers
- Drives 25Ω load
- Low power operation
- 2000V ESD protection
- Voltage compensated operating range = −4.2V to −5.7V
- Available to industrial grade temperature range

Ordering Code:

Logic Symbol



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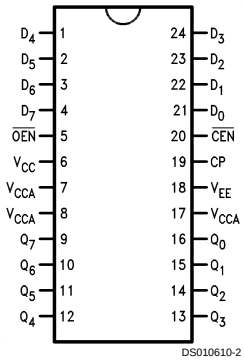
Pin Names	Description
D_0–D_7	Data Inputs
$\overline{CEN}$	Clock Enable Input
CP	Clock Input (Active Rising Edge)
$\overline{OEN}$	Output Enable Input
Q_0–Q_7	Data Outputs

Connection Diagrams

24-Pin DIP



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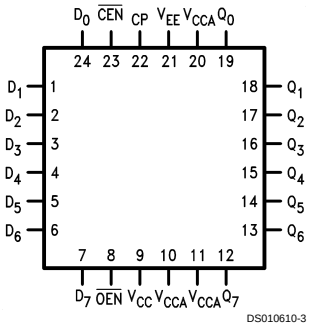
24-Pin Quad Cerpak



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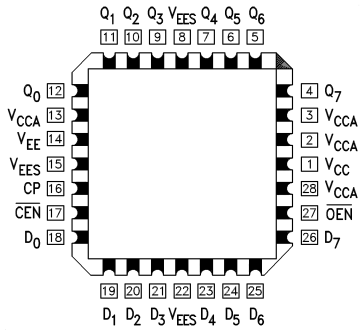
28-Pin PCC



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Absolute Maximum Ratings (Note 1)

Above which the useful life may be impaired.

Storage Temperature (T_{STG})	−65˚C to +150˚C
Maximum Junction Temperature (T_J)	
Ceramic	+175˚C
Plastic	+150˚C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−100 mA
ESD (Note 2)	≥2000V

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0˚C to +85˚C
Industrial	−40˚C to +85˚C
Military	−55˚C to +125˚C
Supply Voltage (V_{EE})	−5.7V to −4.2V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Commercial Version DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0˚C to +85˚C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage	−1025	−955	−870	mV	V_{IN} =$V_{IH\ (Max)}$	Loading with
V_{OL}	Output LOW Voltage	−1830	−1705	−1620		or $V_{IL\ (Min)}$	25Ω to −2.0V
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH\ (Min)}$	Loading with
V_{OLC}	Output LOW Voltage			−1610		or $V_{IL\ (Max)}$	25Ω to −2.0V
V_{OLZ}	Cutoff LOW Voltage			−1950	mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	$\overline{OEN}$ = HIGH
V_{IH}	Input HIGH Voltage	−1165		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			µA	V_{IN} = $V_{IL\ (Min)}$	
I_{IH}	Input HIGH Current			240	µA	V_{IN} = $V_{IH\ (Max)}$	
I_{EE}	Power Supply Current					Inputs Open	
		−202		−105	mA	V_{EE} = −4.2V to −4.8V	
		−209		−105		V_{EE} = −4.2V to −5.7V	

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DIP AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0˚C		T_C = +25˚C		T_C = +85˚C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{Max}	Toggle Frequency	250		250		250		MHz	*Figures 1, 4*
t_{PLH}	Propagation Delay	1.40	3.00	1.40	3.00	1.50	3.10	ns	*Figures 1, 4*
t_{PHL}	CP to Output								(Note 4)
t_{PZH}	Propagation Delay	1.60	4.20	1.60	4.20	1.60	4.20	ns	*Figures 3, 7*
t_{PHZ}	$\overline{OEN}$ to Output	1.00	2.70	1.00	2.70	1.00	2.70		(Note 4)
t_{TLH}	Transition Time	0.45	2.00	0.45	2.00	0.45	2.00	ns	*Figures 1, 4*
t_{THL}	20% to 80%, 80% to 20%								
t_S	Setup Time								
	D_n	1.10		1.10		1.10			
	$\overline{CEN}$ (Disable Time)	0.40		0.40		0.40		ns	*Figures 2, 5*
	$\overline{CEN}$ (Release Time)	1.10		1.10		1.10			
t_H	Hold Time								
	D_n	0.10		0.10		0.10		ns	*Figures 1, 6*

DIP AC Electrical Characteristics (Continued)

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0˚C		T_C = +25˚C		T_C = +85˚C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{pw}(H)	Pulse Width High CP	2.00		2.00		2.00		ns	*Figures 1, 4*

Note 4: The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

PCC and Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0˚C		T_C = +25˚C		T_C = +85˚C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{Max}	Toggle Frequency	250		250		250		MHz	*Figures 1, 4*
t_{PLH}	Propagation Delay	1.40	2.80	1.40	2.80	1.50	2.90	ns	*Figures 1, 4*
t_{PHL}	CP to Output								(Note 6)
t_{PZH}	Propagation Delay	1.60	4.00	1.60	4.00	1.60	4.00	ns	*Figures 3, 7*
t_{PHZ}	$\overline{OEN}$ to Output	1.00	2.50	1.00	2.50	1.00	2.50		(Note 6)
t_{TLH}	Transition Time	0.45	1.90	0.45	1.90	0.45	1.90	ns	*Figures 1, 4*
t_{THL}	20% to 80%, 80% to 20%								
t_S	Setup Time								
	D_n	1.00		1.00		1.00			
	$\overline{CEN}$ (Disable Time)	0.30		0.30		0.30		ns	*Figures 2, 5*
	$\overline{CEN}$ (Release Time)	1.00		1.00		1.00			
t_H	Hold Time								
	D_n	0.00		0.00		0.00		ns	*Figures 1, 6*
t_{pw}(H)	Pulse Width High								
	CP	2.00		2.00		2.00		ns	*Figures 1, 4*
t_{OSHL}	Maximum Skew Common Edge								PCC Only
	Output-to-Output Variation							ps	(Note 5)
	Clock to Output Path		280		280		280		
t_{OSLH}	Maximum Skew Common Edge								PCC Only
	Output-to-Output Variation							ps	(Note 5)
	Clock to Output Path		340		340		340		
t_{OST}	Maximum Skew Opposite Edge								PCC Only
	Output-to-Output Variation							ps	(Note 5)
	Clock to Output Path		340		340		340		
t_{PS}	Maximum Skew								PCC Only
	Pin (Signal) Transition Variation							ps	(Note 5)
	Clock to Output Path		250		250		250		

Note 5: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}), or LOW to HIGH (t_{OSLH}), or in oppostie directions both HL and LH (t_{OST}). Parameters t_{OST} and t_{PS} guaranteed by design.

Note 6: The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

Industrial Version
PCC DC Electrical Characteristics

V_{EE}=−4.2V to −5.7V, V_{CC}= V_{CCA}= GND, T_C=−40˚C to +85˚C (Note 7)

Symbol	Parameter	T_C = −40˚C		T_C = 0˚ to +85˚C		Units	Conditions	
		Min	Max	Min	Max			
V_{OH}	Output HIGH Voltage	−1085	−870	−1025	−870	mV	V_{IN} =V_{IH} (Max)	Loading with
V_{OL}	Output LOW Voltage	−1830	−1575	−1830	−1620		or V_{IL} (Min)	50Ω to −2.0V
V_{OHC}	Output HIGH Voltage	−1095		−1035		mV	V_{IN} = V_{IH} (Min)	Loading with
V_{OLC}	Output LOW Voltage		−1565		−1610		or V_{IL} (Max)	50Ω to −2.0V
V_{OLZ}	Cutoff LOW Voltage		−1900		−1950	mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	$\overline{OEN}$ = HIGH
V_{IH}	Input HIGH Voltage	−1170	−870	−1165	−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830	−1480	−1830	−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50		0.50		µA	V_{IN} = V_{IL} (Min)	
I_{IH}	Input HIGH Current		240		240	µA	V_{IN} = V_{IH} (Max)	
I_{EE}	Power Supply Current						Inputs Open	
		−202	−105	−202	−105	mA	V_{EE} = −4.2V to −4.8V	
		−209	−105	−209	−105		V_{EE} = −4.2V to −5.7V	

Note 7: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

PCC AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −40˚C		T_C = +25˚C		T_C = +85˚C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{Max}	Toggle Frequency	250		250		250		MHz	*Figures 1, 4*
t_{PLH}	Propagation Delay	1.40	2.80	1.40	2.80	1.50	2.90	ns	*Figures 1, 4*
t_{PHL}	CP to Output								(Note 8)
t_{PZH}	Propagation Delay	1.50	4.10	1.60	4.00	1.60	4.00	ns	*Figures 3, 5*
t_{PHZ}	$\overline{OEN}$ to Output	1.00	2.50	1.00	2.50	1.00	2.50		(Note 8)
t_{TLH}	Transition Time	0.45	1.90	0.45	1.90	0.45	1.90	ns	*Figures 1, 4*
t_{THL}	20% to 80%, 80% to 20%								
t_S	Setup Time								
	D_n	1.00		1.00		1.00			
	$\overline{CEN}$ (Disable Time)	0.30		0.30		0.30		ns	*Figures 2, 5*
	$\overline{CEN}$ (Release Time)	1.00		1.00		1.00			
t_H	Hold Time								
	D_n	0.00		0.00		0.00		ns	*Figures 1, 6*
t_{pw}(H)	Pulse Width High								
	CP	2.00		2.00		2.00		ns	*Figures 1, 4*

Note 8: The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

Military Version—Preliminary
DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −55˚C to +125˚C

Symbol	Parameter	Min	Max	Units	T_C	Conditions		Notes
V_{OH}	Output HIGH Voltage	−1025	−870	mV	0˚C to +125˚C	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 25Ω to −2.0V	(Notes 9, 10, 11, 12)
		−1085	−870	mV	−55˚C			
V_{OL}	Output LOW Voltage	−1830	−1620	mV	0˚C to +125˚C			
		−1830	−1555	mV	−55˚C			
V_{OHC}	Output HIGH Voltage	−1035		mV	0˚C to +125˚C	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 25Ω to −2.0V	(Notes 9, 10, 11)
		−1085		mV	−55˚C			
V_{OLC}	Output LOW Voltage		−1610	mV	0˚C to +125˚C			
			−1555	mV	−55˚C			
V_{OLZ}	Cutoff LOW Voltage		−1950	mV	0˚C to +125˚C	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	$\overline{OEN}$ = HIGH	(Notes 9, 10, 11)
			−1850		−55˚C			
V_{IH}	Input HIGH Voltage	−1165	−870	mV	−55˚C to +125˚C	Guaranteed HIGH Signal for All Inputs		(Notes 9, 10, 11, 12)
V_{IL}	Input LOW Voltage	−1830	−1475	mV	−55˚C to +125˚C	Guaranteed LOW Signal for All Inputs		(Notes 9, 10, 11, 12)
I_{IL}	Input LOW Current	0.50		µA	−55˚C to +125˚	V_{EE} = −4.2V, V_{IN} = $V_{IL\ (Min)}$		(Notes 9, 10, 11)
I_{IH}	Input HIGH Current		240	µA	0˚C to +125˚C	V_{EE} = −5.7V, V_{IN} = $V_{IH\ (Max)}$		(Notes 9, 10, 11)
			340	µA	−55˚C			
I_{EE}	Power Supply Current				−55˚C to	Inputs Open		
		−215	−85	mA	+125˚C	V_{EE} = −4.2V to −4.8V		(Notes 9, 10, 11)
		−225	−85			V_{EE} = −4.2V to −5.7V		

Note 9: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55˚C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 10: Screen tested 100% on each device at −55˚C, +25˚C, and +125˚C, Subgroups 1, 2, 3, 7, and 8.

Note 11: Sample tested (Method 5005, Table I) on each manufactured lot at −55˚C, +25˚C, and +125˚C, Subgroups A1, 2, 3, 7, and 8.

Note 12: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL}.

AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −55˚C		T_C = +25˚C		T_C = +125˚C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
f_{Max}	Toggle Frequency	200		250		200		MHz	*Figures 1, 4*	(Note 16)
t_{PLH}	Propagation Delay	0.9	3.70	1.0	3.20	1.20	3.90	ns	*Figures 1, 4*	(Notes 13, 14, 15, 17)
t_{PHL}	CP to Output									
t_{PZH}	Propagation Delay	1.20	5.0	1.60	4.20	1.40	4.30	ns	*Figures 3, 7*	(Notes 13, 14, 15, 17)
t_{PHZ}	$\overline{OEN}$ to Output	0.70	3.0	0.70	2.80	0.70	3.20			
t_{TLH}	Transition Time	0.40	2.50	0.40	2.40	0.40	2.70	ns	*Figures 1, 4*	(Note 16)
t_{THL}	20% to 80%, 80% to 20%									
t_S	Setup Time									
	D_n	1.30		1.30		1.30				
	$\overline{CEN}$ (Disable Time)	0.60		0.60		0.60		ns	*Figures 2, 5*	(Note 16)
	$\overline{CEN}$ (Release Time)	1.30		1.30		1.30				
t_H	Hold Time									
	D_n	0.30		0.30		0.30		ns	*Figures 1, 6*	(Note 16)
t_{pw}(H)	Pulse Width HIGH									
	CP	2.4		2.4		2.4		ns	*Figures 1, 4*	(Note 16)

Note 13: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55˚C), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 14: Screen tested 100% on each device at +25˚C, temperature only, Subgroup A9.

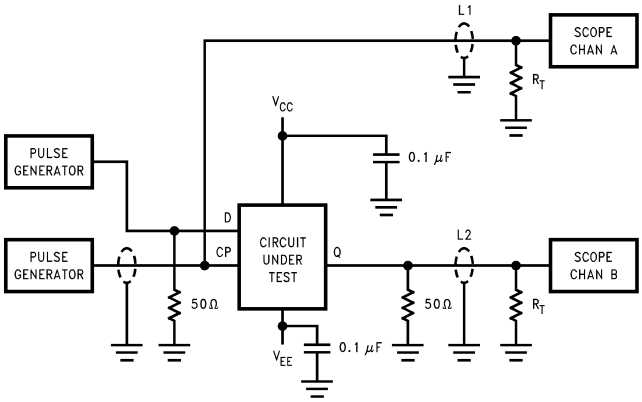
AC Electrical Characteristics (Continued)

Note 15: Sample tested (Method 5005, Table I) on each manufactured lot at +25˚C, Subgroup A9, and at +125˚C and −55˚C temperatures, Subgroups A10 and A11.

Note 16: Not tested at +25˚C, +125˚C, and −55˚C temperature (design characterization data).

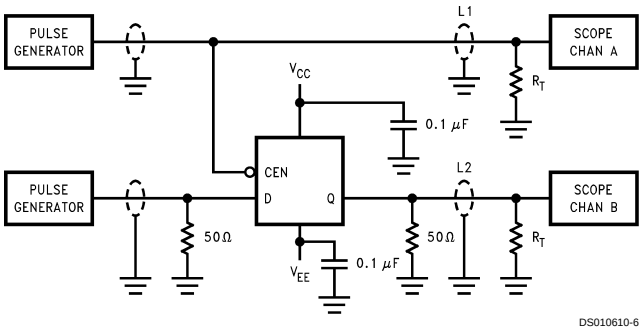
Note 17: The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

Test Circuitry



Notes:
V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 µF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 25Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF

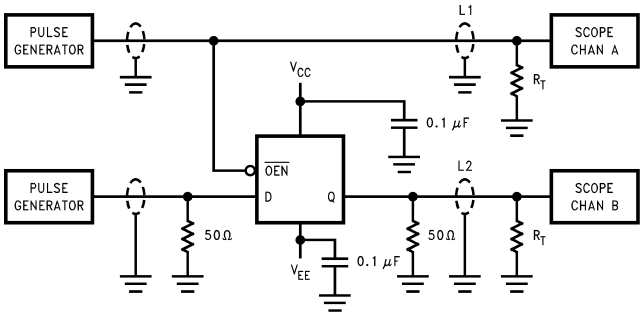
FIGURE 1. Toggle Frequency Test Circuit



Notes:
V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 µF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 25Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF

FIGURE 2. AC Test Circuit

Test Circuitry (Continued)



Notes:
V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 µF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 25Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF

FIGURE 3. AC Test Circuit

Switching Waveforms

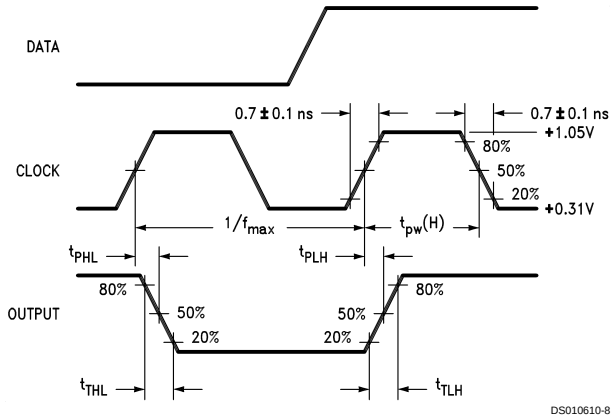


FIGURE 4. Propagation Delay (Clock) and Transition Times

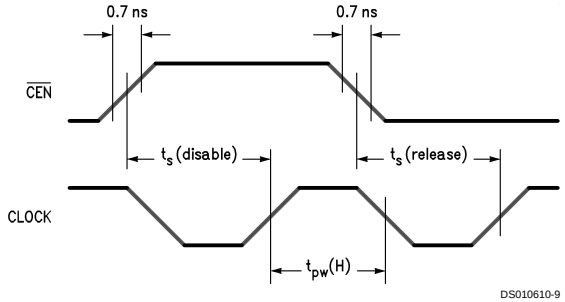
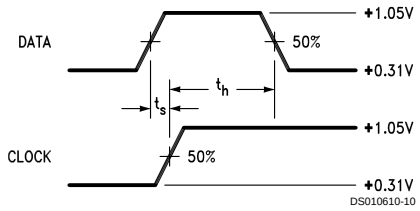


FIGURE 5. Setup and Pulse Width Times

Switching Waveforms (Continued)

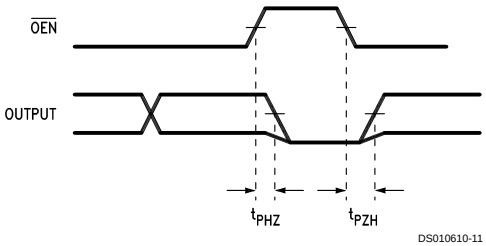


Notes:

t_s is the minimum time before the transition of the clock that information must be present at the data input.

t_h is the minimum time after the transition of the clock that information must remain unchanged at the data input.

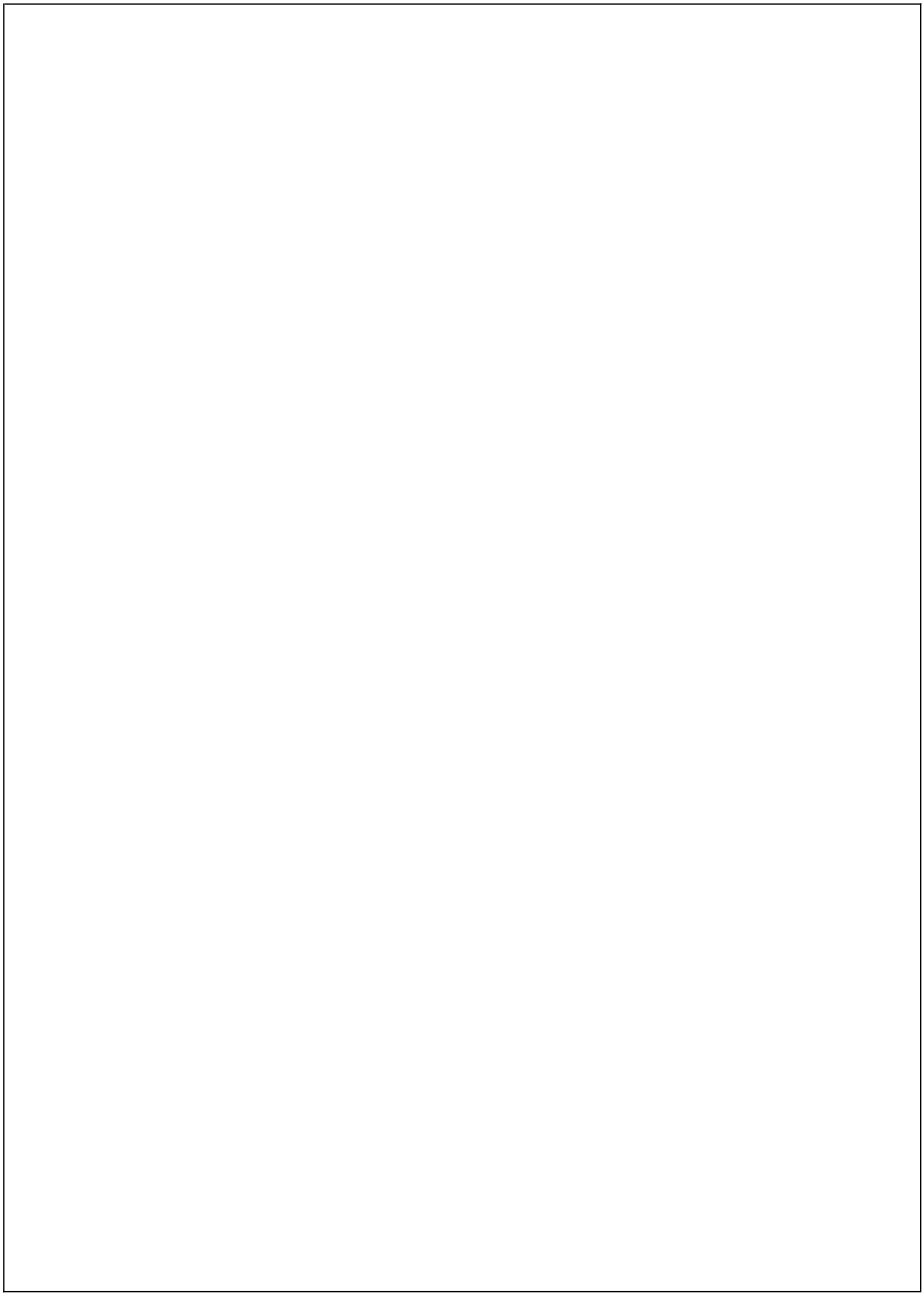
FIGURE 6. Data Setup and Hold Time



Note:

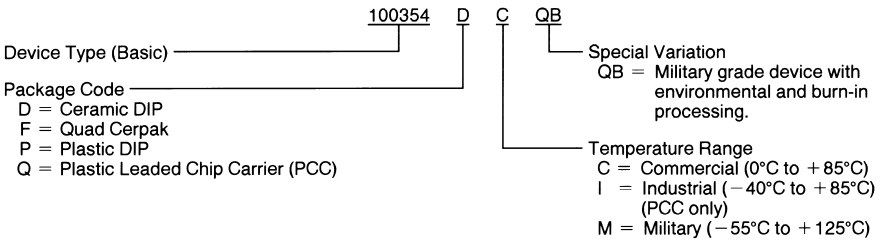
The output AC measurement point for cut-off propagation delay testing = the 50% voltage point between active V_{OL} and V_{OH}.

FIGURE 7. Cutoff Times



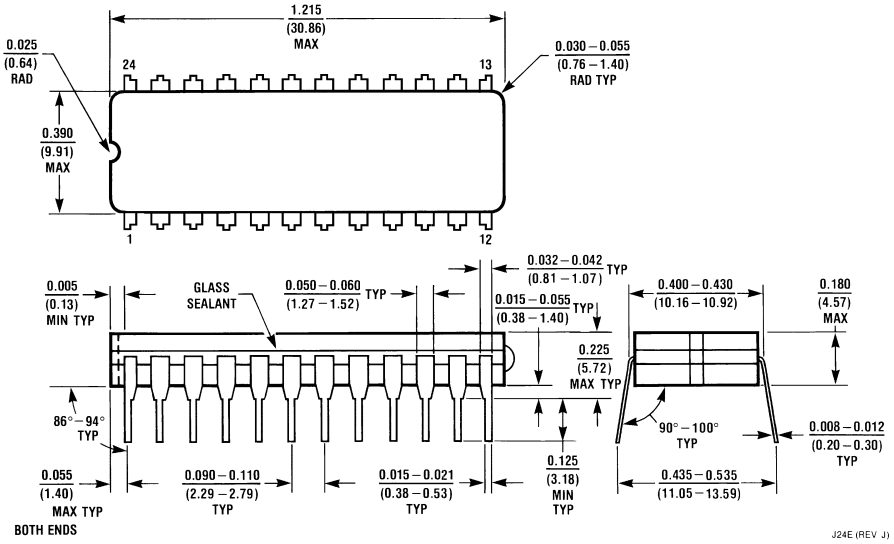
Ordering Information

The device number is used to form part of a simplified purchasing code where a package type and temperature range are defined as follows:



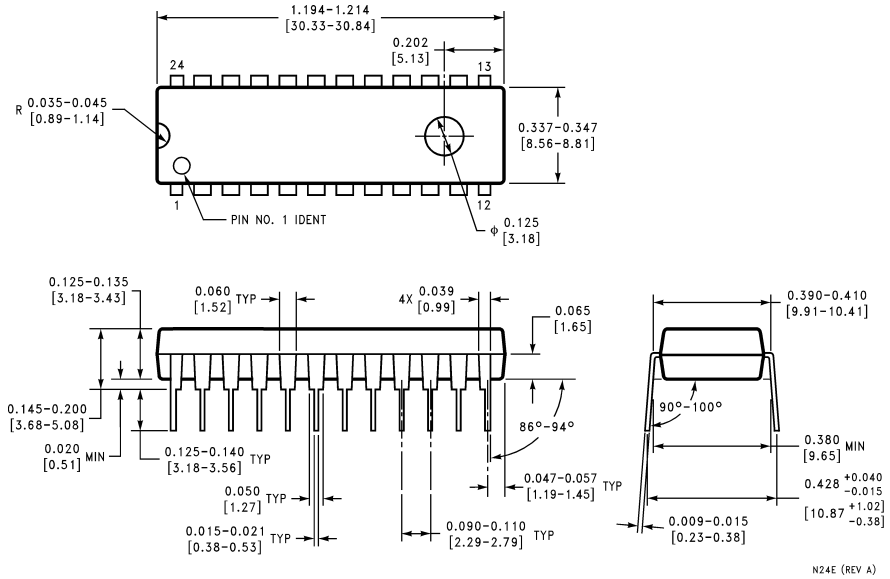
DS010610-12

Physical Dimensions inches (millimeters) unless otherwise noted



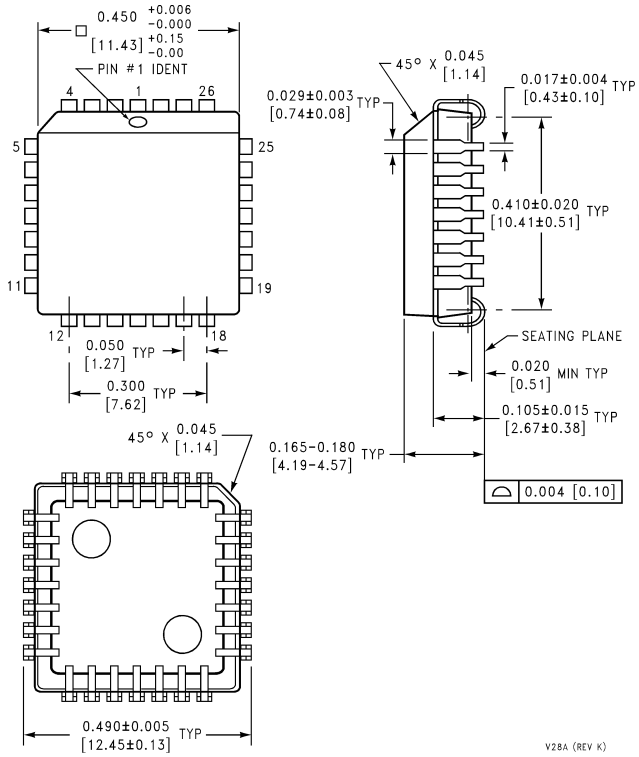
24-Lead Ceramic Dual-In-Line Package (D)
Package Number J24E

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



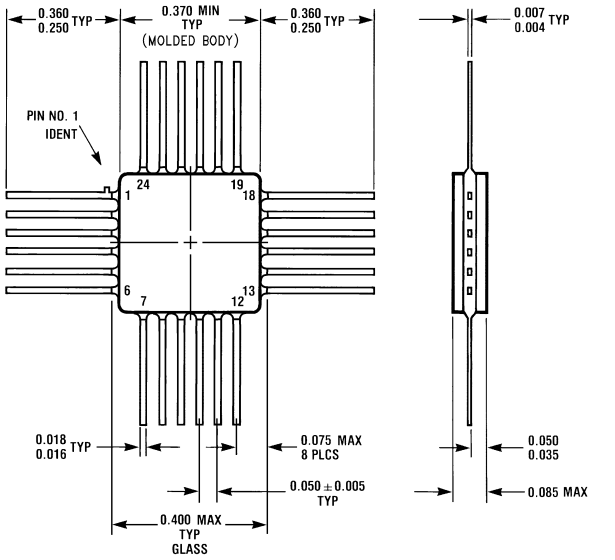
24-Lead Plastic Dual-in-Line Package (P)
Package Number N24E

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



28-Lead Plastic Chip Carrier (Q)
Package Number V28A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



28-Lead Quad Cerpak (F)
Package Number W24B

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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