

# 100363 Low Power Dual 8-Input Multiplexer

## General Description

The 100363 is a dual 8-input multiplexer. The Data Select ( $S_n$ ) inputs determine which bit ( $A_n$  and  $B_n$ ) will be presented at the outputs ( $Z_a$  and  $Z_b$  respectively). The same bit (0-7) will be selected for both the  $Z_a$  and  $Z_b$  output. All inputs have 50 k $\Omega$  pull-down resistors.

## Features

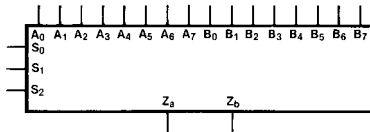
- 50% power reduction of the 100163
- 2000V ESD protection
- Pin/function compatible with 100163
- Voltage compensated operating range = -4.2V to -5.7V
- Available to industrial grade temperature range

## Ordering Code:

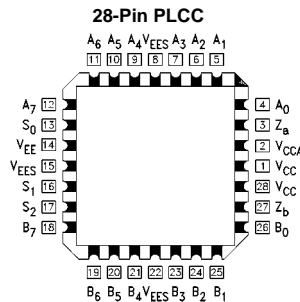
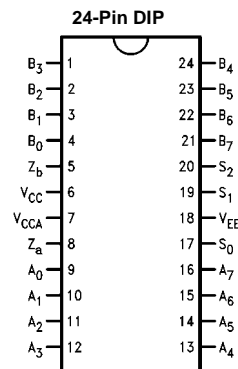
Order Number	Package Number	Package Description
100363PC	N24E	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-011, 0.400 Wide
100363QC	V28A	28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square
100363QI	V28A	28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square Industrial Temperature Range (-40°C to +85°C)

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

## Logic Symbol



## Connection Diagrams



## Pin Descriptions

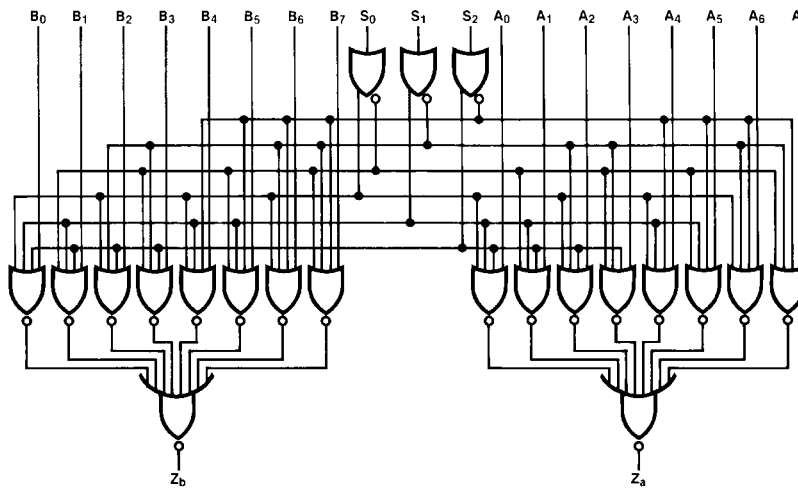
Pin Names	Description
$S_0$ - $S_2$	Data Select Inputs
$A_0$ - $A_7$	A Data Inputs
$B_0$ - $B_7$	B Data Inputs
$Z_a$ , $Z_b$	Data Outputs

### Truth Table

Inputs											Outputs	
Select			Data								Z <sub>a</sub>	Z <sub>b</sub>
S <sub>2</sub>	S <sub>1</sub>	S <sub>0</sub>	A <sub>7</sub> B <sub>7</sub>	A <sub>6</sub> B <sub>6</sub>	A <sub>5</sub> B <sub>5</sub>	A <sub>4</sub> B <sub>4</sub>	A <sub>3</sub> B <sub>3</sub>	A <sub>2</sub> B <sub>2</sub>	A <sub>1</sub> B <sub>1</sub>	A <sub>0</sub> B <sub>0</sub>	Z <sub>a</sub>	Z <sub>b</sub>
L	L	L								L	L	L
L	L	L								H	L	H
L	L	H							L		L	L
L	L	H							H		L	H
L	H	L						L			L	L
L	H	L						H			L	H
L	H	H					L				L	L
L	H	H					H				L	H
H	L	L				L					L	L
H	L	L				H					L	H
H	L	H			L						L	L
H	L	H			H						L	H
H	H	L		L							L	L
H	H	L		H							L	H
H	H	H	L								L	L
H	H	H	H								L	H

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 Blank = X = Don't Care

### Logic Diagram



**Absolute Maximum Ratings**(Note 1)

Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
Maximum Junction Temperature ( $T_J$ )	+150°C
$V_{EE}$ Pin Potential to Ground Pin	-7.0V to +0.5V
Input Voltage (DC)	$V_{EE}$ to +0.5V
Output Current (DC Output HIGH)	-50 mA
ESD (Note 2)	≥2000V

**Recommended Operating Conditions**

Case Temperature ( $T_C$ )	Commercial	0°C to +85°C
	Industrial	-40°C to +85°C
Supply Voltage ( $V_{EE}$ )		-5.7V to -4.2V

**Note 1:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Note 2:** ESD testing conforms to MIL-STD-883, Method 3015.

**Commercial Version****DC Electrical Characteristics** (Note 3)

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $T_C = 0°C$  to  $+85°C$

Symbol	Parameter	Min	Typ	Max	Units	Conditions
$V_{OH}$	Output HIGH Voltage	-1025	-955	-870	mV	$V_{IN} = V_{IH}$ (Max) Loading with 50Ω to -2.0V
$V_{OL}$	Output LOW Voltage	-1830	-1705	-1620	mV	or $V_{IL}$ (Min)
$V_{OHC}$	Output HIGH Voltage	-1035			mV	$V_{IN} = V_{IH}$ (Min) Loading with 50Ω to -2.0V
$V_{OLC}$	Output LOW Voltage			-1610	mV	or $V_{IL}$ (Max)
$V_{IH}$	Input HIGH Voltage	-1165		-870	mV	Guaranteed HIGH Signal for All Inputs
$V_{IL}$	Input LOW Voltage	-1830		-1475	mV	Guaranteed LOW Signal for All Inputs
$I_{IL}$	Input LOW Current	0.50			μA	$V_{IN} = V_{IL}$ (Min)
$I_{IH}$	Input HIGH Current			265 340	μA	$V_{IN} = V_{IH}$ (Max)
$I_{EE}$	Power Supply Current	-80		-40	mA	Inputs OPEN

**Note 3:** The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

**DIP AC Electrical Characteristics**

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = 0°C$		$T_C = +25°C$		$T_C = +85°C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
$t_{PLH}$	Propagation Delay							ns	Figure 1 and Figure 2
$t_{PHL}$	$A_0-A_7, B_0-B_7$ to Output	0.70	1.65	0.80	1.70	0.80	1.80		
$t_{PLH}$	Propagation Delay								
$t_{PHL}$	$S_0-S_2$ to Output	1.30	2.60	1.40	2.70	1.40	2.70		
$t_{TLH}$	Transition Time	0.45	1.30	0.45	1.30	0.45	1.30		
$t_{THL}$	20% to 80%, 80% to 20%								

**PLCC AC Electrical Characteristics**

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = 0°C$		$T_C = +25°C$		$T_C = +85°C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
$t_{PLH}$	Propagation Delay							ns	Figure 1 and Figure 2
$t_{PHL}$	$A_0-A_7, B_0-B_7$ to Output	0.70	1.65	0.80	1.70	0.80	1.80		
$t_{PLH}$	Propagation Delay								
$t_{PHL}$	$S_0-S_2$ to Output	1.30	2.60	1.40	2.70	1.40	2.70		
$t_{TLH}$	Transition Time	0.45	1.30	0.45	1.30	0.45	1.30		
$t_{THL}$	20% to 80%, 80% to 20%								

## Industrial Version

### DC Electrical Characteristics (Note 4)

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $T_C = -40^\circ C$  to  $+85^\circ C$

Symbol	Parameter	$T_C = -40^\circ C$		$T_C = 0^\circ C$ to $+85^\circ C$		Units	Conditions
		Min	Max	Min	Max		
$V_{OH}$	Output HIGH Voltage	-1085	-870	-1025	-870	mV	$V_{IN} = V_{IH}(\text{max})$ Loading with $50\Omega$ to $-2.0V$
$V_{OL}$	Output LOW Voltage	-1830	-1575	-1830	-1620	mV	or $V_{IL}(\text{min})$
$V_{OHC}$	Output HIGH Voltage	-1095		-1035		mV	$V_{IN} = V_{IH}(\text{min})$ Loading with $50\Omega$ to $-2.0V$
$V_{OLC}$	Output LOW Voltage		-1565		-1610	mV	or $V_{IL}(\text{max})$
$V_{IH}$	Input HIGH Voltage	-1170	-870	-1165	-870	mV	Guaranteed HIGH Signal for All Inputs
$V_{IL}$	Input LOW Voltage	-1830	-1480	-1830	-1475	mV	Guaranteed LOW Signal for All Inputs
$I_{IL}$	Input LOW Current	0.50		0.50		$\mu A$	$V_{IN} = V_{IL}(\text{min})$
$I_{IH}$	Input HIGH Current					$\mu A$	$V_{IN} = V_{IH}(\text{Max})$
	$S_n$		265		265		
	$A_n, B_n$		380		340		
$I_{EE}$	Power Supply Current	-80	-35	-80	-40	mA	Inputs OPEN

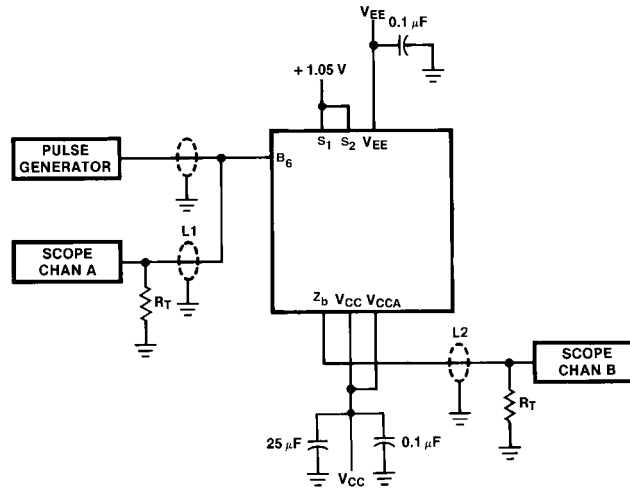
**Note 4:** The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

### AC Electrical Characteristics

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = -40^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
$t_{PLH}$	Propagation Delay	0.60	1.65	0.80	1.70	0.80	1.80	ns	Figure 1 and Figure 2
$t_{PHL}$	$A_0-A_7, B_0-B_7$ to Output								
$t_{PLH}$	Propagation Delay	1.20	2.60	1.40	2.70	1.40	2.70	ns	
$t_{PHL}$	$S_0-S_2$ to Output								
$t_{TLH}$	Transition Time	0.30	1.90	0.45	1.30	0.45	1.30	ns	
$t_{THL}$	20% to 80%, 80% to 20%								

### Test Circuitry



**Notes:**  
 $V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V$   
 L<sub>1</sub> and L<sub>2</sub> = equal length 50Ω impedance lines  
 $R_T = 50\Omega$  terminator internal to scope  
 Decoupling 0.1 μF from GND to V<sub>CC</sub> and V<sub>EE</sub>  
 All unused outputs are loaded with 50Ω to GND  
 $C_L =$  Fixture and stray capacitance  $\leq 3$  pF

FIGURE 1. AC Test Circuit

### Switching Waveforms

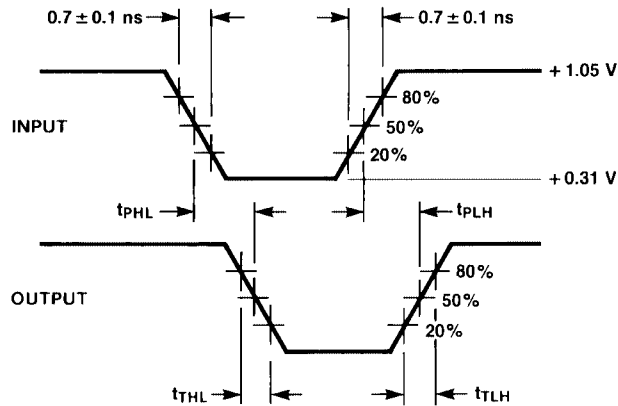
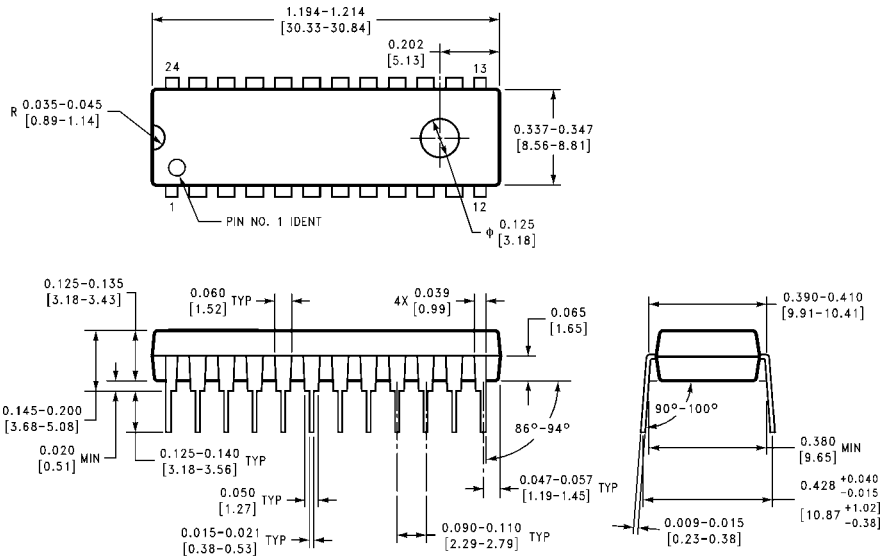


FIGURE 2. Propagation Delay and Transition Times

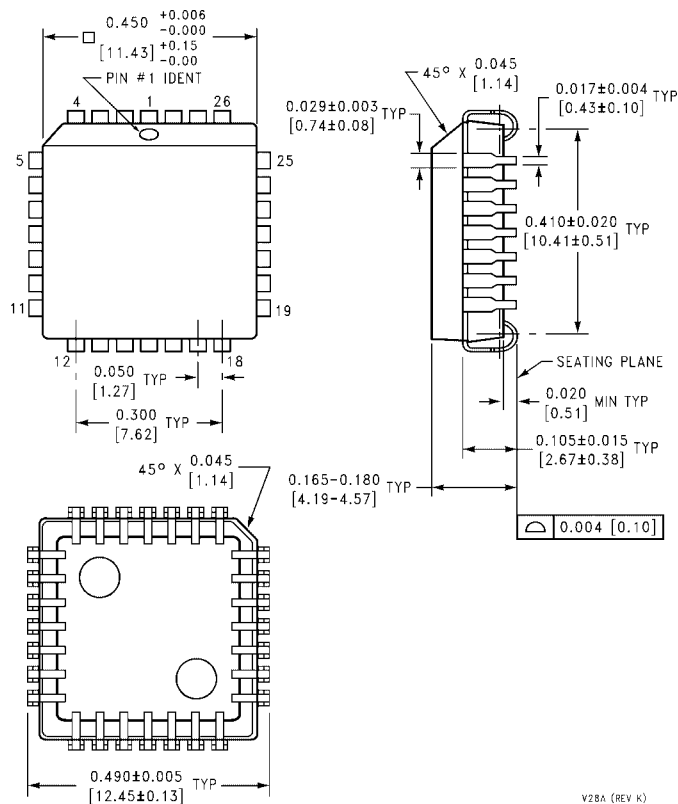
100363

**Physical Dimensions** inches (millimeters) unless otherwise noted



**24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-011, 0.400 Wide  
Package Number N24E**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square  
Package Number V28A**

V28A (REV K)

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