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P1 98.2

MOS FIELD EFFECT POWER TRANSISTOR
2SK1122

SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE

DESCRIPTION

The 2SK1122 is N-channel MOS Field Effect Transistor designed for solenoid, motor and lamp driver.

FEATURES

- Low On-state Resistance
 $R_{DS(on)} \leq 50 \text{ m}\Omega$ ($V_{GS} = 10 \text{ V}$, $I_D = 20 \text{ A}$)
 $R_{DS(on)} \leq 70 \text{ m}\Omega$ ($V_{GS} = 4 \text{ V}$, $I_D = 20 \text{ A}$)
- Low C_{iss} $C_{iss} = 3 \text{ 300 pF TYP.}$
- Built-in G-S Gate Protection Diodes

QUALITY GRADE

Standard

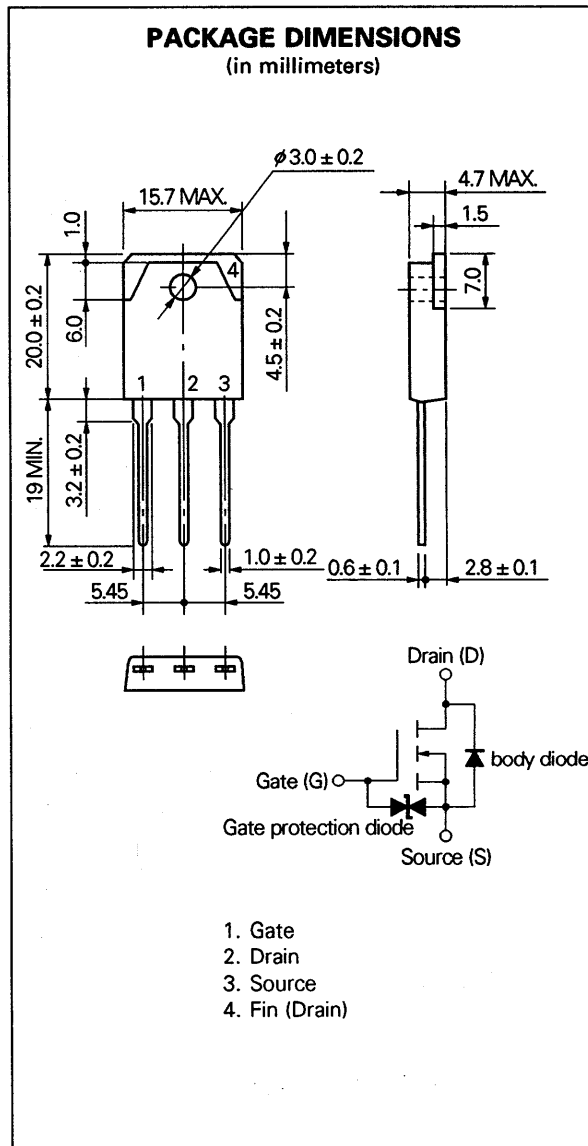
Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

ABSOLUTE MAXIMUM RATINGS ($T_a = 25 \text{ }^\circ\text{C}$)

Drain to Source Voltage	V_{DSS}	100	V
Gate to Source Voltage	$V_{GSS(AC)}$	± 20	V
Drain Current (DC)	$I_{D(DC)}$	± 40	A
Drain Current (pulse)	$I_{D(pulse)^*}$	± 160	A
Total Power Dissipation ($T_c = 25 \text{ }^\circ\text{C}$)	P_{T1}	100	W
Total Power Dissipation ($T_a = 25 \text{ }^\circ\text{C}$)	P_{T2}	3.0	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

* $PW \leq 10 \text{ } \mu\text{s}$, Duty Cycle $\leq 1 \%$

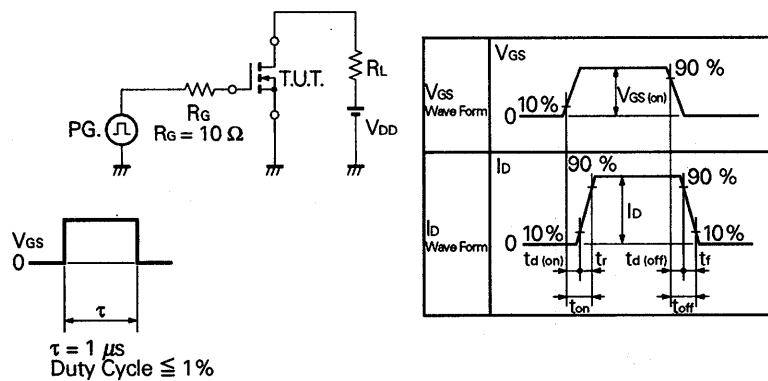
PACKAGE DIMENSIONS
 (in millimeters)



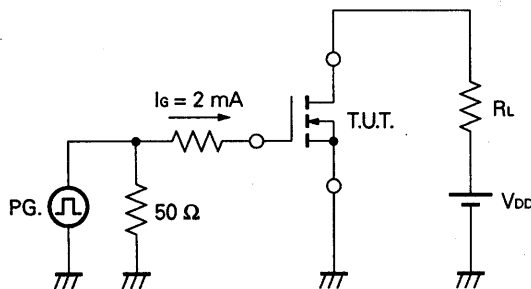
ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	R _{DS(on)}		42	50	mΩ	V _{GS} = 10 V, I _D = 20 A
Drain to Source On-state Resistance	R _{DS(on)}		50	70	mΩ	V _{GS} = 4.0 V, I _D = 20 A
Gate to Source Cutoff Voltage	V _{GS(off)}	1.0		2.5	V	V _{DS} = 10 V, I _D = 1 mA
Forward Transfer Admittance	y _{fs}	12			S	V _{DS} = 10 V, I _D = 20 A
Drain Leakage Current	I _{DSS}			10	μA	V _{DS} = 100 V, V _{GS} = 0
Gate to Source Leakage Current	I _{GSS}			±10	μA	V _{GS} = ±20 V, V _{DS} = 0
Input Capacitance	C _{iss}		3300		pF	V _{DS} = 10 V
Output Capacitance	C _{oss}		800		pF	V _{GS} = 0
Reverse Transfer Capacitance	C _{res}		200		pF	f = 1 MHz
Turn-On Delay Time	t _{d(on)}		40		ns	V _{GS(on)} = 10 V
Rise Time	t _r		210		ns	V _{DD} = 50 V
Turn-Off Delay Time	t _{d(off)}		210		ns	I _D = 20 A, R _G = 10 Ω
Fall Time	t _f		155		ns	R _L = 2.5 Ω
Total Gate Charge	Q _G		80		nC	V _{GS} = 10 V
Gate to Source Charge	Q _{GS}		10		nC	I _D = 40 A
Gate to Drain Charge	Q _{GD}		30		nC	V _{DD} = 80 V
Diode Forward Voltage	V _{SD}		1.2		V	I _{SD} = 40 A, V _{GS} = 0
Reverse Recovery Time	t _{rr}		210		ns	I _F = 40 A, V _{GS} = 0
Reverse Recovery Charge	Q _{rr}		600		nC	di/dt = 50 A/μs

Test Circuit 1: Switching Time

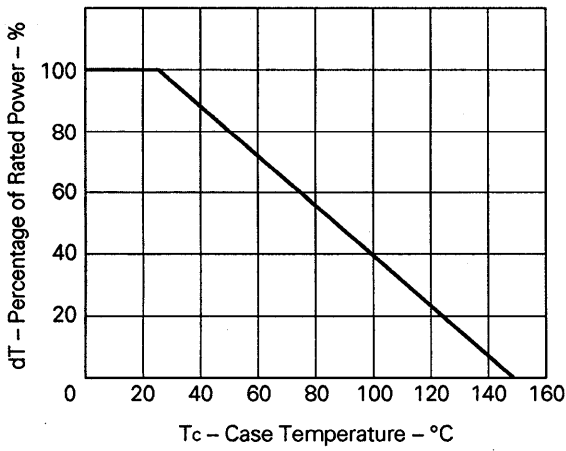


Test Circuit 2: Gate Charge

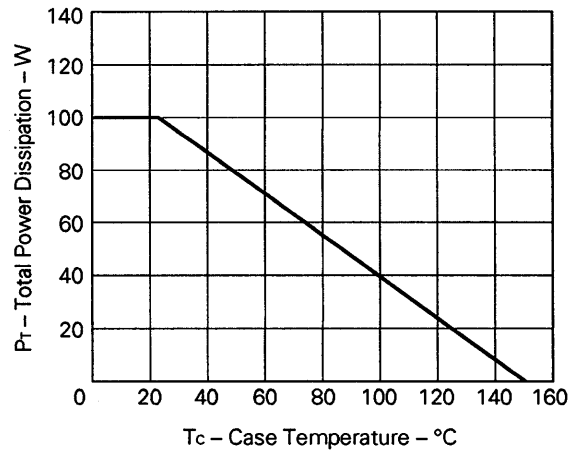


TYPICAL CHARACTERISTICS (T_a = 25 °C)

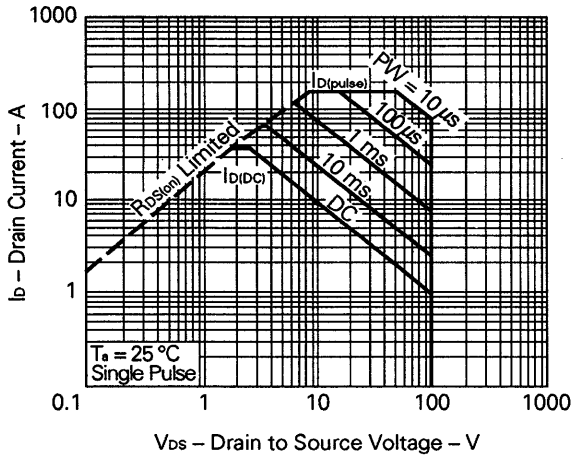
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



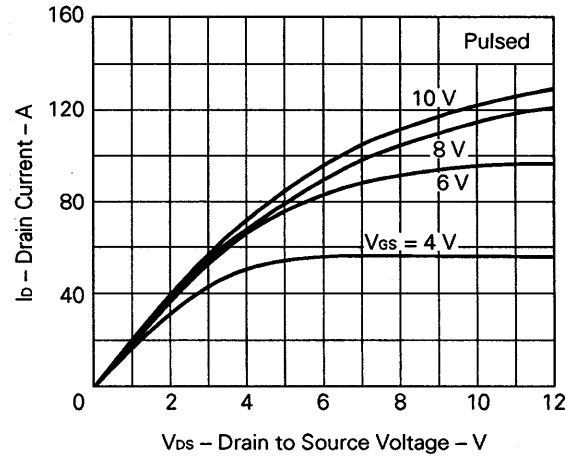
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



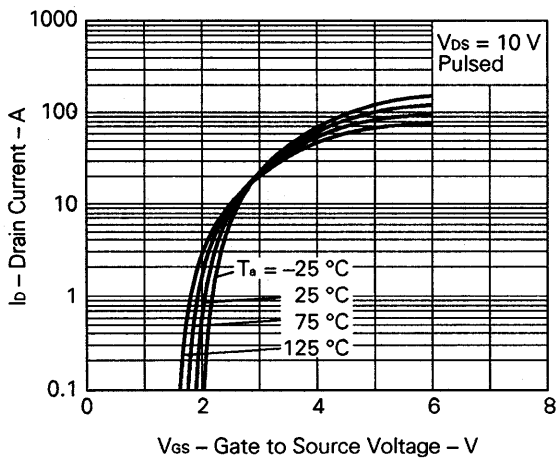
FORWARD BIAS SAFE OPERATING AREA

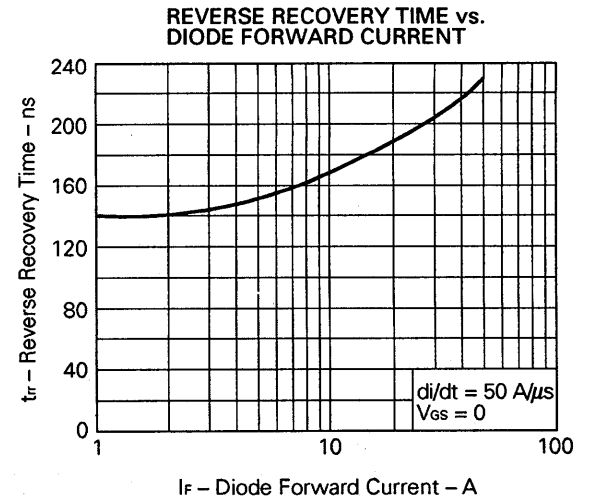
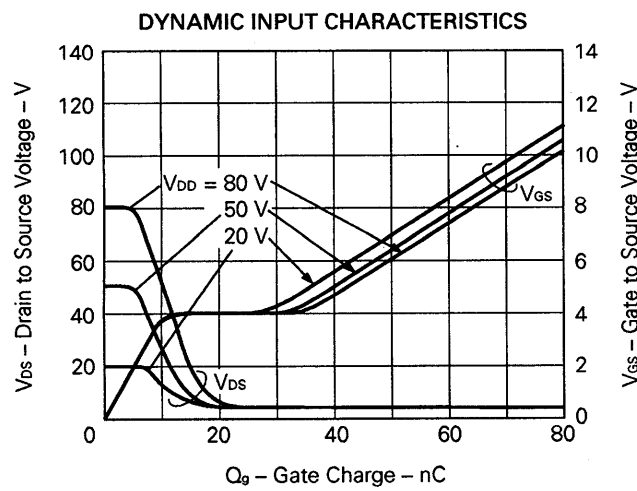
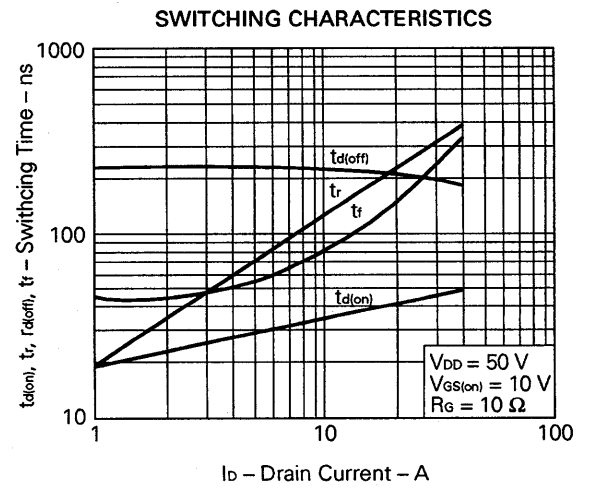
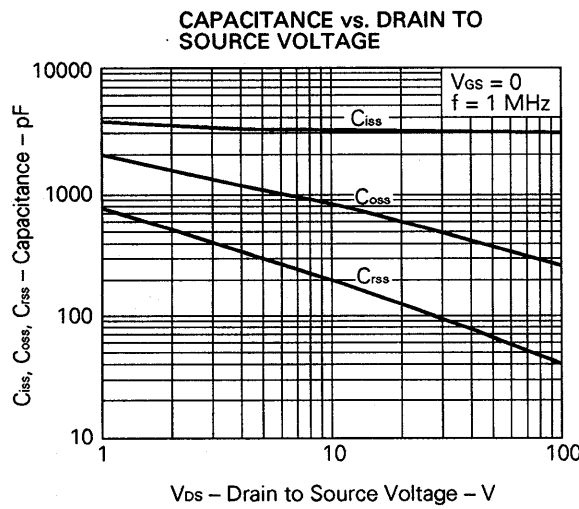
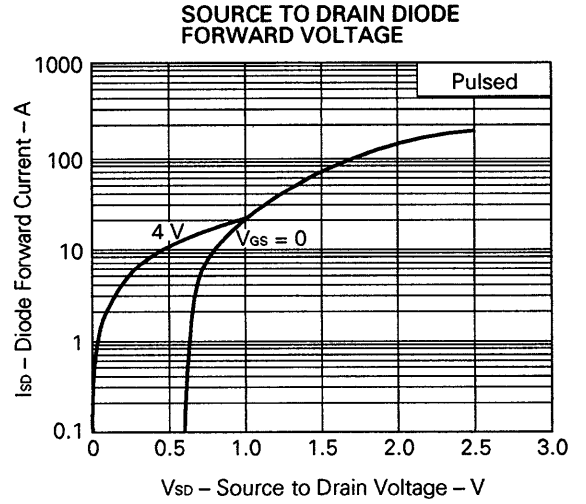
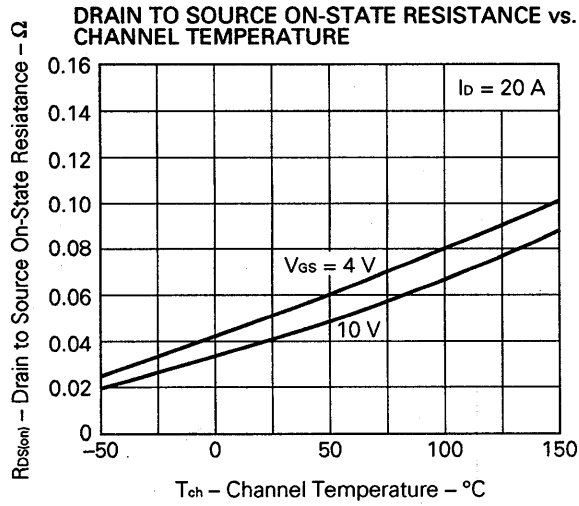


DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE

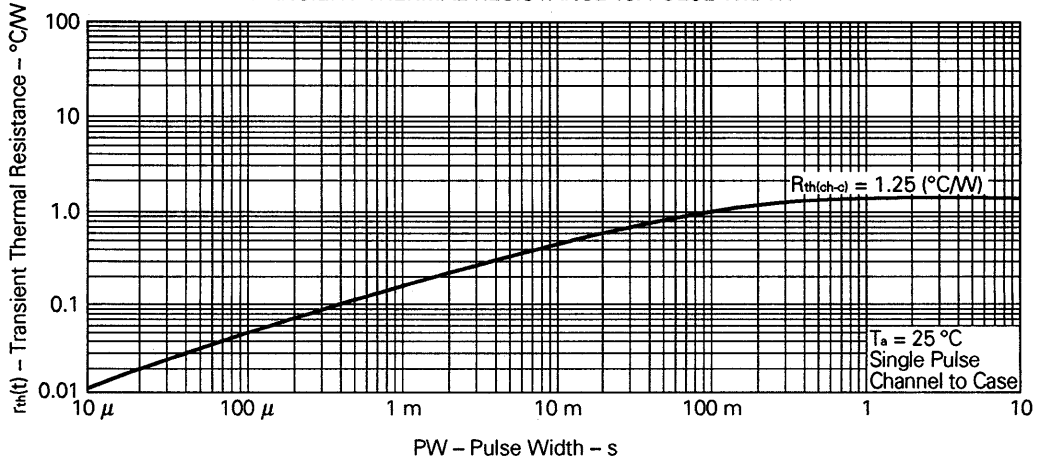


TRANSFER CHARACTERISTICS

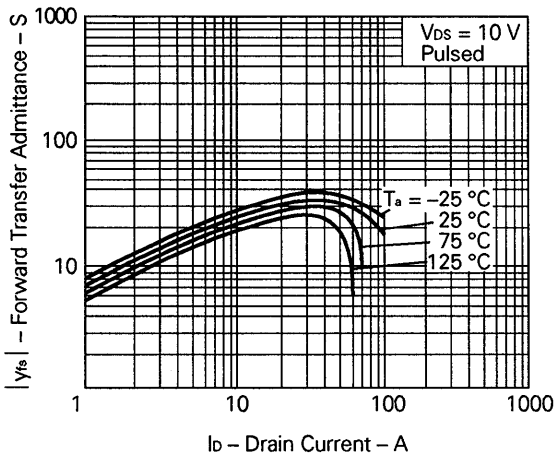




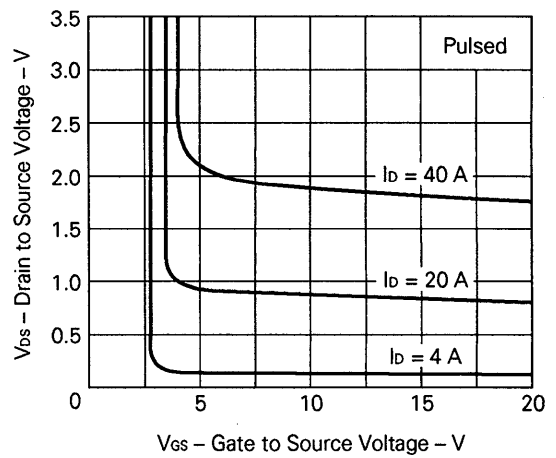
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



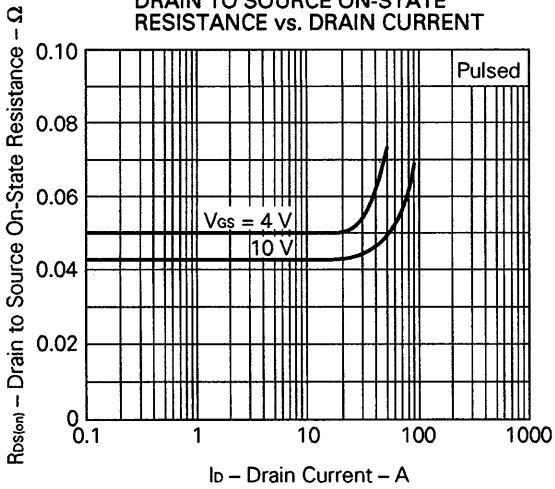
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



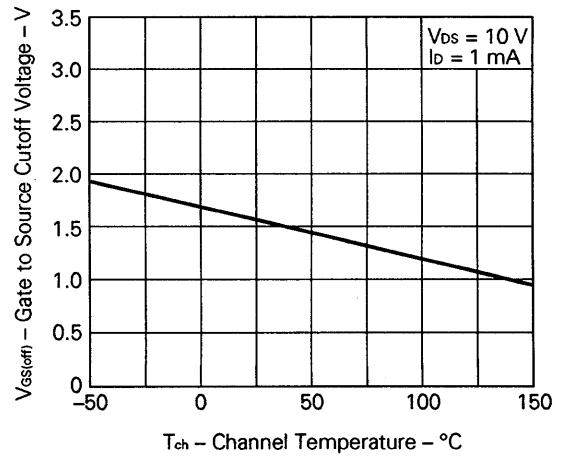
DRAIN TO SOURCE VOLTAGE vs. GATE TO SOURCE VOLTAGE



DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE



REFERENCE

Application note name	No.
Safe operating area of Power MOS FET.	TEA-1034
Application circuit using Power MOS FET.	TEA-1035
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207

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