HITACHI

# 2SK1151Ⓛ , 2SK1152Ⓛ , 2SK1151Ⓢ , 2SK1152Ⓢ

**Silicon N-Channel MOS FET**

## Application

High speed power switching

## Features

- Low on-resistance
- High speed switching
- Low drive current
- No secondary breakdown
- Suitable for switching regulator and DC-DC converter

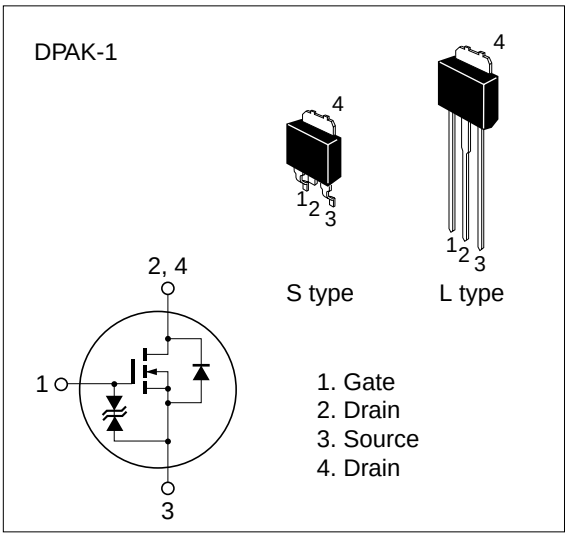



**Table 1 Absolute Maximum Ratings** (Ta = 25°C)

| Item | | Symbol | Ratings | Unit |
|---|---|---|---|---|
| Drain to source voltage | 2SK1151 | $V_{DSS}$ | 450 | V |
| | 2SK1152 | | 500 | |
| Gate to source voltage | | $V_{GSS}$ | ±30 | V |
| Drain current | | $I_D$ | 1.5 | A |
| Drain peak current | | $I_{D(pulse)}$* | 6 | A |
| Body to drain diode reverse drain current | | $I_{DR}$ | 1.5 | A |
| Channel dissipation | | Pch** | 20 | W |
| Channel temperature | | Tch | 150 | °C |
| Storage temperature | | Tstg | –55 to +150 | °C |

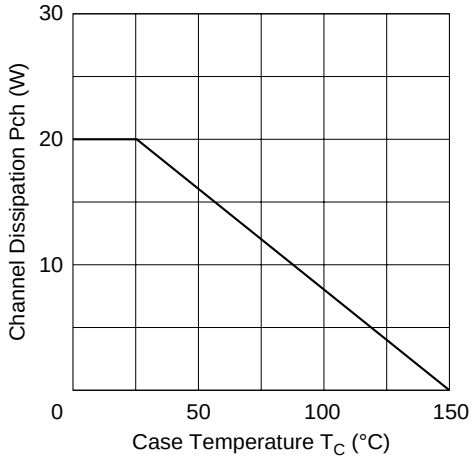
* PW ≤ 10 µs, duty cycle ≤ 1 %
** Value at $T_C$ = 25 °C

**Table 2 Electrical Characteristics** (Ta = 25°C)

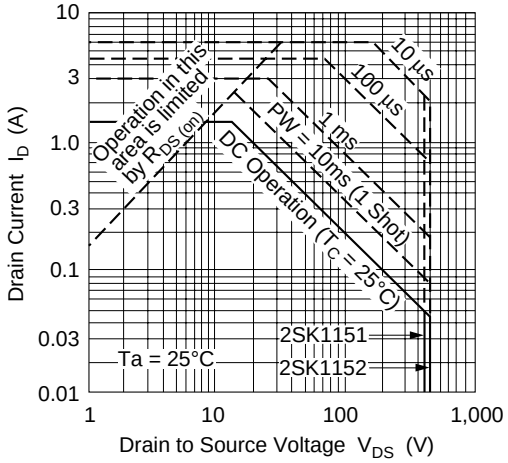
| Item | | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Drain to source breakdown voltage | 2SK1151 | $V_{(BR)DSS}$ | 450 | — | — | V | $I_D$ = 10 mA, $V_{GS}$ = 0 |
| | 2SK1152 | | 500 | | | | |
| Gate to source breakdown voltage | | $V_{(BR)GSS}$ | ±30 | — | — | V | $I_G$ = ±100 µA, $V_{DS}$ = 0 |
| Gate to source leak current | | $I_{GSS}$ | — | — | ±10 | µA | $V_{GS}$ = ±25 V, $V_{DS}$ = 0 |
| Zero gate voltage drain current | 2SK1151 | $I_{DSS}$ | — | — | 100 | µA | $V_{DS}$ = 360 V, $V_{GS}$ = 0 |
| | 2SK1152 | | | | | | $V_{DS}$ = 400 V, $V_{GS}$ = 0 |
| Gate to source cutoff voltage | | $V_{GS(off)}$ | 2.0 | — | 3.0 | V | $I_D$ = 1 mA, $V_{DS}$ = 10 V |
| Static Drain to source on state resistance | 2SK1151 | $R_{DS(on)}$ | — | 3.5 | 5.5 | Ω | $I_D$ = 1 A, $V_{GS}$ = 10 V * |
| | 2SK1152 | | — | 4.0 | 6.0 | | |
| Forward transfer admittance | | $\|y_{fs}\|$ | 0.6 | 1.1 | — | S | $I_D$ = 1 A, $V_{DS}$ = 20 V * |
| Input capacitance | | Ciss | — | 160 | — | pF | $V_{DS}$ = 10 V, $V_{GS}$ = 0, f = 1 MHz |
| Output capacitance | | Coss | — | 45 | — | pF | |
| Reverse transfer capacitance | | Crss | — | 5 | — | pF | |
| Turn-on delay time | | $t_{d(on)}$ | — | 5 | — | ns | $I_D$ = 1 A, $V_{GS}$ = 10 V, $R_L$ = 30 Ω |
| Rise time | | $t_r$ | — | 10 | — | ns | |
| Turn-off delay time | | $t_{d(off)}$ | — | 20 | — | ns | |
| Fall time | | $t_f$ | — | 10 | — | ns | |
| Body to drain diode forward voltage | | $V_{DF}$ | — | 1.0 | — | V | $I_F$ = 1.5 A, $V_{GS}$ = 0 |
| Body to drain diode reverse recovery time | | $t_{rr}$ | — | 220 | — | ns | $I_F$ = 1.5 A, $V_{GS}$ = 0, $di_F/dt$ = 100 A/µs |

* Pulse Test

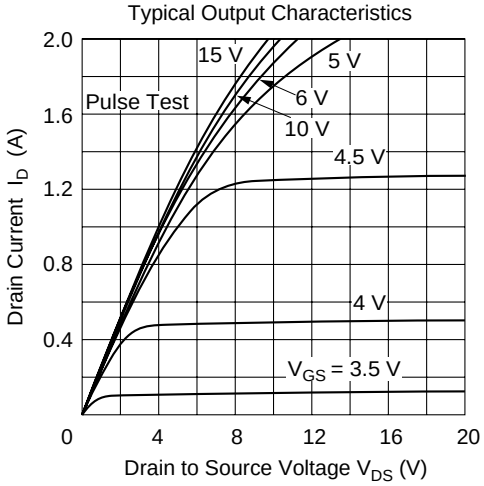
Power vs. Temperature Derating



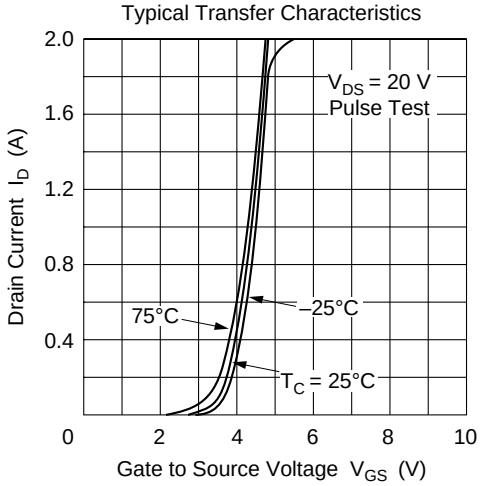

Maximum Safe Operation Area



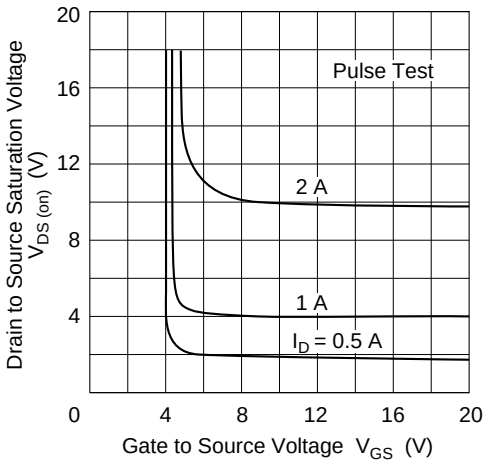

Typical Output Characteristics



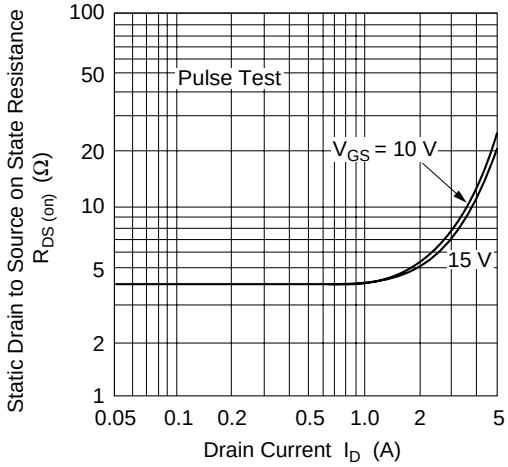

Typical Transfer Characteristics



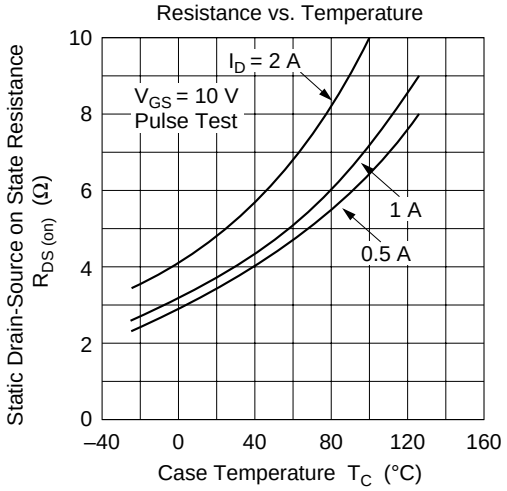
Drain to Source Saturation Voltage vs. Gate to Source Voltage



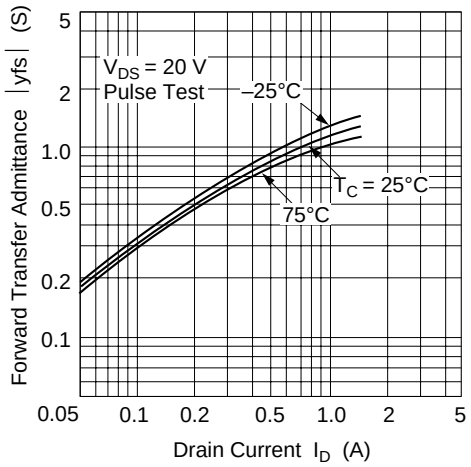

Static Drain to Source on State Resistance vs. Drain Current



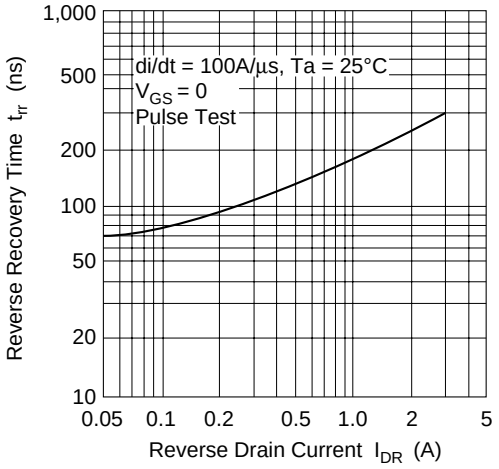

Static Drain to Source on State Resistance vs. Temperature



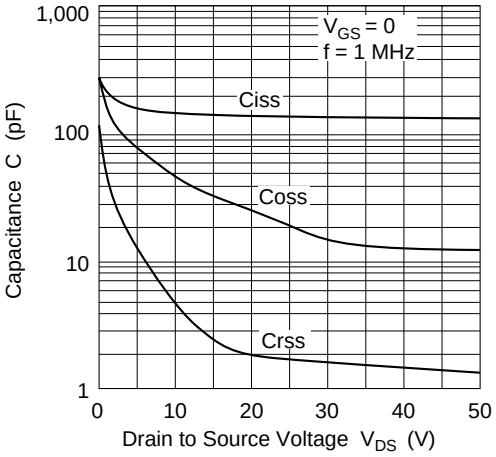

Forward Transfer Admittance vs. Drain Current



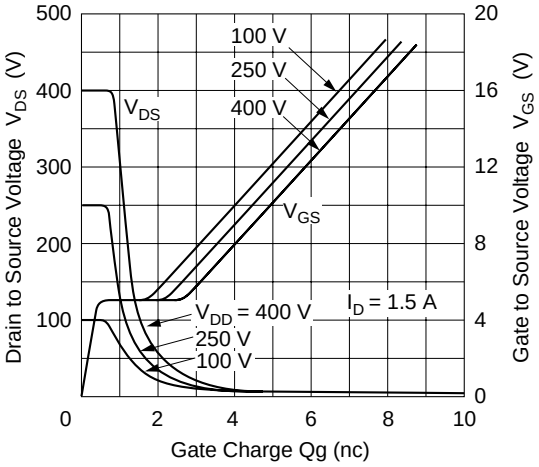
Body to Drain Diode Reverse Recovery Time



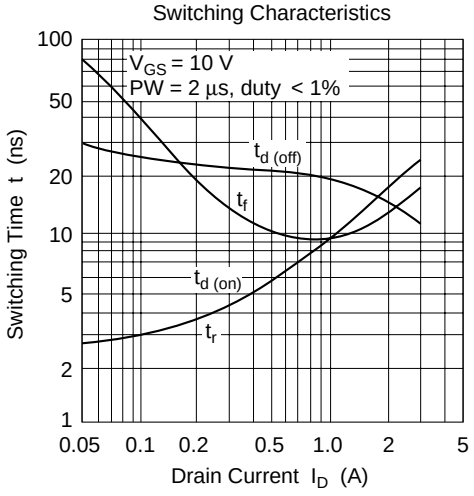

Typical Capacitance vs. Drain to Source Voltage

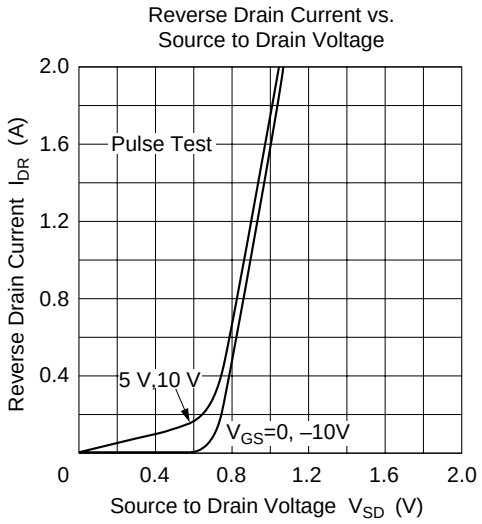


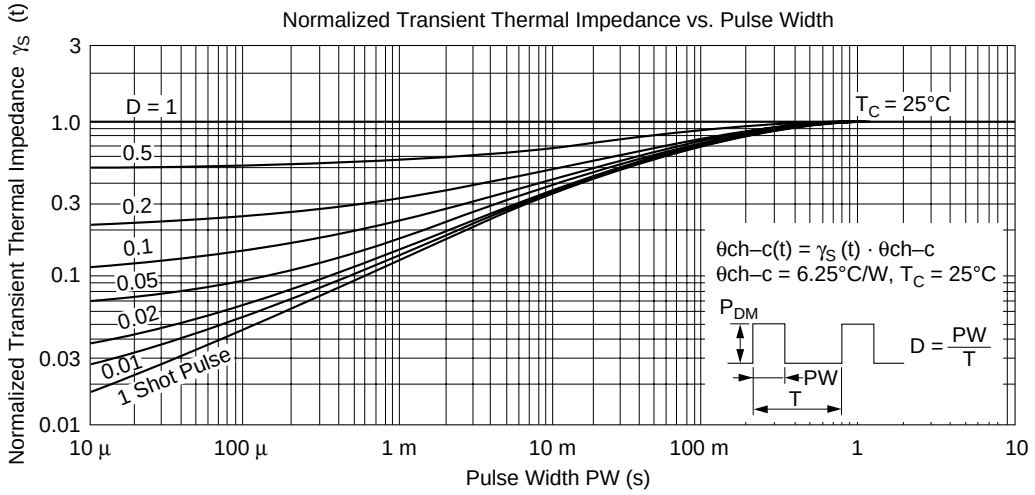

Dynamic Input Characteristics



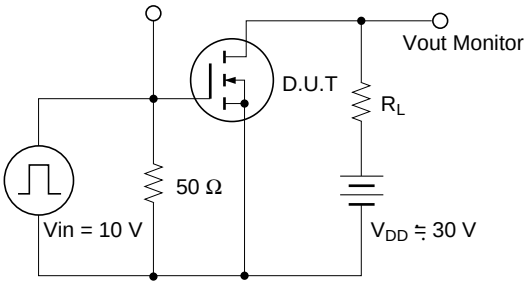

Switching Characteristics




Reverse Drain Current vs.
Source to Drain Voltage
Reverse Drain Current $I_{DR}$ (A)
2.0
1.6
1.2
0.8
0.4
0
Pulse Test
5 V, 10 V
$V_{GS}$=0, –10V
0.4
0.8
1.2
1.6
2.0
Source to Drain Voltage $V_{SD}$ (V)


Normalized Transient Thermal Impedance vs. Pulse Width
Normalized Transient Thermal Impedance $\gamma_S$ (t)
3
1.0
0.3
0.1
0.03
0.01
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1 Shot Pulse
$T_C$ = 25°C
θch–c(t) = $\gamma_S$ (t) · θch–c
θch–c = 6.25°C/W, $T_C$ = 25°C
$P_{DM}$
PW
T
D = PW / T
10 µ
100 µ
1 m
10 m
100 m
1
10
Pulse Width PW (s)

Switching Time Test Circuit




Wavewforms