DATA SHEET

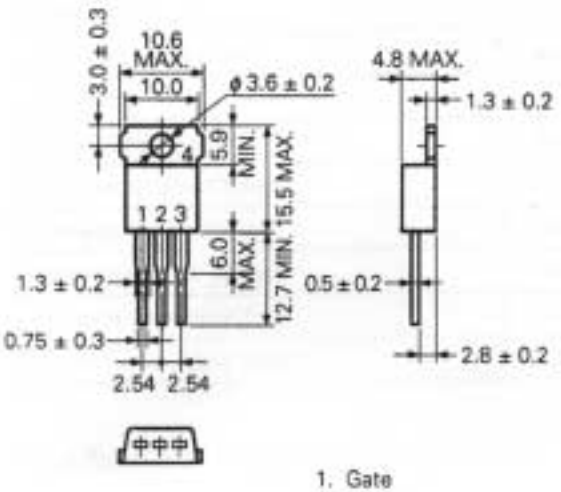
NEC

N-CHANNEL MOS FIELD EFFECT POWER TRANSISTOR

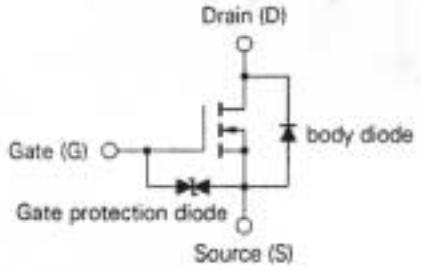
2SK1287

SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE

PACKAGE DIMENSIONS
(in millimeters)



1. Gate
2. Drain
3. Source
4. Fin (Drain)



DESCRIPTION

The 2SK1287 is N-channel MOS Field Effect Transistor designed for solenoid, motor and lamp driver.

FEATURES

- Low On-state Resistance
  $R_{DS(on)}$ ≦ 70 mΩ MAX. (V_{GS} = 10 V, I_D = 10 A)
  $R_{DS(on)}$ ≦ 95 mΩ MAX. (V_{GS} = 4 V, I_D = 10 A)
- Low C_{iss} C_{iss} = 1 400 pF TYP.
- Built-in G-S Gate Protection Diodes

QUALITY GRADE

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

ABSOLUTE MAXIMUM RATINGS

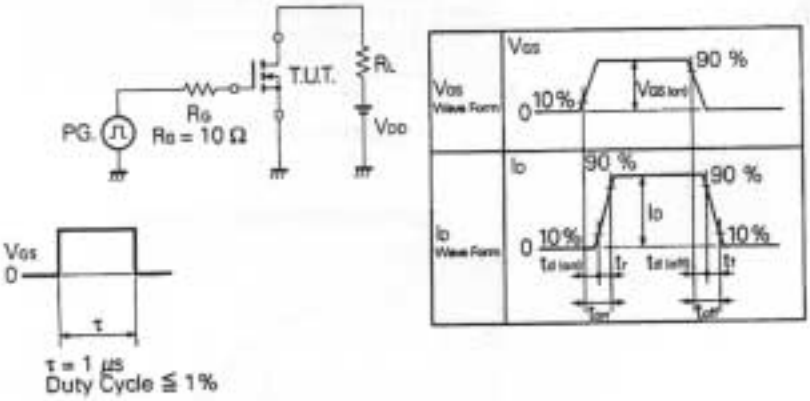
Maximum Temperatures			
Storage Temperature		−55 to +150	°C
Channel Temperature		150	°C MAX.
Maximum Power Dissipation			
Total Power Dissipation (T_a = 25 °C)		1.5	W
Total Power Dissipation (T_C = 25 °C)		60	W
Maximum Voltages and Currents (T_a = 25 °C)			
V_{DSS}	Drain to Source Voltage	60	V
$V_{GSS(AC)}$	Gate to Source Voltage	±20	V
$I_{D(DC)}$	Drain Current (DC)	±15	A
$I_{D(pulse)}$*	Drain Current (pulse)	±80	A

* PW ≦ 10 μs, Duty Cycle ≦ 1 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	$R_{DS(on)}$		55	70	mΩ	V_{GS} = 10 V, I_D = 10 A
Drain to Source On-state Resistance	$R_{DS(on)}$		80	95	mΩ	V_{GS} = 4.0 V, I_D = 10 A
Gate to Source Cutoff Voltage	$V_{GS(off)}$	1.0		2.5	V	V_{DS} = 10 V, I_D = 1 mA
Forward Transfer Admittance	$\|y_{fs}\|$	7.0	14		S	V_{DS} = 10 V, I_D = 10 A
Drain Leakage Current	I_{DSS}			10	μA	V_{DS} = 60 V, V_{GS} = 0
Gate to Source Leakage Current	I_{GSS}			±10	μA	V_{GS} = ±20 V, V_{DS} = 0
Input Capacitance	C_{iss}		1 400		pF	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz
Output Capacitance	C_{oss}		500		pF	
Reverse Transfer Capacitance	C_{rss}		130		pF	
Turn-On Delay Time	$t_{d(on)}$		25		ns	$V_{GS(on)}$ = 10 V V_{DD} = 30 V I_D = 10 A, R_G = 10 Ω R_L = 3.0 Ω
Rise Time	t_r		160		ns	
Turn-Off Delay Time	$t_{d(off)}$		130		ns	
Fall Time	t_f		80		ns	
Total Gate Charge	Q_G		30		nC	V_{GS} = 10 V I_D = 20 A V_{DD} = 48 V
Gate to Source Charge	Q_{GS}		5		nC	
Gate to Drain Charge	Q_{GD}		10		nC	
Diode Forward Voltage	V_{SD}		1.0		V	I_{SD} = 20 A, V_{GS} = 0
Reverse Recovery Time	t_{rr}		150		ns	I_F = 20 A, V_{GS} = 0 di/dt = 50 A/μs
Reverse Recovery Charge	Q_{rr}		250		nC	

Test Circuit 1: Switching Time



Test Circuit 2: Gate Charge