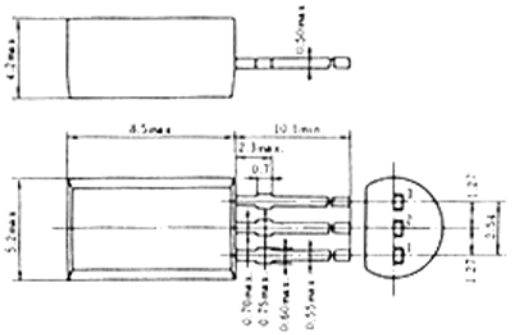
HITACHI

2SK190

SILICON N-CHANNEL JUNCTION FET

LOW FREQUENCY LOW NOISE AMPLIFIER



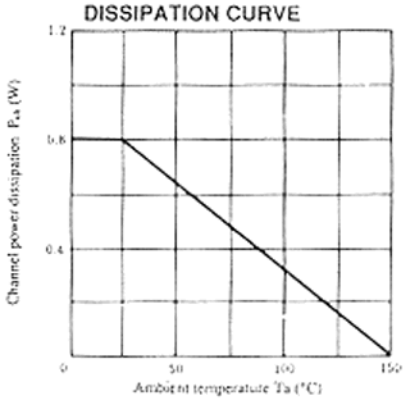
(JEDEC TO-92MOD.)

■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	2SK190	Unit
Gate to drain voltage	V_{GDO}	−40	V
Drain to source voltage	V_{DSX}*	40	V
Gate to source voltage	V_{GSS}	−40	V
Drain current	I_D	200	mA
Gate current	I_G	10	mA
Channel power dissipation	P_{ch}	800	mW
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	−55 to +150	°C

* Value at V_{GS}=−2V

MAXIMUM CHANNEL POWER DISSIPATION CURVE



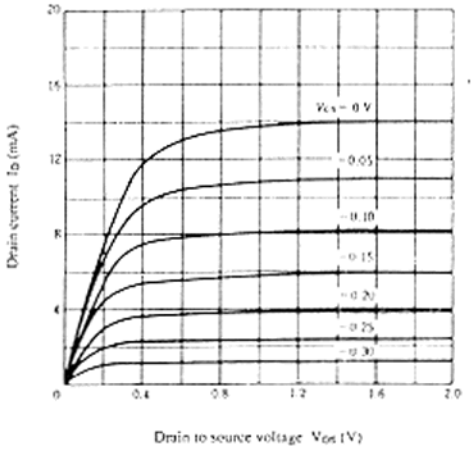
■ ELECTRICAL CHARACTERISTICS (Ta=25°C)

Item	Symbol	Test Condition	min.	typ.	max.	Unit
Gate to drain breakdown voltage	$V_{(BR)GDO}$	I_G = −100μA, I_S = 0	−40	—	—	V
Drain to source breakdown voltage	$V_{(BR)DSX}$	I_D = 100μA, V_{GS} = −2V	40	—	—	V
Gate cutoff current	I_{GSS}	V_{GS} = −30V, V_{DS} = 0	—	—	−10	nA
Drain current	I_{DSS}*	V_{DS} = 10V, V_{GS} = 0	6	—	50	mA
Gate to source cutoff voltage	$V_{GS(off)}$	V_{DS} = 10V, I_D = 10μA	−0.13	—	−1.5	V
Forward transfer admittance	$\|y_{fs}\|$	V_{DS} = 10V, I_D = 5mA, f = 1kHz	37	45	—	mS
Input capacitance	C_{iss}	V_{DS} = 10V, I_D = 5mA, f = 1MHz	—	75	—	pF
Noise voltage referred to input	e_n	V_{DS} = 10V, R_g = 0, I_D = 5mA, f = 1kHz	—	0.75	—	nV/√Hz
Output noise voltage	V_N	See Test Circuit	—	—	15	mV

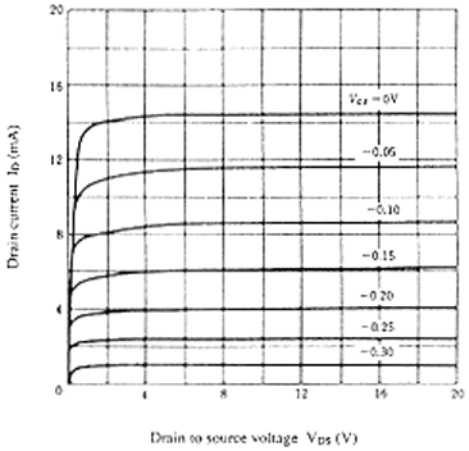
* The 2SK190 is grouped by I_{DSS} as follows.

E	F	G	H
6 to 12	10 to 20	16 to 32	25 to 50

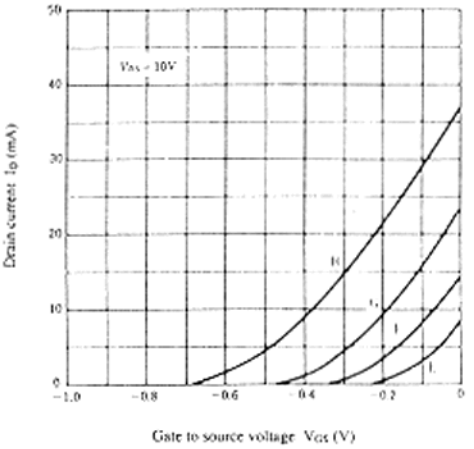
TYPICAL OUTPUT CHARACTERISTICS



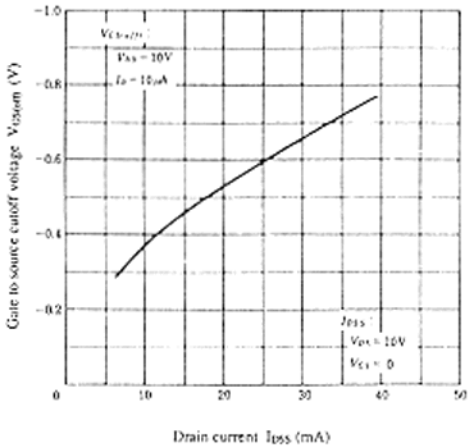
TYPICAL OUTPUT CHARACTERISTICS



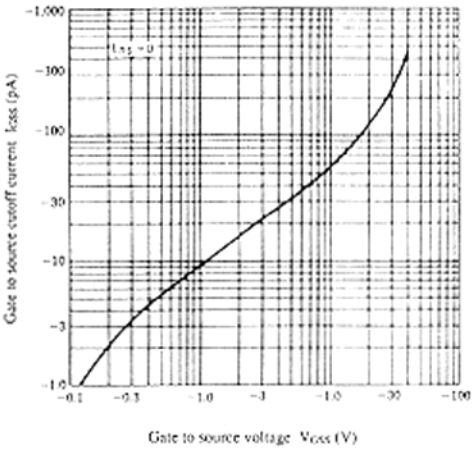
TYPICAL TRANSFER CHARACTERISTICS



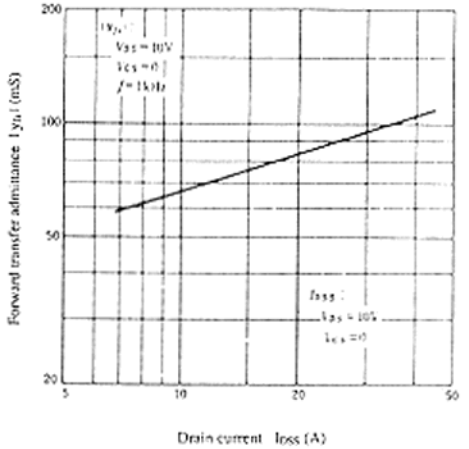
GATE TO SOURCE CUT-OFF VOLTAGE VS. DRAIN CURRENT



GATE TO SOURCE CUTOFF CURRENT VS. GATE TO SOURCE VOLTAGE



FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



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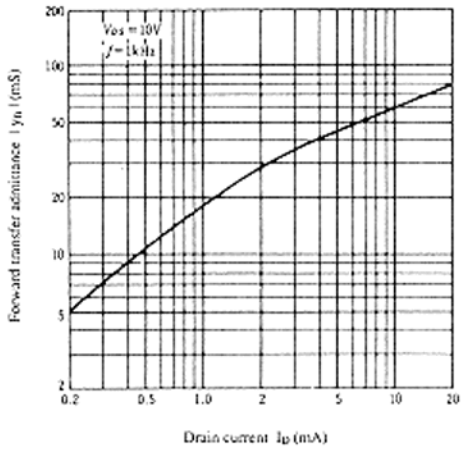
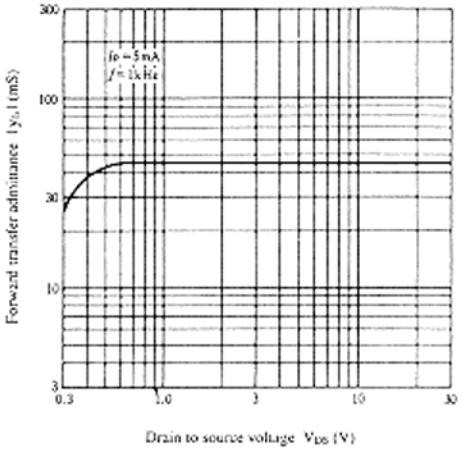
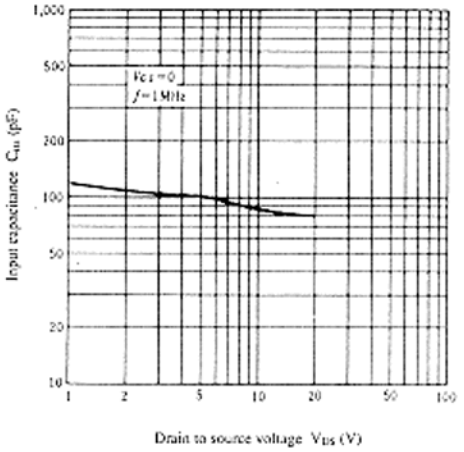
FORWARD TRANSFER ADMITTANCE VS. DRAIN CURRENT



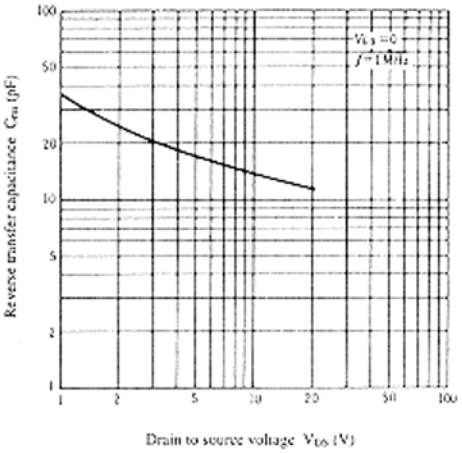
FORWARD TRANSFER ADMITTANCE VS. DRAIN TO SOURCE VOLTAGE



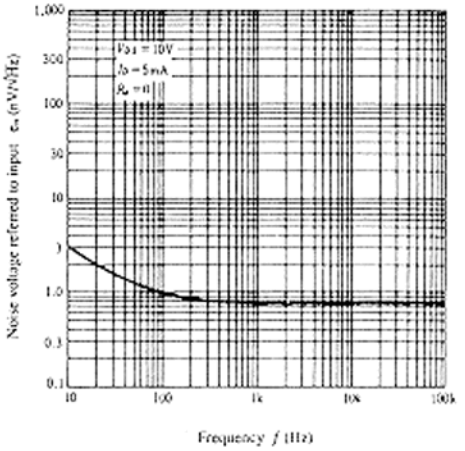
INPUT CAPACITANCE VS. DRAIN TO SOURCE VOLTAGE



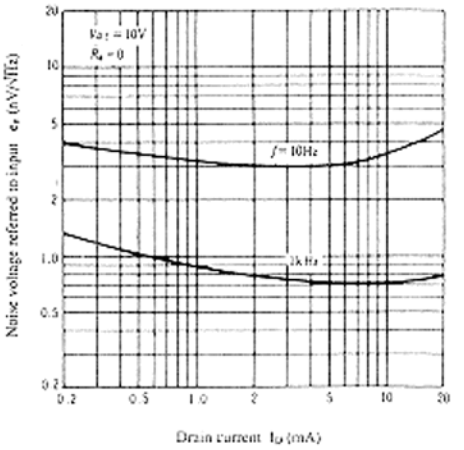
REVERSE TRANSFER CAPACITANCE VS. DRAIN TO SOURCE VOLTAGE



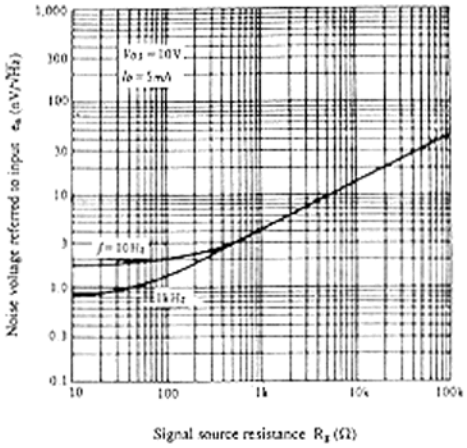
NOISE VOLTAGE REFERRED TO INPUT VS. FREQUENCY



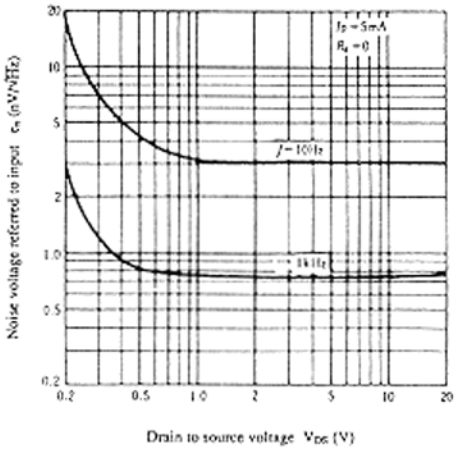
NOISE VOLTAGE REFERRED TO INPUT VS. DRAIN CURRENT



NOISE VOLTAGE REFERRED TO INPUT
VS. SIGNAL SOURCE RESISTANCE



NOISE VOLTAGE REFERRED TO INPUT
VS. DRAIN TO SOURCE VOLTAGE



V_N TEST CIRCUIT