N-CHANNEL MOS FIELD EFFECT POWER TRANSISTOR

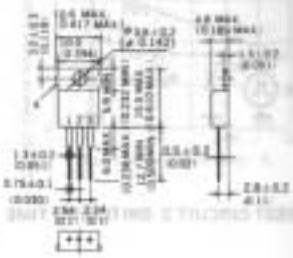
2SK812

DESCRIPTION The 2SK812 is N-Channel MOS Field Effect Power Transistor designed for solenoid, motor and lamp driver.

FEATURES

- 4 V Gate Drive – Logic level –
- Low $R_{DS(on)}$
- No Secondary Breakdown
- High Unclamped Sustaining Energy

PACKAGE DIMENSIONS
in millimeters (inches)



1. Gate
2. Drain
3. Source
4. Fin (Drain)

JEDEC: TO-220AB

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures

Storage Temperature	−55 to +150	°C
Channel Temperature	150 Maximum	°C

Maximum Power Dissipations

Total Power Dissipation (T_a = 25 °C)	1.5	W
Total Power Dissipation (T_c = 25 °C)	60	W

Maximum Voltages and Currents (T_a = 25 °C)

V_{DSS}	Drain to Source Voltage	60	V
V_{GSS}	Gate to Source Voltage	±20	V
$I_{D(DC)}$	Drain Current (DC)*	±27	A
$I_{D(pulse)}$	Drain Current (pulse)**	±108	A

*T_c = 25 °C
**PW ≤ 100 μs, Duty Cycle ≤ 2 %

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
$R_{DS(on)}$	Drain to Source On-State Resistance		0.06	0.085	Ω	V_{GS} = 10 V, I_D = 15 A
$R_{DS(on)}$	Drain to Source On-State Resistance		0.12	0.18	Ω	V_{GS} = 4 V, I_D = 15 A
V_{SD}	Body Diode Forward Voltage Drop		1.3		V	I_{SD} = 27 A, V_{GS} = 0
I_{DL}	Unclamped Sustaining Energy			27	A	V_{DD} = 30 V, $V_{GS(off)}$ = 0 L ≤ 100 μH, R_G ≥ 100 Ω Unclamped, See Test Circuit 1
$V_{GS(off)}$	Gate to Source Cutoff Voltage	1.0		2.5	V	V_{DS} = 10 V, I_D = 1 mA
$\|Y_{fs}\|$	Forward Transfer Admittance	8.0	12		S	V_{DS} = 10 V, I_D = 15 A
I_{DSS}	Drain Leakage Current			10	μA	V_{DS} = 60 V, V_{GS} = 0
I_{GSS}	Gate to Source Leakage Current			±100	nA	V_{GS} = ±20 V, V_{DS} = 0
C_{iss}	Input Capacitance		1200		pF	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz
C_{oss}	Output Capacitance		520		pF	
C_{rss}	Reverse Transfer Capacitance		130		pF	
$t_{d(on)}$	Turn-On Delay Time		10		ns	I_D = 15 A, V_{DD} ≒ 30 A $V_{GS(on)}$ = 10 V R_L = 2 Ω R_{in} = 10 Ω See Test Circuit 2
t_r	Rise Time		10		ns	
$t_{d(off)}$	Turn-Off Delay Time		70		ns	
t_f	Fall Time		100		ns	
Q_G	Total Gate Charge		28		nC	V_{GS} = 10 V, I_D = 34 A V_{DD} = 40 V See Test Circuit 3
Q_{GS}	Gate to Source Charge		22		nC	
Q_{GD}	Gate to Drain Charge		6		nC	