HITACHI

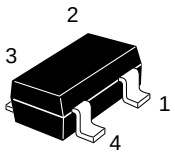
3SK228

GaAs Dual Gate MES FET
UHF TV Tuner RF Amplifier

Table 1 Absolute Maximum Ratings
(Ta = 25°C)

Item	Symbol	Rating	Unit
Drain to source voltage	V_{DS}	12	V
Gate 1 to source voltage	V_{G1S}	–6	V
Gate 2 to source voltage	V_{G2S}	–6	V
Drain current	I_D	50	mA
Channel power dissipation	Pch	150	mW
Channel temperature	Tch	125	°C
Storage temperature	Tstg	–55 to +125	°C

MPAK-4



1. Source
2. Gate 1
3. Gate 2
4. Drain

Table 2 Electrical Characteristics (Ta = 25°C)

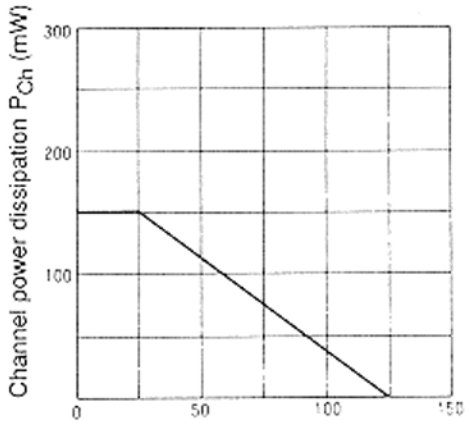
Item	Symbol	Min	Typ	Max	Unit	Test condition
Drain to source cutoff current	I_{DSX}	—	—	50	µA	V_{DS} = 12 V, V_{G1S} = –3 V, V_{G2S} = 0
Gate 1 to source breakdown voltage	$V_{(BR)G1SS}$	–6	—	—	V	I_{G1} = –10 µA, V_{G2S} = V_{DS} = 0
Gate 2 to source breakdown voltage	$V_{(BR)G2SS}$	–6	—	—	V	I_{G2} = –10 µA, V_{G1S} = V_{DS} = 0
Gate 1 cutoff current	I_{G1SS}	—	—	–5	µA	V_{G1S} = –5 V, V_{G2S} = V_{DS} = 0
Gate 2 cutoff current	I_{G2SS}	—	—	–5	µA	V_{G2S} = –5 V, V_{G15} = V_{DS} = 0
Drain current	I_{DSS}	10	17	32	mA	V_{DS} = 5 V, V_{G1S} = V_{G2S} = 0
Gate 1 to source cutoff voltage	$V_{G1S(off)}$	—	–1.1	–1.5	V	V_{DS} = 5 V, V_{G2S} = 0, I_D = 100 µA
Gate 2 to source cutoff voltage	$V_{G2S(off)}$	—	–1.1	–1.5	V	V_{DS} = 5 V, V_{G1S} = 0, I_D = 100 µA

Table 2 Electrical Characteristics (Ta = 25°C) (cont)

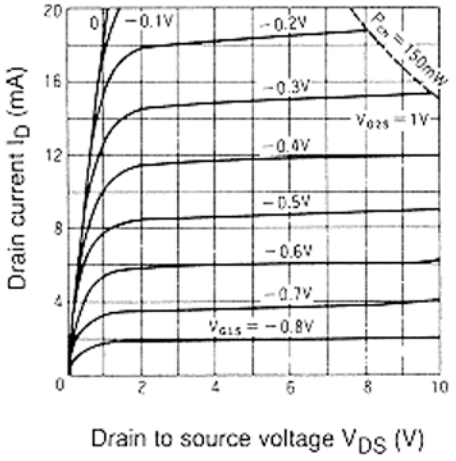
Item	Symbol	Min	Typ	Max	Unit	Test condition
Forward transfer admittance	$\|y_{fs}\|$	20	34	—	mS	V_{DS} = 5 V, V_{G2S} = 1V, I_D = 10 mA, f = 1kHz
Input capacitance	Ciss	—	0.58	1.0	pF	V_{DS} = 5 V, V_{G1S} = V_{G2S} = −3 V, f = 1MHz
Output capacitance	Coss	—	0.36	0.6	pF	
Reverse transfer capacitance	Crss	—	0.028	0.05	pF	
Power gain	PG	17	19.6	—	dB	V_{DS} = 5 V, V_{G2S} = 1 V I_D = 10 mA, f = 900 MHz
Noise figure	NF	—	1.3	2.0	dB	

• Marking is "XR-".

Maximum channel power dissipation curve



Typical output characteristics



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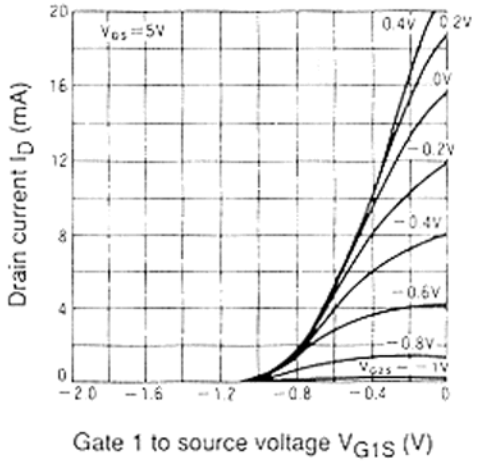
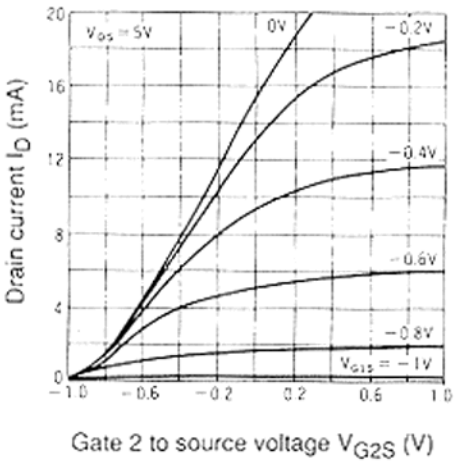
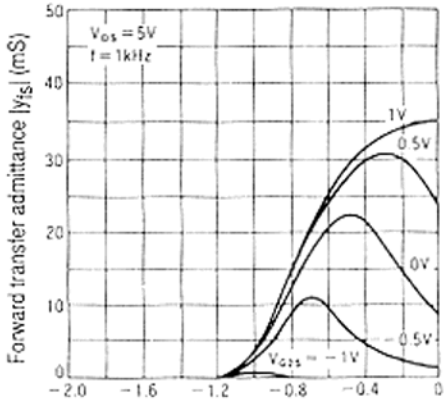
Drain current vs. gate 1 to source voltage



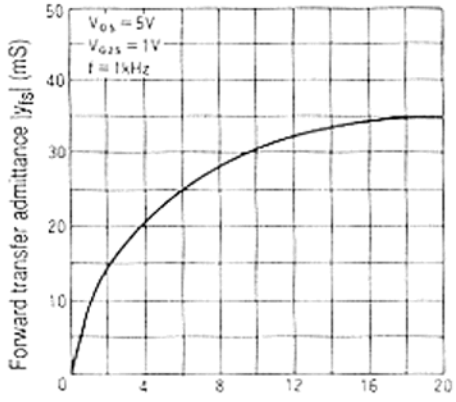
Drain current vs. gate 2 to source voltage



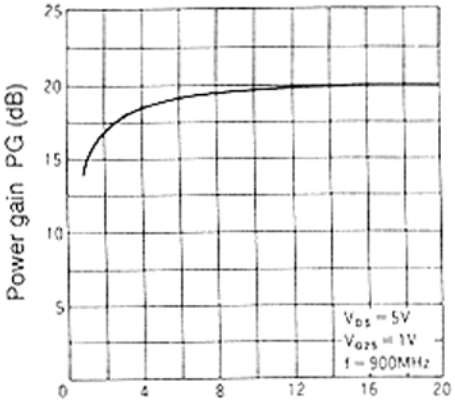
Forward transfer admittance vs. gate 1 to source voltage



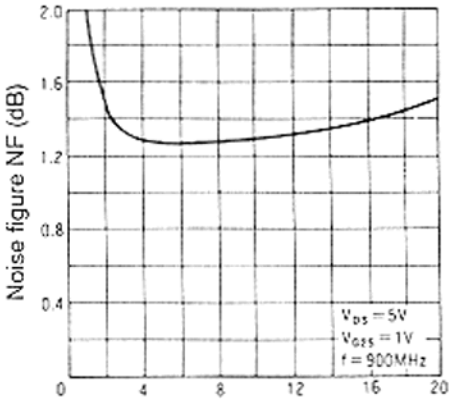
Forward transfer admittance vs. drain current



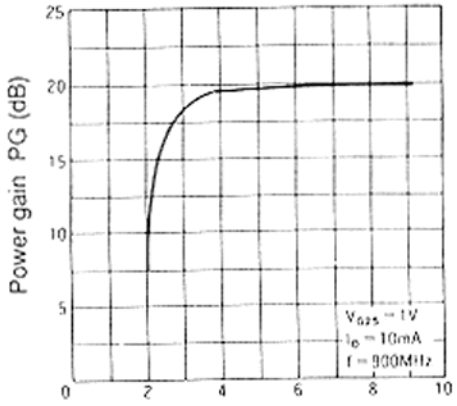
Power gain vs. drain current



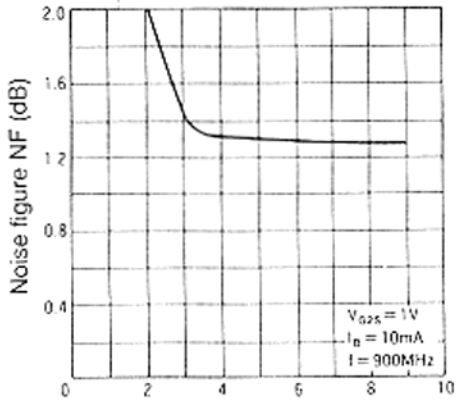
Noise figure vs. drain current



Power gain vs. drain to source voltage



Noise figure vs. drain to source voltage



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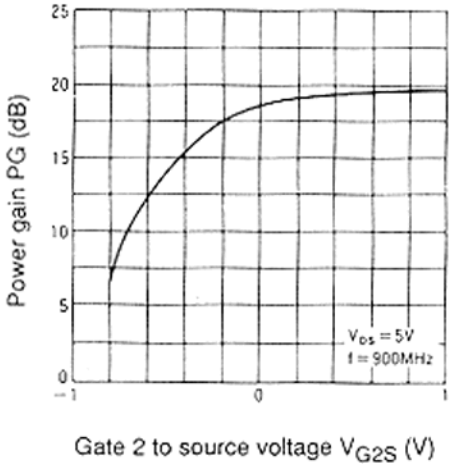
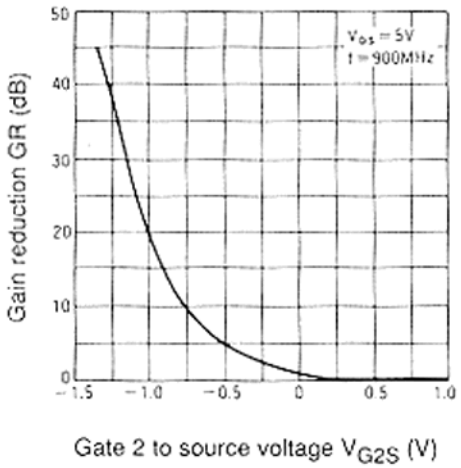
Power gain vs. gate 2 to source voltage



Gain reduction vs.
gate 2 to source voltage



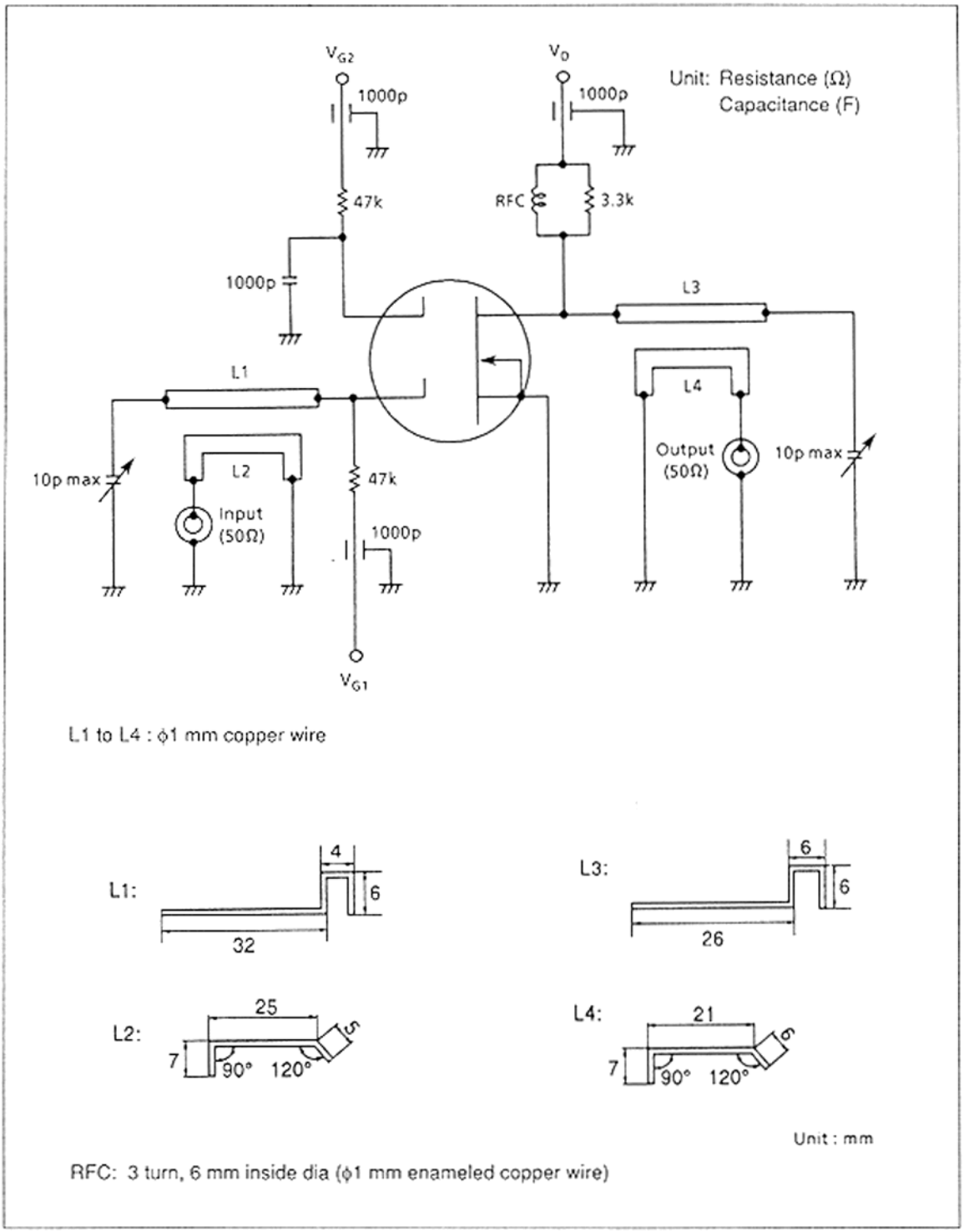


Figure 1 Power Gain, Noise Figure Test Circuit