HITACHI

4AM14

Silicon N Channel/P Channel Complementary Power MOS FET Array

Application

High speed power switching

Features

- Low on-resistance
  N-channel: R_{DS} (on) ≤ 0.17 Ω, V_{GS} = 10 V
  I_D = 4 A
  P-channel: R_{DS} (on) ≤ 0.2 Ω, V_{GS} = –10 V
  I_D = –4 A
- Capable of 4 V gate drive
- Low drive current
- Hight speed switching
- High density mounting
- Suitable for H-bridged motor driver
- Discrete packaged devices of same die
  N-channel: 2SK970 (TO-220AB),
  2SK1093 (TO-220FM)
  P-channel: 2SJ172 (TO-220AB),
  2SJ175 (TO-220FM)

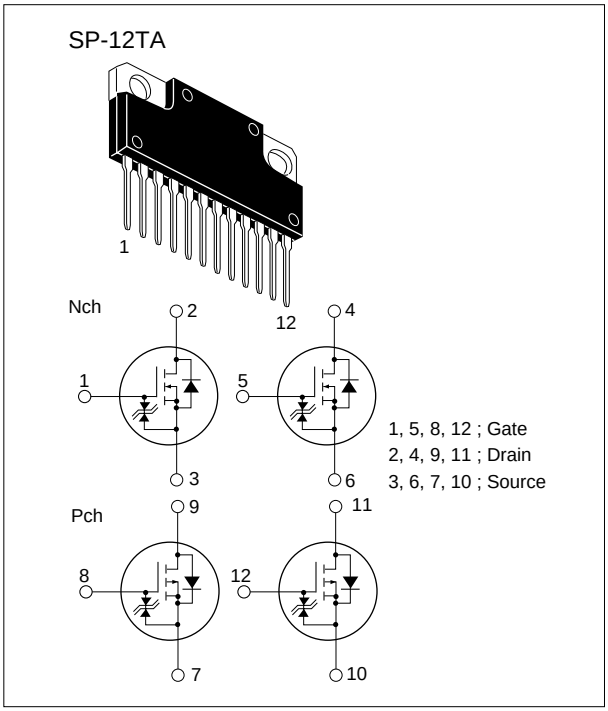


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings Nch	Ratings Pch	Unit
Drain to source voltage	V_{DSS}	60	–60	V
Gate to source voltage	V_{GSS}	±20	±20	V
Drain current	I_D	8	–8	A
Drain peak current	$I_{D(pulse)}$*	32	–32	A
Body–drain diode reverse drain current	I_{DR}	8	–8	A
Channel dissipation	Pch (Tc =25°C)**	32		W
Channel dissipation	Pch**	4		W
Channel temperature	Tch	150		°C
Storage temperature	Tstg	–55 to +150		°C

* PW ≤ 10 µs, duty cycle ≤ 1 %
** 4 devices operation

Table 2 Electrical Characteristics (Ta = 25°C) (1 Unit)

		N channel			P channel				
Item	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	–60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	—	—	–250	µA	V_{DS} = 50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	–1.0	—	–2.0	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.13	0.17	—	0.15	0.2	Ω	I_D = 4 A, V_{GS} = 10 V *
		—	0.18	0.24		0.20	0.27	Ω	I_D = 4 A, V_{GS} = 4 V *
Forward transfer admittance	|yfs|	3.5	5.5	—	3.5	6.0	—	S	I_D = 4 A *V_{DS} = 10 V *
Input capacitance	Ciss	—	400	—	—	900	—	pF	V_{DS} = 10 V, V_{GS} = 0, f = 1 MHz
Output capacitance	Coss	—	220	—	—	460	—	pF	
Reverse transfer capacitance	Crss	—	60	—	—	130	—	pF	
Turn–on delay time	$td_{(on)}$	—	5	—	—	8	—	ns	I_D = 4 A, V_{GS} = 10 V, R_L = 7.5 Ω
Rise time	tr	—	45	—	—	50	—	ns	
Turn–off delay time	$td_{(off)}$	—	150	—	—	180	—	ns	
Fall time	tf	—	85	—	—	95	—	ns	
Body–drain diode forward voltage	V_{DF}	—	1.2	—	—	–1.2	—	V	I_F = 8 A, V_{GS} = 0
Body–drain diode reverse recovery time	trr	—	120	—	—	185	—	ns	I_F = 8 A, V_{GS} = 0, dI_F/dt = 50 A/µs

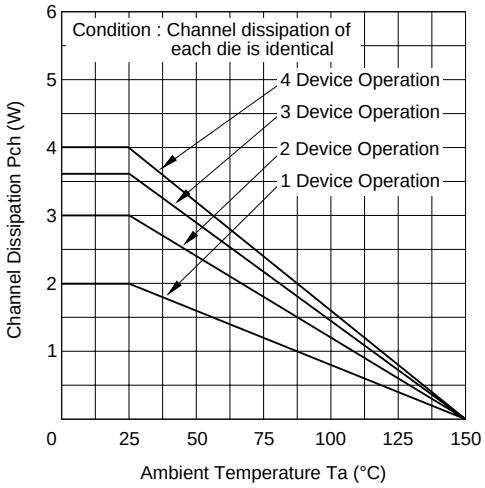
* Pulse Test

Note: Polarity of test conditions for P channel device is reversed.

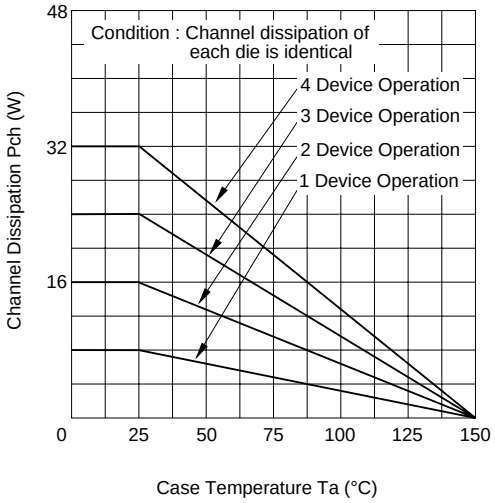
■ Nch : See characteristeic curves of 2SK970

■ Pch : See characteristeic curves of 2SJ172

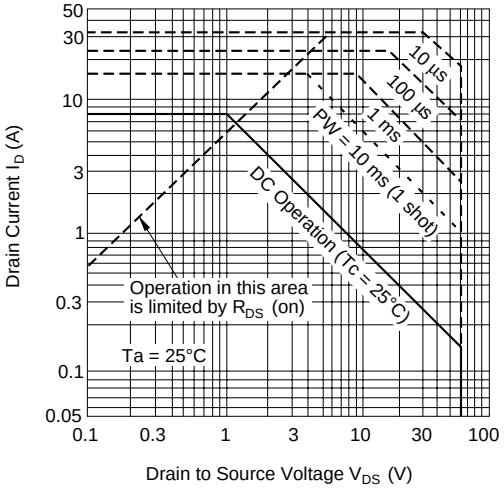
Maximum Channel Dissipation Curve



Maximum Channel Dissipation Curve



Maximum Safe Operation Area (N-channel)



Maximum Safe Operation Area (P-channel)