

74ACT825 8-Bit D-Type Flip-Flop

General Description

The ACT825 is an 8-bit buffered register. They have Clock Enable and Clear features which are ideal for parity bus interfacing in high performance microprogramming systems. Also included are multiple enables that allow multi-use control of the interface. The ACT825 has noninverting outputs and is fully compatible with AMD's Am29825.

Features

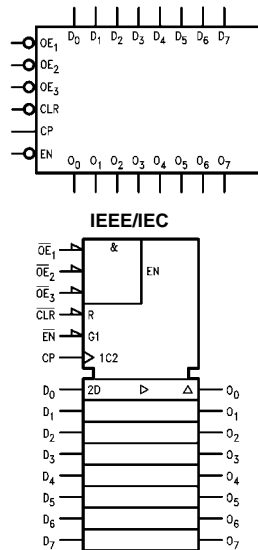
- Outputs source/sink 24 mA
- Inputs and outputs are on opposite sides
- ACT825 has TTL-compatible inputs

Ordering Code:

Order Number	Package Number	Package Description
74ACT825SC	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body
74ACT825MTC	MTC24	24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ACT825SPC	N24C	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-100, 0.300" Wide

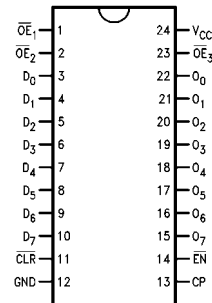
Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Logic Symbols



Connection Diagram

Pin Assignment
for DIP, SOIC and TSSOP



Pin Descriptions

Pin Names	Description
D ₀ -D ₇	Data Inputs
O ₀ -O ₇	Data Outputs
$\overline{OE}_1, \overline{OE}_2, \overline{OE}_3$	Output Enables
\overline{EN}	Clock Enable
\overline{CLR}	Clear
CP	Clock Input

FACT™ is a trademark of Fairchild Semiconductor.

Functional Description

The ACT825 consists of eight D-type edge-triggered flip-flops. These devices have 3-STATE outputs for bus systems, organized in a broadside pinning. In addition to the clock and output enable pins, the buffered clock (CP) and buffered Output Enable (\overline{OE}) are common to all flip-flops. The flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH CP transition. With \overline{OE}_1 , \overline{OE}_2 and \overline{OE}_3 LOW, the contents of the flip-flops are available at the outputs. When one of \overline{OE}_1 , \overline{OE}_2 or \overline{OE}_3 is HIGH, the outputs go to the high impedance state.

Operation of the \overline{OE} input does not affect the state of the flip-flops. The ACT825 has Clear (\overline{CLR}) and Clock Enable (\overline{EN}) pins. These pins are ideal for parity bus interfacing in high performance systems.

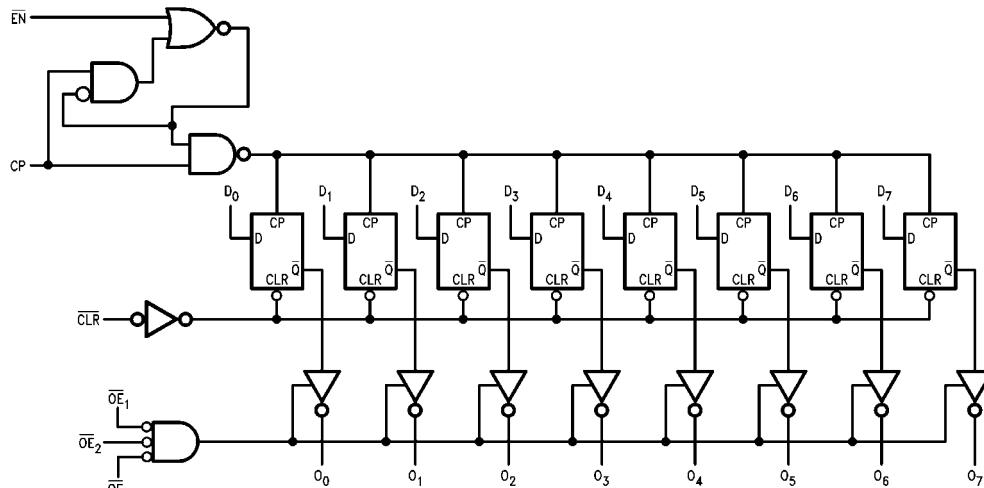
When \overline{CLR} is LOW and \overline{OE} is LOW, the outputs are LOW. When \overline{CLR} is HIGH, data can be entered into the flip-flops. When \overline{EN} is LOW, data on the inputs is transferred to the outputs on the LOW-to-HIGH clock transition. When \overline{EN} is HIGH, the outputs do not change state, regardless of the data or clock input transitions.

Function Table

Inputs					Internal	Output	Function
\overline{OE}	\overline{CLR}	\overline{EN}	CP	D_n	Q	O	
H	X	L	↗	L	L	Z	High-Z
H	X	L	↗	H	H	Z	High-Z
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	Clear
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	Hold
H	H	L	↗	L	L	Z	Load
H	H	L	↗	H	H	Z	Load
L	H	L	↗	L	L	L	Load
L	H	L	↗	H	H	H	Load

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = High Impedance
 ↗ = LOW-to-HIGH Transition
 NC = No Change

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)		Junction Temperature (T_J)	
Supply Voltage (V_{CC})	-0.5V to 7.0V	PDIP	140°C
DC Input Diode Current (I_{IK})		Recommended Operating Conditions	
$V_I = -0.5V$	-20 mA	Supply Voltage (V_{CC})	4.5V to 5.5V
$V_I = V_{CC} + 0.5V$	+20 mA	Input Voltage (V_I)	0V to V_{CC}
DC Input Voltage (V_I)	-0.5V to $V_{CC} + 0.5V$	Output Voltage (V_O)	0V to V_{CC}
DC Output Diode Current (I_{OK})		Operating Temperature (T_A)	-40°C to +85°C
$V_O = -0.5V$	-20 mA	Minimum Input Edge Rate ($\Delta V/\Delta t$)	125 mV/ns
$V_O = V_{CC} + 0.5V$	+20 mA	V_{IN} from 0.8V to 2.0V	
DC Output Voltage (V_O)	+0.5V	V_{CC} @ 4.5V, 5.5V	
DC Output Source or Sink Current (I_O)	± 50 mA	Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.	
DC V_{CC} or Ground Current			
Per Output Pin (I_{CC} or I_{GND})	± 50 mA		
Storage Temperature (T_{STG})	-65°C to +150°C		

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = 25^\circ\text{C}$		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level	4.5	1.5	2.0	2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
	Input Voltage	5.5	1.5	2.0	2.0		
V_{IL}	Maximum Low Level	4.5	1.5	0.8	0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
	Input Voltage	5.5	1.5	0.8	0.8		
V_{OH}	Minimum High Level	4.5	4.49	4.4	4.4	V	$I_{OUT} = -50 \mu\text{A}$
		5.5	5.49	5.4	5.4		
	Output Voltage	4.5		3.86	3.76	V	$V_{IN} = V_{IL}$ or V_{IH} $I_{OH} = -24 \text{ mA}$ $I_{OH} = -24 \text{ mA (Note 2)}$
		5.5		4.86	4.76		
V_{OL}	Maximum Low Level	4.5	0.001	0.1	0.1	V	$I_{OUT} = 50 \mu\text{A}$
		5.5	0.001	0.1	0.1		
	Output Voltage	4.5		0.36	0.44	V	$V_{IN} = V_{IL}$ or V_{IH} $I_{OL} = 24 \text{ mA}$ $I_{OL} = 24 \text{ mA (Note 2)}$
5.5		0.36	0.44				
I_{IN}	Maximum Input Leakage Current	5.5		± 0.1	± 1.0	μA	$V_I = V_{CC}, \text{ GND}$
I_{OZ}	Maximum 3-STATE Current	5.5		± 0.5	± 5.0	μA	$V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}, \text{ GND}$
I_{CCT}	Maximum I_{CC} /Input	5.5	0.6		1.5	mA	$V_I = V_{CC} - 2.1V$
I_{OLD}	Minimum Dynamic	5.5			75	mA	$V_{OLD} = 1.65V \text{ Max}$
I_{OHD}	Output Current (Note 3)	5.5			-75	mA	$V_{OHD} = 3.85V \text{ Min}$
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	$V_{IN} = V_{CC}$ or GND

Note 2: All outputs loaded; thresholds on input associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics								
Symbol	Parameter	V _{CC} (V) (Note 4)	T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF		Units
			Min	Typ	Max	Min	Max	
f _{max}	Maximum Clock Frequency	5.0	120	158		109		MHz
t _{PLH}	Propagation Delay CP to O _n	5.0	1.5	5.5	9.5	1.5	10.5	ns
t _{PHL}	Propagation Delay CP to O _n	5.0	2.0	5.5	9.5	1.5	10.5	ns
t _{PHL}	Propagation Delay CLR to O _n	5.0	2.5	8.0	13.5	2.0	15.5	ns
t _{PZH}	Output Enable Time OE to O _n	5.0	1.5	6.0	10.5	1.5	11.5	ns
t _{PZL}	Output Enable Time OE to O _n	5.0	2.0	6.5	11.0	1.5	12.0	ns
t _{PHZ}	Output Disable Time OE to O _n	5.0	1.5	6.5	11.0	1.5	12.0	ns
t _{PLZ}	Output Disable Time OE to O _n	5.0	1.5	6.0	10.5	1.5	11.5	ns

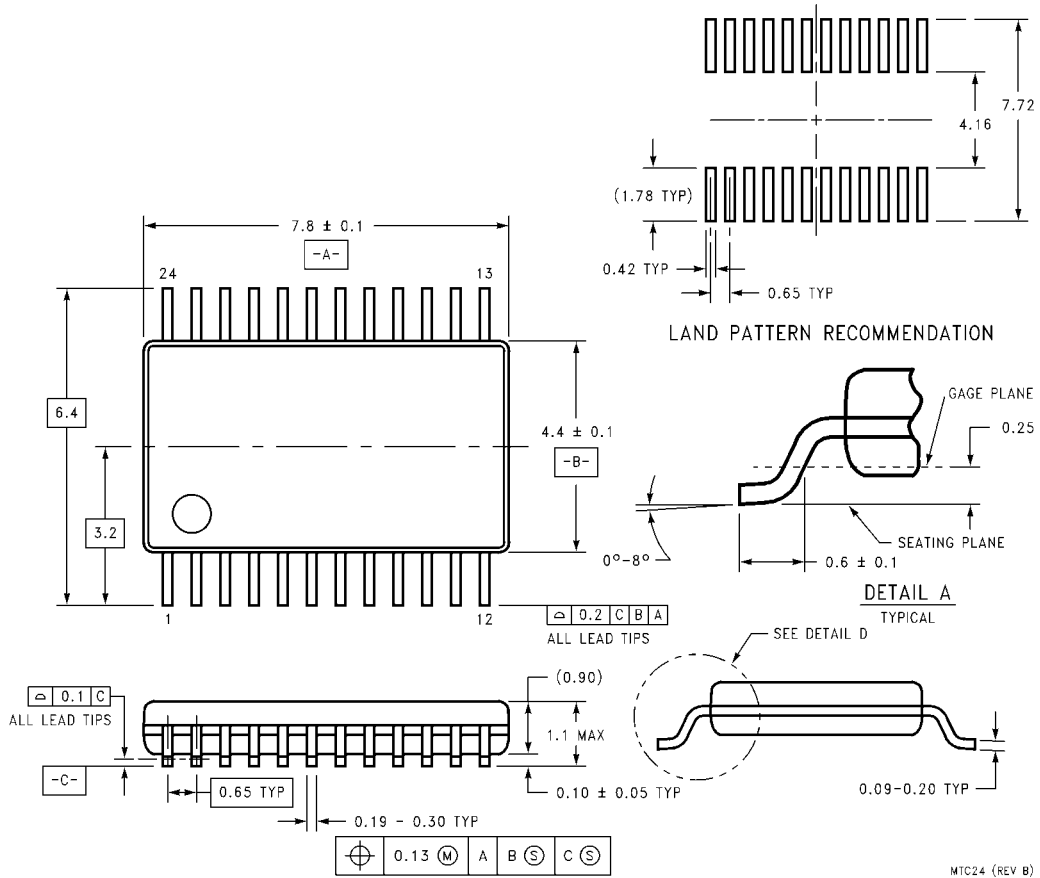
Note 4: Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements							
Symbol	Parameter	V _{CC} (V) (Note 5)	T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF		Units
			Typ	Guaranteed Minimum	Guaranteed Minimum	Guaranteed Minimum	
t _S	Setup Time, HIGH or LOW D _n to CP	5.0	0.5	2.5	2.5	2.5	ns
t _H	Hold Time, HIGH or LOW D _n to CP	5.0	0	2.5	2.5	2.5	ns
t _S	Setup Time, HIGH or LOW EN to CP	5.0	0	2.0	2.5	2.5	ns
t _H	Hold Time, HIGH or LOW EN to CP	5.0	0	1.0	1.0	1.0	ns
t _W	CP Pulse Width HIGH or LOW	5.0	2.5	4.5	5.5	5.5	ns
t _W	CLR Pulse Width, LOW	5.0	3.0	5.5	5.5	5.5	ns
t _{rec}	CLR to CP Recovery Time	5.0	1.5	3.5	4.0	4.0	ns

Note 5: Voltage Range 5.0 is 5.0V ±0.5V

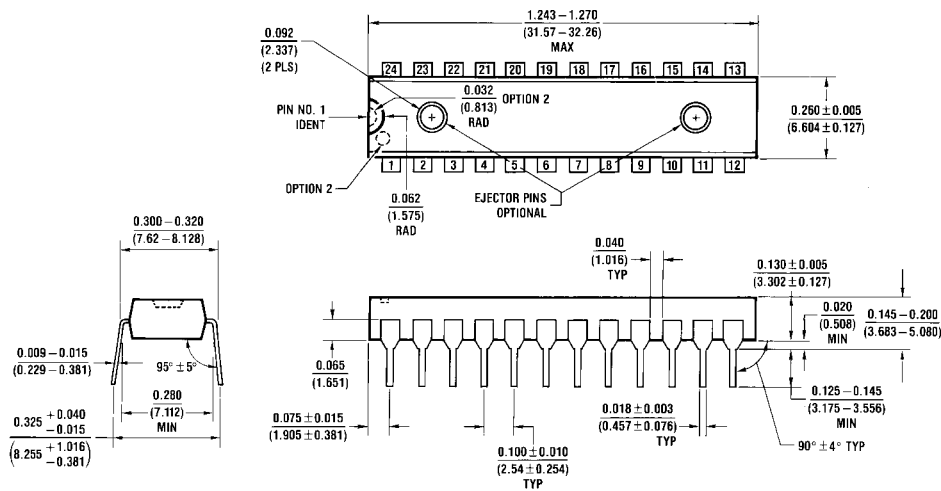
Capacitance				
Symbol	Parameter	Typ	Units	Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = OPEN
C _{PD}	Power Dissipation Capacitance	44	pF	V _{CC} = 5.0V

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC24**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-100, 0.300" Wide Package Number N24C

N24C (REV F)

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.