

74ACTQ273 Quiet Series Octal D-Type Flip-Flop

General Description

The ACTQ273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset (\overline{MR}) input load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D-type input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the \overline{MR} input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

The ACTQ utilizes Fairchild Quiet Series™ technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series™ features

GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

Features

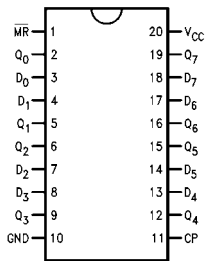
- I_{CC} reduced by 50%
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Improved latch-up immunity
- Buffered common clock and asynchronous master reset
- Outputs source/sink 24 mA
- 4 kV minimum ESD immunity

Ordering Code:

| Order Number | Package Number | Package Description |
|--------------|----------------|---|
| 74ACTQ273SC | M20B | 20-Lead Small Outline Integrated Circuit, JEDEC MS-013, 0.300" Wide Body |
| 74ACTQ273SJ | M20D | 20-Lead Small Outline Package, EIAJ TYPE II, 5.3mm Wide |
| 74ACTQ273MTC | MTC20 | 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |
| 74ACTQ273PC | N20A | 20-Lead Plastic Dual-In-Line Package, JEDEC MS-001, 0.300" Wide |

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Connection Diagram

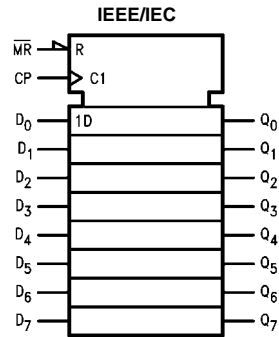
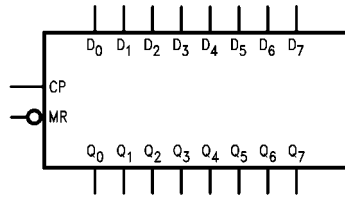


Pin Descriptions

| Pin Names | Description |
|-----------------|-------------------|
| D_0 – D_7 | Data Inputs |
| \overline{MR} | Master Reset |
| CP | Clock Pulse Input |
| Q_0 – Q_7 | Data Outputs |

FACT™, FACT Quiet Series™, and GTO™ are trademarks of Fairchild Semiconductor Corporation.

Logic Symbols

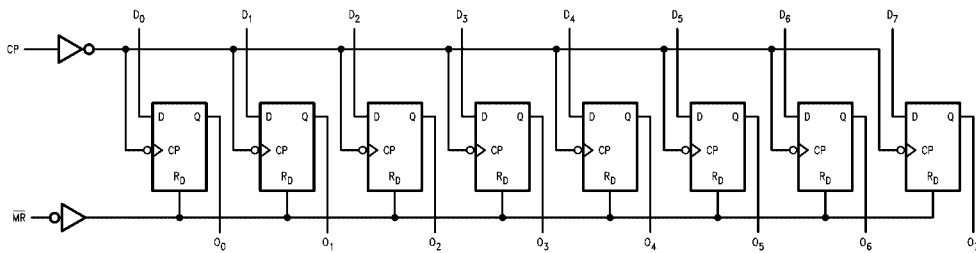


Mode Select-Function Table

| Operating Mode | Inputs | | | Outputs |
|----------------|-----------------|----|-------|---------|
| | \overline{MR} | CP | D_n | Q_n |
| Reset (Clear) | L | X | X | L |
| Load "1" | H | ↗ | H | H |
| Load "0" | H | ↗ | L | L |

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 ↗ = LOW-to-HIGH Transition

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 1)

| | |
|---|--------------------------|
| Supply Voltage (V_{CC}) | -0.5V to +7.0V |
| DC Input Diode Current (I_{IK}) | |
| $V_I = -0.5V$ | -20 mA |
| $V_I = V_{CC} + 0.5V$ | +20 mA |
| DC Input Voltage (V_I) | -0.5V to $V_{CC} + 0.5V$ |
| DC Output Diode Current (I_{OK}) | |
| $V_O = -0.5V$ | -20 mA |
| $V_O = V_{CC} + 0.5V$ | +20 mA |
| DC Output Voltage (V_O) | -0.5V to $V_{CC} + 0.5V$ |
| DC Output Source or Sink Current (I_O) | ± 50 mA |
| DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND}) | ± 50 mA |
| Storage Temperature (T_{STG}) | -65°C to +150°C |
| DC Latch-up Source or Sink Current | ± 300 mA |
| Junction Temperature (T_J) PDIP | 140°C |

Recommended Operating Conditions

| | |
|---|----------------|
| Supply Voltage (V_{CC}) | 4.5V to 5.5V |
| Input Voltage (V_I) | 0V to V_{CC} |
| Output Voltage (V_O) | 0V to V_{CC} |
| Operating Temperature (T_A) | -40°C to +85°C |
| Minimum Input Edge Rate $\Delta V/\Delta t$ | |
| V_{IN} from 0.8V to 2.0V | |
| V_{CC} @ 4.5V, 5.5V | 125 mV/ns |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

DC Electrical Characteristics

| Symbol | Parameter | V_{CC} (V) | $T_A = +25^\circ\text{C}$ | | $T_A = -40^\circ\text{C to } +85^\circ\text{C}$ | | Units | Conditions |
|-----------|--|-----------------|---------------------------|-------------------|---|---------|--|------------|
| | | | Typ | Guaranteed Limits | | | | |
| V_{IH} | Minimum HIGH Level Input Voltage | 4.5 | 1.5 | 2.0 | 2.0 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| | | 5.5 | 1.5 | 2.0 | 2.0 | | | |
| V_{IL} | Maximum LOW Level Input Voltage | 4.5 | 1.5 | 0.8 | 0.8 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| | | 5.5 | 1.5 | 0.8 | 0.8 | | | |
| V_{OH} | Minimum HIGH Level Output Voltage | 4.5 | 4.49 | 4.4 | 4.4 | V | $I_{OUT} = -50 \mu A$ | |
| | | 5.5 | 5.49 | 5.4 | 5.4 | | | |
| | | 4.5 | | 3.86 | 3.76 | V | $V_{IN} = V_{IL}$ or V_{IH} $I_{OH} = -24$ mA $I_{OH} = -24$ mA (Note 2) | |
| | | 5.5 | | 4.86 | 4.76 | | | |
| V_{OL} | Maximum LOW Level Output Voltage | 4.5 | 0.001 | 0.1 | 0.1 | V | $I_{OUT} = 50 \mu A$ | |
| | | 5.5 | 0.001 | 0.1 | 0.1 | | | |
| | | 4.5 | | 0.36 | 0.44 | V | $V_{IN} = V_{IL}$ or V_{IH} $I_{OL} = 24$ mA $I_{OL} = 24$ mA (Note 2) | |
| | | 5.5 | | 0.36 | 0.44 | | | |
| I_{IN} | Maximum Input Leakage Current | 5.5 | | ± 0.1 | ± 1.0 | μA | $V_I = V_{CC}, GND$ | |
| I_{CCT} | Maximum I_{CC} /Input | 5.5 | 0.6 | | 1.5 | mA | $V_I = V_{CC} - 2.1V$ | |
| I_{OLD} | Minimum Dynamic Output Current (Note 3) | 5.5 | | | 75 | mA | $V_{OLD} = 1.65V$ Max | |
| | | 5.5 | | | -75 | mA | $V_{OHD} = 3.85V$ Min | |
| I_{CC} | Maximum Quiescent Supply Current | 5.5 | | 4.0 | 40.0 | μA | $V_{IN} = V_{CC}$ or GND | |
| V_{OLP} | Quiet Output Maximum Dynamic V_{OL} | 5.0 | 1.1 | 1.5 | | V | Figure 1 Figure 2 (Note 4) | |
| | | | | | | | | |
| V_{OLV} | Quiet Output Minimum Dynamic V_{OL} | 5.0 | -0.6 | -1.2 | | V | Figure 1 Figure 2 (Note 4) | |
| | | | | | | | | |
| V_{IHD} | Minimum HIGH Level Dynamic Input Voltage | 5.0 | 1.9 | 2.2 | | V | (Note 5) | |
| V_{ILD} | Maximum LOW Level Dynamic Input Voltage | 5.0 | 1.2 | 0.8 | | V | (Note 5) | |

Note 2: All outputs loaded; thresholds on input associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

Note 4: Max number of outputs defined as (n). n - 1 Data inputs are driven 0V to 3V; one output @ GND.

Note 5: Max number of Data Inputs (n) switching. (n - 1) Inputs switching 0V to 3V (ACTQ). Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}) $f = 1$ MHz.

| AC Electrical Characteristics | | | | | | | | |
|--|---|------------------------------------|--|-----|-----|---|-----|-------|
| Symbol | Parameter | V _{CC} (V) (Note 6) | T _A = +25°C C _L = 50 pF | | | T _A = -40°C to +85°C C _L = 50 pF | | Units |
| | | | Min | Typ | Max | Min | Max | |
| f _{MAX} | Maximum Clock Frequency | 5.0 | 125 | 189 | | 110 | | MHz |
| t _{PLH} t _{PHL} | Propagation Delay CP to Q _n | 5.0 | 1.5 | 6.5 | 8.5 | 1.5 | 9.0 | ns |
| t _{PHL} | Propagation Delay MR to Q _n | 5.0 | 1.5 | 7.0 | 9.0 | 1.5 | 9.5 | ns |
| t _{OSHL} t _{OSLH} | Output to Output Skew (Note 7) | 5.0 | | 0.5 | 1.0 | | 1.0 | ns |

Note 6: Voltage Range 5.0 is 5.0V ± 0.5V

Note 7: Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs within the same packaged device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}). Parameter guaranteed by design. Not tested.

| AC Operating Requirements | | | | | | | |
|---------------------------|---|------------------------------------|--|--------------------|---|--|-------|
| Symbol | Parameter | V _{CC} (V) (Note 8) | T _A = +25°C C _L = 50 pF | | T _A = -40°C to +85°C C _L = 50 pF | | Units |
| | | | Typ | Guaranteed Minimum | | | |
| t _S | Setup Time, HIGH or LOW D _n to CP | 5.0 | 1.0 | 3.5 | 3.5 | | ns |
| t _H | Hold Time, HIGH or LOW D _n to CP | 5.0 | -0.5 | 1.5 | 1.5 | | ns |
| t _W | Clock Pulse Width HIGH or LOW | 5.0 | 2.0 | 4.0 | 4.0 | | ns |
| t _W | MR Pulse Width HIGH or LOW | 5.0 | 1.5 | 4.0 | 4.0 | | ns |
| t _W | Recovery Time MR to CP | 5.0 | 0.5 | 3.0 | 3.0 | | ns |

Note 8: Voltage Range 5.0 is 5.0V ± 0.5V

| Capacitance | | | | | |
|-----------------|-------------------------------|------|-------|------------------------|--|
| Symbol | Parameter | Typ | Units | Conditions | |
| C _{IN} | Input Capacitance | 4.5 | pF | V _{CC} = OPEN | |
| C _{PD} | Power Dissipation Capacitance | 40.0 | pF | V _{CC} = 5.0V | |

FACT Noise Characteristics

The setup of a noise characteristics measurement is critical to the accuracy and repeatability of the tests. The following is a brief description of the setup used to measure the noise characteristics of FACT.

Equipment:

Hewlett Packard Model 8180A Word Generator

PC-163A Test Fixture

Tektronics Model 7854 Oscilloscope

Procedure:

1. Verify Test Fixture Loading: Standard Load 50 pF, 500Ω.
2. Deskew the HFS generator so that no two channels have greater than 150 ps skew between them. This requires that the oscilloscope be deskewed first. It is important to deskew the HFS generator channels before testing. This will ensure that the outputs switch simultaneously.
3. Terminate all inputs and outputs to ensure proper loading of the outputs and that the input levels are at the correct voltage.
4. Set the HFS generator to toggle all but one output at a frequency of 1 MHz. Greater frequencies will increase DUT heating and effect the results of the measurement.
5. Set the HFS generator input levels at 0V LOW and 3V HIGH for ACT devices and 0V LOW and 5V HIGH for AC devices. Verify levels with an oscilloscope.

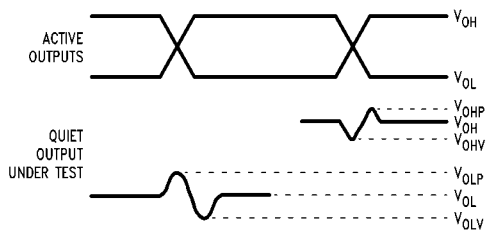


FIGURE 1. Quiet Output Noise Voltage Waveforms

Note 9: V_{OHV} and V_{OLP} are measured with respect to ground reference.

Note 10: Input pulses have the following characteristics: $f = 1$ MHz, $t_r = 3$ ns, $t_f = 3$ ns, skew < 150 ps.

V_{OLP}/V_{OLV} and V_{OHP}/V_{OHV} :

- Determine the quiet output pin that demonstrates the greatest noise levels. The worst case pin will usually be the furthest from the ground pin. Monitor the output voltages using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- Measure V_{OLP} and V_{OLV} on the quiet output during the worst case transition for active and enable. Measure V_{OHP} and V_{OHV} on the quiet output during the worst case active and enable transition.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

V_{ILD} and V_{IHD} :

- Monitor one of the switching outputs using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- First increase the input LOW voltage level, V_{IL} , until the output begins to oscillate or steps out a min of 2 ns. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input LOW voltage level at which oscillation occurs is defined as V_{ILD} .
- Next decrease the input HIGH voltage level, V_{IH} , until the output begins to oscillate or steps out a min of 2 ns. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input HIGH voltage level at which oscillation occurs is defined as V_{IHD} .
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

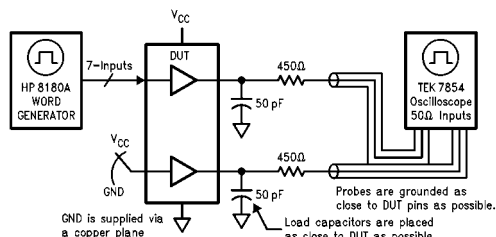
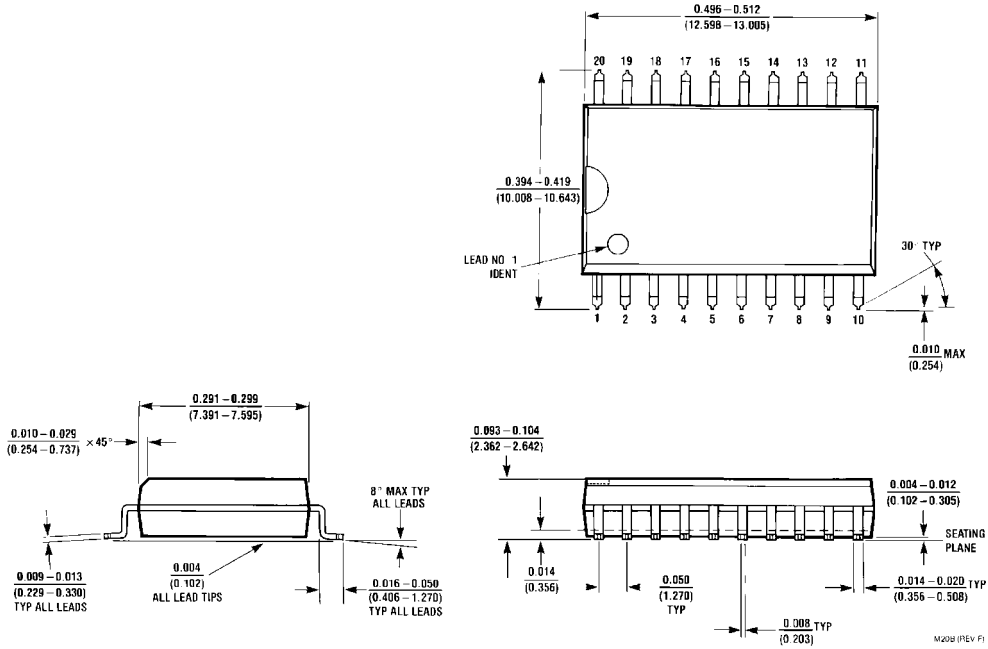


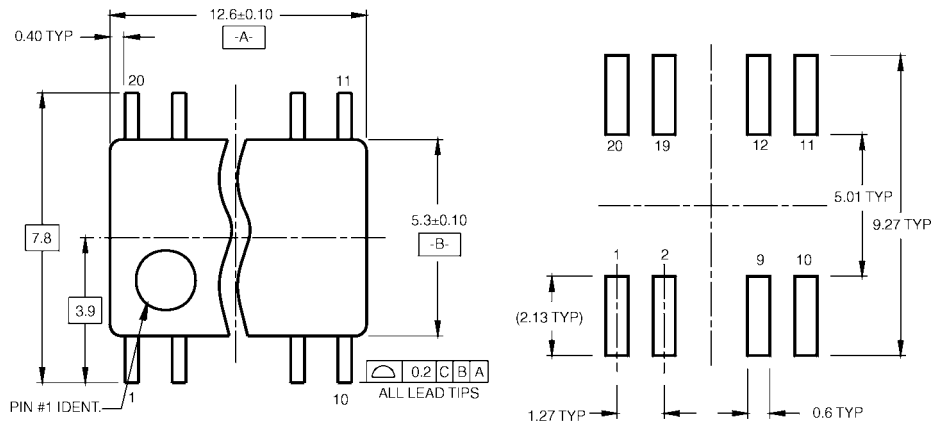
FIGURE 2. Simultaneous Switching Test Circuit

Physical Dimensions inches (millimeters) unless otherwise noted

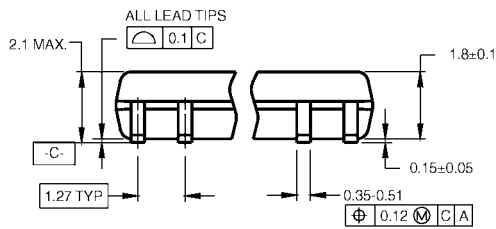


**20-Lead Small Outline Integrated Circuit, JEDEC MS-013, 0.300" Wide Body
Package Number M20B**

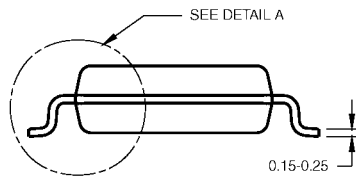
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS



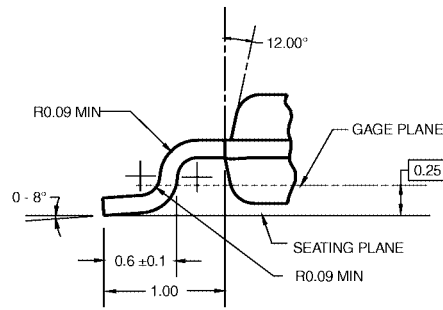
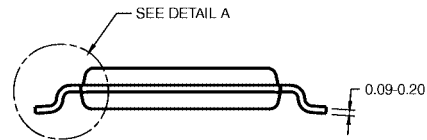
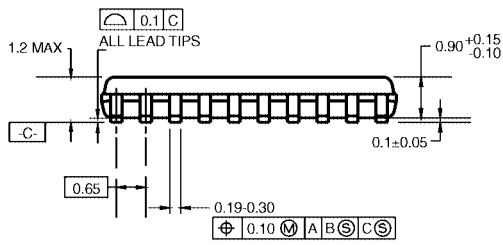
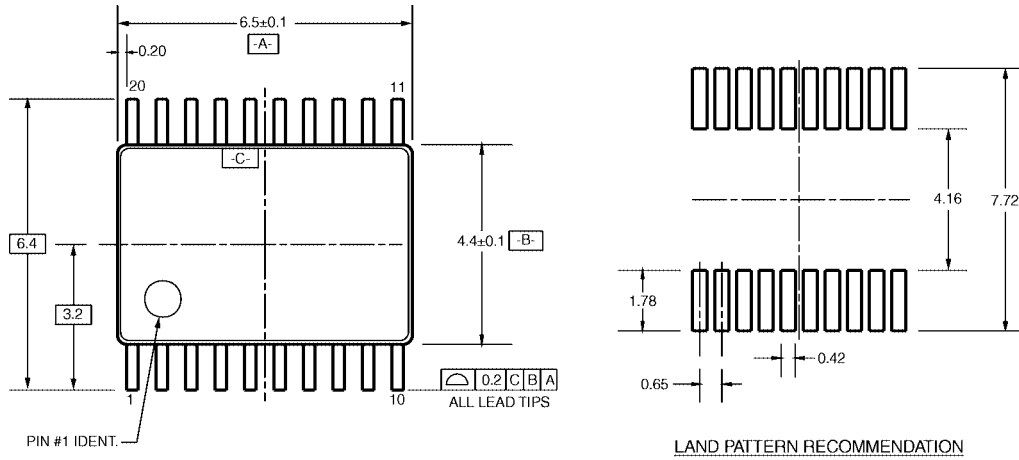
DETAIL A

- NOTES:
- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
 - B. DIMENSIONS ARE IN MILLIMETERS.
 - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DRevB1

**20-Lead Small Outline Package, EIAJ TYPE II, 5.3mm Wide
Package Number M20D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS

NOTES:

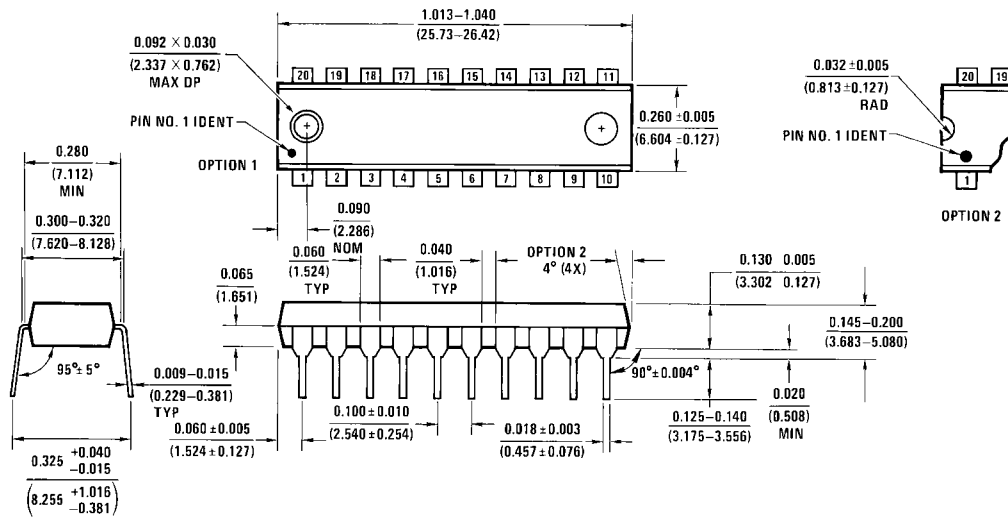
- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20RevD1

DETAIL A

**20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC20**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



N20A (REV G)

**20-Lead Plastic Dual-In-Line Package, JEDEC MS-001, 0.300" Wide
Package Number N20A**

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com