

## 74F1071

### 18-Bit Undershoot/Overshoot Clamp and ESD Protection Device

#### General Description

The 74F1071 is an 18-bit undershoot/overshoot clamp which is designed to limit bus voltages and also to protect more sensitive devices from electrical overstress due to electrostatic discharge (ESD). The inputs of the device aggressively clamp voltage excursions nominally at 0.5V below and 7V above ground.

#### Features

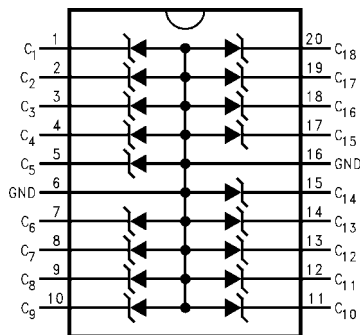
- 18-bit array structure in 20-pin package
- FAST® Bipolar voltage clamping action
- Dual center pin grounds for min inductance
- Robust design for ESD protection
- Low input capacitance
- Optimum voltage clamping for 5V CMOS/TTL applications

#### Ordering Code:

Order Number	Package Number	Package Description
74F1071SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74F1071MSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
74F1071MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

#### Connection Diagram



**Note:** Simplified Component Representation

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74F1071 18-Bit Undershoot/Overshoot Clamp

**Absolute Maximum Ratings** (Note 1)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-65°C to +125°C
Junction Temperature under Bias	-65°C to +150°C
Input Voltage (Note 2)	-0.5V to +6V
Input Current (Note 2)	-200 mA to +50 mA
ESD (Note 3)	
Human Body Model (MIL-STD-883D method 3015.7)	±10 kV
IEC 801-2	±6 kV
Machine Model (EIAJIC-121-1981)	±2 kV
DC Latchup Source Current (JEDEC Method 17)	±500 mA
Package Power Dissipation @+70°C	
SOIC Package	800 mW

**Recommended Operating Conditions**

Free Air Ambient Temperature	0°C to +70°C
Reverse Bias Voltage	0V to 5.25 V <sub>DC</sub>
Thermal Resistance ( $\theta_{JA}$ in Free Air)	
SOIC Package	100°C/W
SSOP Package	110°C/W

**Note 1:** Absolute maximum ratings are DC values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Voltage ratings may be exceeded if current ratings and junction temperature and power consumption ratings are not exceeded.

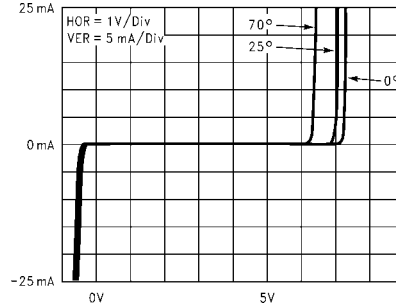
**Note 3:** ESD Rating for Direct contact discharge using ESD Simulation Tester. Higher rating may be realized in the actual application.

**DC Electrical Characteristics**

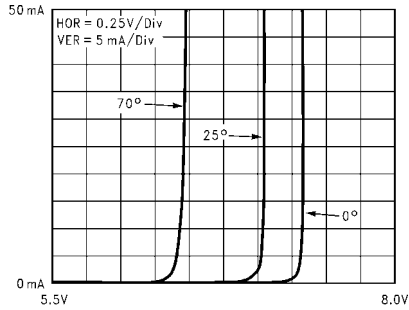
Symbol	Parameter	T <sub>A</sub> = +25°C			T <sub>A</sub> = 0°C to +70°C		Units	Conditions
		Min	Typ	Max	Min	Max		
I <sub>IH</sub>	Input HIGH Current		1.5	10		50	μA	V <sub>IN</sub> = 5.25V; Untested Input @ GND V <sub>IN</sub> = 5.5V; Untested Input @ GND
			3	20		100		
V <sub>Z</sub>	Reverse Voltage	6.6	6.9	7.2	5.9	7.7	V	I <sub>Z</sub> = 1 mA; Untested Inputs @ GND I <sub>Z</sub> = 50 mA; Untested Inputs @ GND
			7.1	7.5		8.0		
V <sub>F</sub>	Forward Voltage	-0.3	-0.6	-0.9	-0.3	-0.9	V	I <sub>F</sub> = -18 mA; Untested Inputs @ 5V I <sub>F</sub> = -200 mA; Untested Inputs @ 5V
		-0.5	-1.1	-1.5	-0.5	-1.5		
I <sub>CT</sub>	Adjacent Input Crosstalk			3			%	
C <sub>IN</sub>	Input Capacitance (small signal @ 1 MHz)		25				pF	V <sub>BIAS</sub> = 0 V <sub>DC</sub> V <sub>BIAS</sub> = 5 V <sub>DC</sub>
			13					

## DC Electrical Characteristics

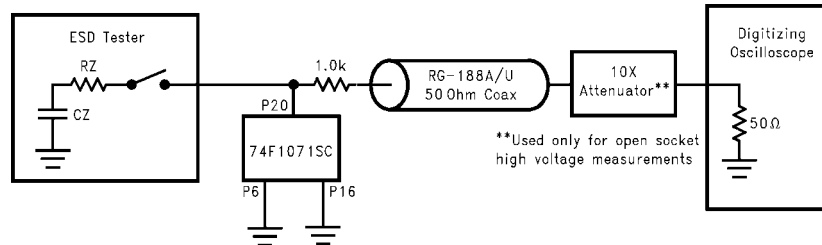
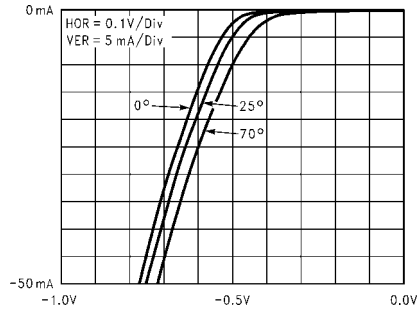
**Typical Forward and Reverse V/I Characteristics**



**Typical Reverse Conduction Characteristics**



**Typical Forward Conduction Characteristics**

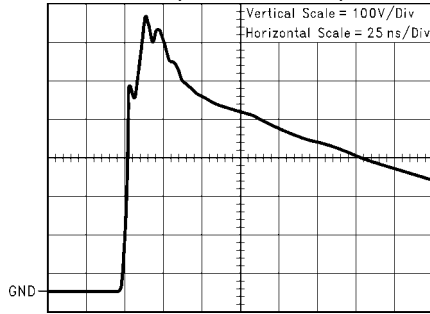


ESD Network	CZ	RZ
Human Body Model	100 pF	1500Ω
IEC 801-2	150 pF	330Ω

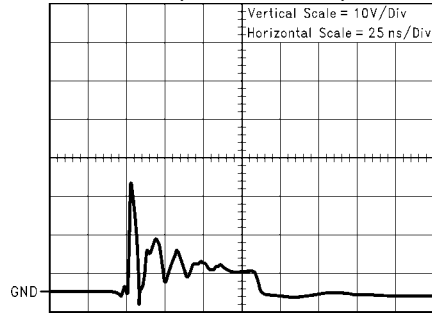
Simulated ESD Voltage Clamping Test Circuit

**DC Electrical Characteristics** (Continued)

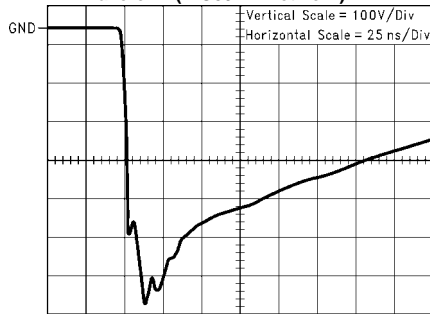
**Unclamped + 1 KV ESD Voltage Waveform (IEC801-2 Network)**



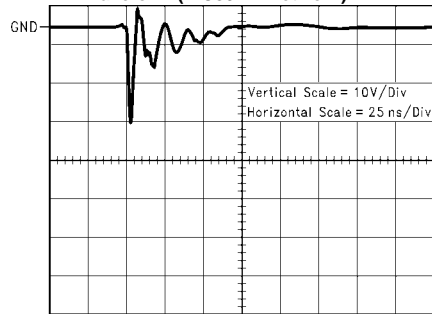
**Clamped + 1 KV ESD Voltage Waveform (IEC801-2 Network)**



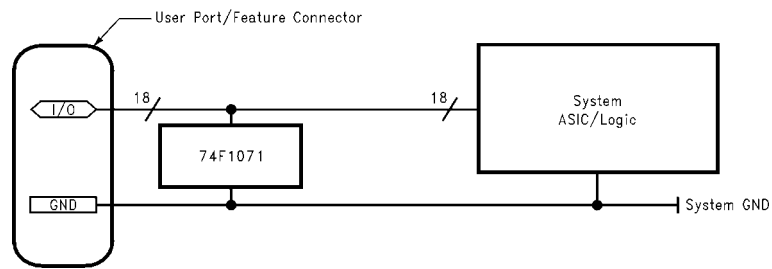
**Unclamped - 1 KV ESD Voltage Waveform (IEC801-2 Network)**



**Clamped - 1 KV ESD Voltage Waveform (IEC801-2 Network)**

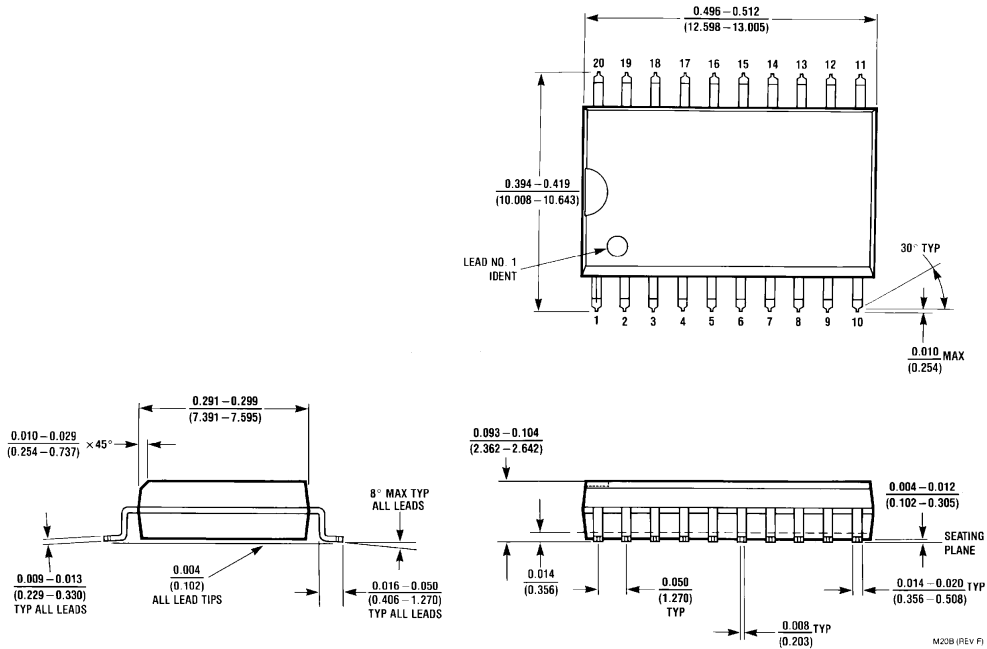


**Typical Application**

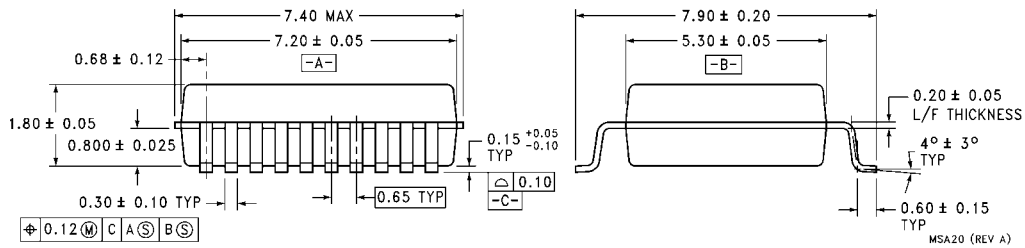
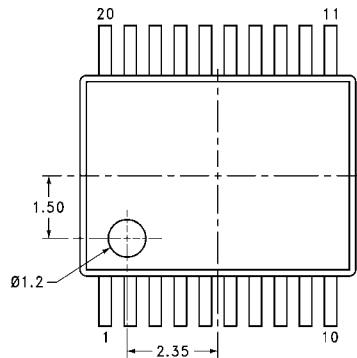


**74F1071 ESD Protection of ASIC on User Port**

**Physical Dimensions** inches (millimeters) unless otherwise noted

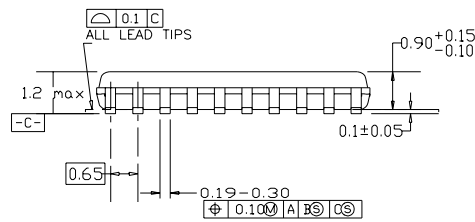
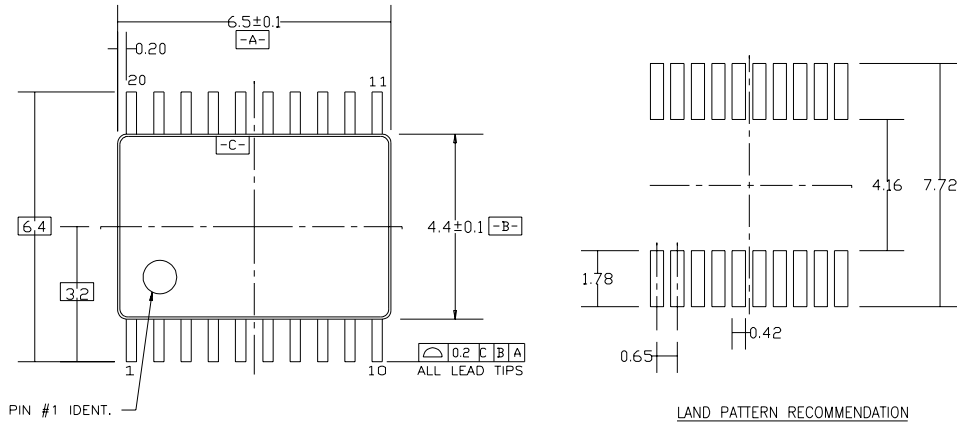


**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide  
Package Number M20B**

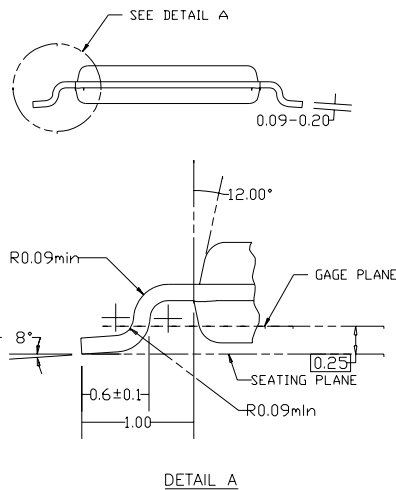


**20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide  
Package Number MSA20**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS



**NOTES:**

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

**20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide  
Package Number MTC20**

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