

## 74FR25900

### 9-Bit, 3-Port Latchable Datapath Multiplexer with 25Ω Output Series Resistors

#### General Description

The 74FR25900 is a data bus multiplexer routing any of three 9-bit ports to any other one of the three ports. Readback of data latched from any port onto itself is also possible. The 74FR25900 maintains separate control of all latch-enable, output enable and select inputs for maximum flexibility. PINV allows inversion of the data from the C<sub>8</sub> to A<sub>8</sub> or B<sub>8</sub> path. This is useful for control of the parity bit in systems diagnostics.

This device includes 25Ω resistors in series with A and B Port outputs. Resistors minimize undershoot and ringing which may damage or corrupt sensitive device inputs driven by these ports.

#### Features

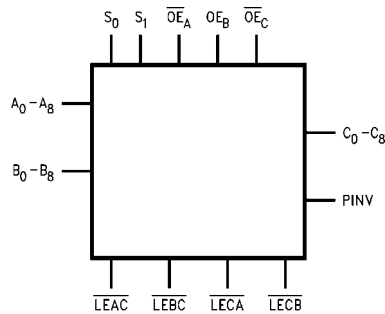
- 25Ω series resistors in the port A and B outputs eliminate the need for external resistors when driving MOS inputs such as DRAM arrays
- 9-bit data ports for systems carrying parity bits
- Readback capability for system self checks.
- Independent control lines for maximum flexibility
- Guaranteed multiple output switching and 250 pF load delays
- Outputs optimized for dynamic bus drive capability
- PINV parity control facilitates system diagnostics
- 74FR900 option available without output series resistors

#### Ordering Code:

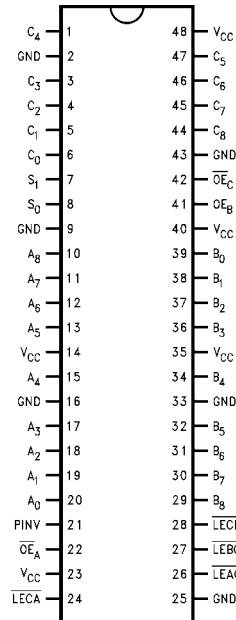
Order Number	Package Number	Package Description
74FR25900SSC	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

#### Logic Symbol



#### Connection Diagram



#### Pin Description

Pin Names	Description
$\overline{LE}_{xx}$	Latch Enable Inputs
$\overline{OE}_x$	Output Enable Inputs
PINV	Parity Invert Input
S <sub>0</sub> , S <sub>1</sub>	Select Inputs
A <sub>0</sub> -A <sub>8</sub>	Port A Inputs or 3-STATE Outputs
B <sub>0</sub> -B <sub>8</sub>	Port B Inputs or 3-STATE Outputs
C <sub>0</sub> -C <sub>8</sub>	Port C Inputs or 3-STATE Outputs

## Functional Description

The 74FR25900 allows 9-bit data to be transferred from any of three 9-bit I/O ports to either of the two remaining I/O ports. The device employs latches in all paths for either transparent or synchronous operation. Readback capability from any port to itself is also possible.

Data transfer within the 74FR25900 is controlled through use of the select ( $S_0$  and  $S_1$ ) and output-enable ( $\overline{OE}_A$ ,  $OE_B$  and  $\overline{OE}_C$ ) inputs as described in Table 1. Additional control is available by use of the latch-enable inputs ( $\overline{LEAC}$ ,  $\overline{LECA}$ ,  $\overline{LEBC}$ ,  $\overline{LECB}$ ) allowing either synchronous or transparent transfers (see Table 2). Table 1 indicates several readback conditions. By latching data on a given port and initiating the readback control configuration, previous data may be read for system verification or diagnostics. This mode may be useful in implementing system diagnostics.

Data at the port to be readback must be latched prior to enabling the outputs on that port. If this is not done, a closed data loop will result causing possible data integrity problems. Note that the A and B Ports allow readback without affecting any other port. C Port, however, requires interruption of either A or B Ports to complete its readback path.

PINV controls inversion of the  $C_8$  bit. A LOW on PINV allows  $C_8$  data to pass unaltered. A HIGH causes inversion of the data. See Table 3. This feature allows forcing of parity errors for use in system diagnostics. This is particularly helpful in 486 processor designs as the 486 does not provide odd/even parity selection internally.

**TABLE 1. Datapath Control**

		Inputs			Function
$S_0$	$S_1$	$\overline{OE}_A$	$OE_B$	$\overline{OE}_C$	
L	X	H	L	L	Port A to Port C
L	L	H	H	H	Port A to Port B
L	O	H	H	L	Port A to B+C
H	L	L	L	H	Port B to Port A
H	X	H	L	L	Port B to Port C
H	O	L	L	L	Port B to A+C
X	H	L	L	H	Port C to Port A
X	H	H	H	H	Port C to Port B
X	H	L	H	H	Port C to A+B
X	X	H	L	H	Outputs Disabled
L	L	L	X	X	(Readback to A) (Note 1)
L	H	L	X	L	(Readback to A or C) (Note 1)
H	L	X	H	X	(Readback to B) (Note 1)
H	H	X	H	L	(Readback to B or C) (Note 1)

**Note 1:** Readback operation in latched mode only. Transparent operation could result in unpredictable results.

**TABLE 2. Latch-Enable Control**

$\overline{LE}_{xx}$	Input	Output
L	L	L
L	H	H
H	X	$Q_0$

**TABLE 3. PINV Control**

PINV	$C_8$	$A_8$ or $B_8$
L	L	L
L	H	H
H	L	H
H	H	L

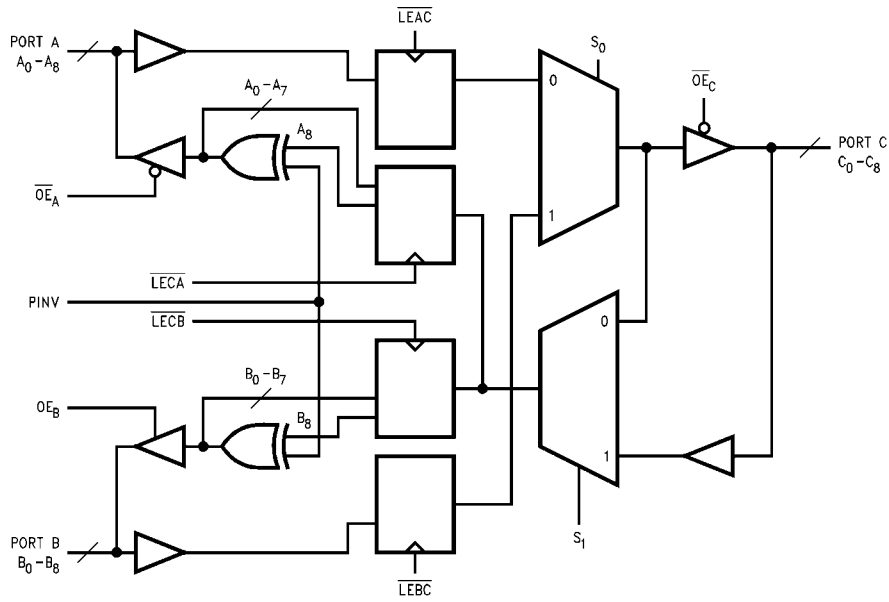
**Key:**

L = LOW Voltage

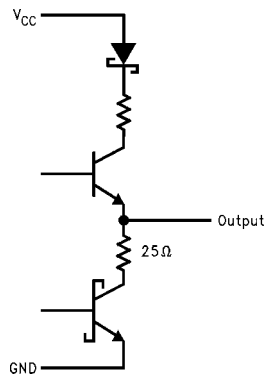
H = HIGH Voltage Level

$Q_0$  = Output state prior to  $\overline{LE}_{xx}$  LOW-to-HIGH transition

**Logic Diagram**



**Schematic of A and B Port Outputs**



**Absolute Maximum Ratings** (Note 2)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +150°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 3)	-0.5V to +7.0V
Input Current (Note 3)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	-0.5V to V <sub>CC</sub>
3-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
ESD Last Passing Voltage (Min)	2000V

**Recommended Operating Conditions**

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

**Note 2:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 3:** Either voltage limit or current limit is sufficient to protect inputs.

**DC Electrical Characteristics**

Symbol	Parameter	Min	Typ	Max	Units	V <sub>CC</sub>	Conditions
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	2.4			V	Min	I <sub>OH</sub> = -3 mA (A <sub>n</sub> , B <sub>n</sub> , C <sub>n</sub> )
		2.0			V	Min	I <sub>OH</sub> = -15 mA (A <sub>n</sub> , B <sub>n</sub> , C <sub>n</sub> )
V <sub>OL</sub>	Output LOW Voltage			0.50	V	Min	I <sub>OL</sub> = 1 mA (A <sub>n</sub> , B <sub>n</sub> )
				0.75	V	Min	I <sub>OL</sub> = 12 mA (A <sub>n</sub> , B <sub>n</sub> )
				0.50	V	Min	I <sub>OL</sub> = 24 mA (C <sub>n</sub> )
I <sub>IH</sub>	Input HIGH Current			5	μA	Max	V <sub>IN</sub> = 2.7V (Control Inputs)
I <sub>BVI</sub>	Input HIGH Current Breakdown Test			7	μA	Max	V <sub>IN</sub> = 7.0V (Control Inputs)
I <sub>BVIT</sub>	Input High Current Breakdown Test (I/O)			100	μA	Max	V <sub>IN</sub> = 5.5V (A <sub>n</sub> , B <sub>n</sub> , C <sub>n</sub> )
I <sub>IL</sub>	Input Low Current			-150	μA	Max	V <sub>IN</sub> = 0.5V (Control Inputs)
V <sub>ID</sub>	Input Leakage Test	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA, All Other Pins Grounded
I <sub>OD</sub>	Output Circuit Leakage Test			3.75	V	0.0	V <sub>IOD</sub> = 150 mV, All Other Pins Grounded
I <sub>IH</sub> + I <sub>OZH</sub>	Output Leakage Current			25	μA	Max	V <sub>OUT</sub> = 2.7V (A <sub>n</sub> , B <sub>n</sub> , C <sub>n</sub> )
I <sub>IIL</sub> + I <sub>OZL</sub>	Output Leakage Current			-150	μA	Max	V <sub>OUT</sub> = 0.5V (A <sub>n</sub> , B <sub>n</sub> , C <sub>n</sub> )
I <sub>OS</sub>	Output Short Circuit Current	-100		-225	mA	Max	V <sub>OUT</sub> = 0.0V (A <sub>n</sub> , B <sub>n</sub> , C <sub>n</sub> )
I <sub>CEX</sub>	Output HIGH Leakage Current			50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub> (A <sub>n</sub> , B <sub>n</sub> , C <sub>n</sub> )
I <sub>ZZ</sub>	Bus Drainage Test			100	μA	0.0	V <sub>OUT</sub> = 5.25V (A <sub>n</sub> , B <sub>n</sub> , C <sub>n</sub> )
I <sub>CCH</sub>	Power Supply Current		115	150	mA	Max	All Outputs HIGH (Note 4)
I <sub>CCL</sub>	Power Supply Current		170	200	mA	Max	All Outputs LOW (Note 4)
I <sub>CCZ</sub>	Power Supply Current		147	175	mA	Max	Outputs in 3-STATE

**Note 4:** 2 ports active only

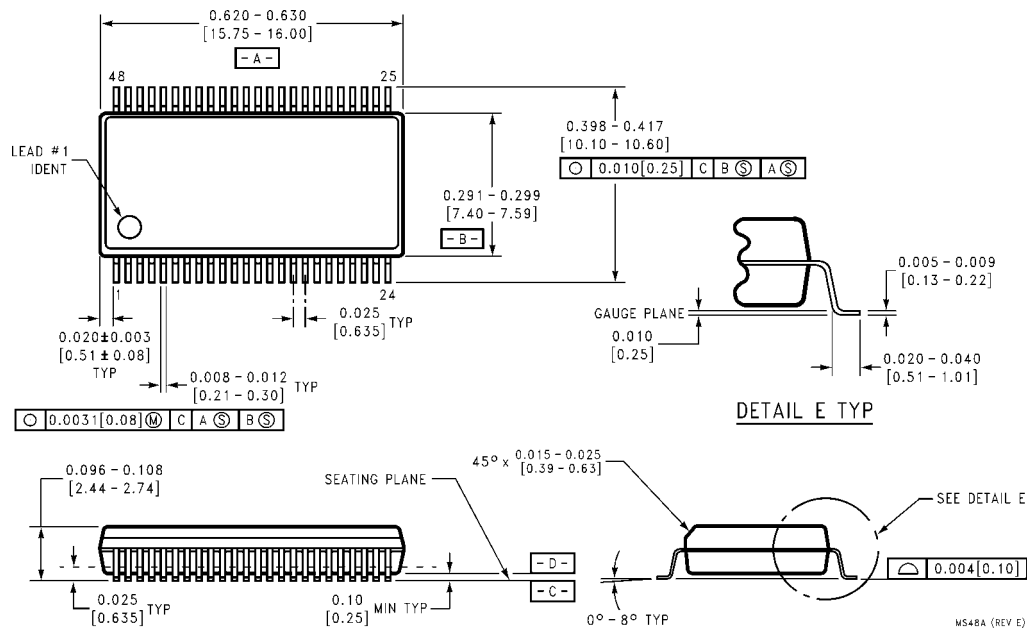
AC Electrical Characteristics							
Symbol	Parameter	$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$		Units
		Min	Typ	Max	Min	Max	
$t_{PLH}$ $t_{PHL}$	Propagation Delay $A_n$ or $B_n$ to $C_n$ $C_n$ to $A_n$ or $B_n$	2.0	4.7	7.5	2.0	7.5	ns
$t_{PLH}$ $t_{PHL}$	Propagation Delay $C_8$ to $A_8$ or $B_8$ (PINV HIGH)	2.5	4.8	7.5	2.5	7.5	ns
$t_{PLH}$ $t_{PHL}$	Propagation Delay $A_n$ to $B_n$ , $B_n$ to $A_n$	4.5	7.0	11.5	4.5	11.5	ns
$t_{PLH}$ $t_{PHL}$	Propagation Delay $\overline{LEAC}$ to $C_n$ , $\overline{LEBC}$ to $C_n$	4.5	6.8	10.0	4.5	10.0	ns
$t_{PLH}$ $t_{PHL}$	Propagation Delay $\overline{LECA}$ to $A_n$ , $\overline{LECB}$ to $B_n$	3.5	6.0	10.0	3.5	10.0	ns
$t_{PLH}$ $t_{PHL}$	Propagation Delay $S_0$ to $C_n$	3.0	6.0	10.0	3.0	10.0	ns
$t_{PLH}$ $t_{PHL}$	Propagation Delay $S_1$ to $A_n$ or $B_n$	4.0	7.0	11.5	4.0	11.5	ns
$t_{PLH}$ $t_{PHL}$	Propagation Delay PINV to $A_8$ or $B_8$	2.5	5.5	9.5	2.5	9.5	ns
$t_{PZH}$ $t_{PZL}$	Output Enable Time $C_n$	1.5	4.0	6.5	1.5	6.5	ns
$t_{PHZ}$ $t_{PLZ}$	Output Disable Time $C_n$	1.5	4.0	6.0	1.5	6.0	ns
$t_{PZH}$ $t_{PZL}$	Output Enable Time $A_n$ , $B_n$	1.5	6.0	8.0	1.5	8.0	ns
$t_{PHZ}$ $t_{PLZ}$	Output Disable Time $A_n$ , $B_n$	1.5	5.0	7.0	1.5	7.0	ns
AC Operating Requirements							
Symbol	Parameter	$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$		Units
		Min	Typ	Max	Min	Max	
$t_S(H)$ $t_S(L)$	Setup Time, HIGH or LOW $A_n$ to $\overline{LEAC}$ , $B_n$ to $\overline{LEBC}$	4.5	2.5		4.5		ns
$t_H(H)$ $t_H(L)$	Hold Time, HIGH or LOW $A_n$ to $\overline{LEAC}$ , $B_n$ to $\overline{LEBC}$	1.0	-1.5		1.0		ns
$t_S(H)$ $t_S(L)$	Setup Time, HIGH or LOW $C_n$ to $\overline{LECA}$ or $\overline{LECB}$	3.0	1.0		3.0		ns
$t_H(H)$ $t_H(L)$	Hold Time, HIGH or LOW $C_n$ to $\overline{LECA}$ or $\overline{LECB}$	1.0	-1.0		1.0		ns
$t_{W(H)}$	$\overline{LE}$ Pulse Width LOW	8.0	4.0		8.0		ns

Extended AC Electrical Characteristics						
Symbol	Parameter	$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$ Nine Outputs Switching (Note 5)		$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 250\text{ pF}$ (Note 6)		Units
		Min	Max	Min	Max	
$t_{PLH}$ $t_{PHL}$	Propagation Delay $A_n$ or $B_n$ to $C_n$ $C_n$ to $A_n$ or $B_n$	2.0	11.5	4.0	12.5	ns
$t_{PLH}$ $t_{PHL}$	Propagation Delay $C_8$ to $A_8$ or $B_8$ (PINV HIGH)			5.5	13.0	ns
$t_{PLH}$ $t_{PHL}$	Propagation Delay $A_n$ to $B_n$ , $B_n$ to $A_n$	4.5	16.0	6.0	16.5	ns
$t_{PLH}$ $t_{PHL}$	Propagation Delay $\overline{LEAC}$ to $C_n$ , $\overline{LEBC}$ to $C_n$	4.5	13.0	5.5	13.5	ns
$t_{PLH}$ $t_{PHL}$	Propagation Delay $\overline{LECA}$ to $A_n$ , $\overline{LECB}$ to $B_n$	3.5	11.5	5.5	14.5	ns
$t_{PLH}$ $t_{PHL}$	Propagation Delay $S_0$ to $C_n$	3.0	11.0	3.0	14.0	ns
$t_{PLH}$ $t_{PHL}$	Propagation Delay $S_1$ to $A_n$ or $B_n$	4.0	16.5	6.5	16.5	ns
$t_{PLH}$ $t_{PHL}$	Propagation Delay PINV to $A_8$ or $B_8$			4.5	14.5	ns
$t_{PZH}$ $t_{PZL}$	Output Enable Time $C_n$	1.5	8.0			ns
$t_{PHZ}$ $t_{PLZ}$	Output Disable Time $C_n$	1.5	6.0			ns
$t_{PZH}$ $t_{PZL}$	Output Enable Time $A_n$ , $B_n$	1.5	8.0			ns
$t_{PHZ}$ $t_{PLZ}$	Output Disable Time $A_n$ , $B_n$	1.5	7.0			ns

**Note 5:** This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase, i.e., all LOW-to-HIGH, HIGH-to-LOW, 3-STATE-to-HIGH, etc.

**Note 6:** This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors standard AC load. This specification pertains to single output switching only.

**Physical Dimensions** inches (millimeters) unless otherwise noted



**48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300 Wide  
Package Number MS48A**

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