

## 74LVQ244

### Low Voltage Octal Buffer/Line Driver with 3-STATE Outputs

#### General Description

The LVQ244 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density.

#### Features

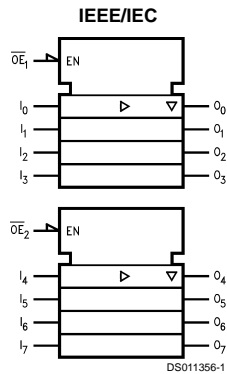
- Ideal for low power/low noise 3.3V applications
- Implements patented EMI reduction circuitry
- Available in SOIC JEDEC, SOIC EIAJ and QSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Improved latch-up immunity
- Guaranteed incident wave switching into 75Ω
- 4 kV minimum ESD immunity

#### Ordering Code:

| Order Number | Package Number | Package Description  |
|--------------|----------------|--|
| 74LVQ244SC   | M20B           | 20-Lead (0.300" Wide) Molded Small Outline Package, SOIC, JEDEC        |
| 74LVQ244SJ   | M20D           | 20-Lead Shrink Molded Small Outline Package, SOIC, EIAJ                |
| 74LVQ244QSC  | MQA20          | 20-Lead (0.150" Wide) Molded Shrink Small Outline Package, SSOP, JEDEC |

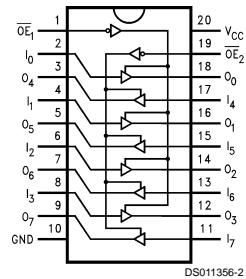
Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

#### Logic Symbol



#### Connection Diagram

Pin Assignment for SOIC and QSOP



## Truth Tables

| Inputs            |       | Outputs<br>(Pins 12, 14, 16, 18) |
|-------------------|-------|----------------------------------|
| $\overline{OE}_1$ | $I_n$ |                                  |
| L                 | L     | L                                |
| L                 | H     | H                                |
| H                 | X     | Z                                |

| Inputs            |       | Outputs<br>(Pins 3, 5, 7, 9) |
|-------------------|-------|------------------------------|
| $\overline{OE}_2$ | $I_n$ |                              |
| L                 | L     | L                            |
| L                 | H     | H                            |
| H                 | X     | Z                            |

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 Z = High Impedance

## Pin Descriptions

| Pin Names                          | Description                  |
|------------------------------------|------------------------------|
| $\overline{OE}_1, \overline{OE}_2$ | 3-STATE Output Enable Inputs |
| $I_0-I_7$                          | Inputs                       |
| $O_0-O_7$                          | Outputs                      |

## Absolute Maximum Ratings (Note 1)

|  |                          |
|--|--------------------------|
| Supply Voltage ( $V_{CC}$ )                                | -0.5V to +7.0V           |
| DC Input Diode Current ( $I_{IK}$ )                        |                          |
| $V_I = -0.5V$  | -20 mA                   |
| $V_I = V_{CC} + 0.5V$                                      | +20 mA                   |
| DC Input Voltage ( $V_I$ )                                 | -0.5V to $V_{CC} + 0.5V$ |
| DC Output Diode Current ( $I_{OK}$ )                       |                          |
| $V_O = -0.5V$  | -20 mA                   |
| $V_O = V_{CC} + 0.5V$                                      | +20 mA                   |
| DC Output Voltage ( $V_O$ )                                | -0.5V to $V_{CC} + 0.5V$ |
| DC Output Source<br>or Sink Current ( $I_O$ )              | ±50 mA                   |
| DC $V_{CC}$ or Ground Current<br>( $I_{CC}$ or $I_{GND}$ ) | ±400 mA                  |
| Storage Temperature ( $T_{STG}$ )                          | -65°C to +150°C          |
| DC Latch-Up Source or<br>Sink Current                      | ±300 mA                  |

## Recommended Operating Conditions (Note 2)

|   |                |
|---|----------------|
| Supply Voltage ( $V_{CC}$ )                 | 2.0V to 3.6V   |
| Input Voltage ( $V_I$ )                     | 0V to $V_{CC}$ |
| Output Voltage ( $V_O$ )                    | 0V to $V_{CC}$ |
| Operating Temperature ( $T_A$ )             | -40°C to +85°C |
| Minimum Input Edge Rate $\Delta V/\Delta t$ |                |
| $V_{IN}$ from 0.8V to 2.0V                  |                |
| $V_{CC}$ @ 3.0V                             | 125 mV/ns      |

**Note 1:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Note 2:** Unused inputs must be held HIGH or LOW. They may not float.

## DC Electrical Characteristics

| Symbol    | Parameter                                | $V_{CC}$<br>(V) | $T_A = +25^\circ C$ |                   | $T_A = -40^\circ C$ to $+85^\circ C$ | Units | Conditions   |
|-----------|--|-----------------|---------------------|-------------------|--------------------------------------|-------|--|
|           |  |                 | Typ                 | Guaranteed Limits |                                      |       |  |
| $V_{IH}$  | Minimum High Level Input Voltage         | 3.0             | 1.5                 | 2.0               | 2.0                                  | V     | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |
| $V_{IL}$  | Maximum Low Level Input Voltage          | 3.0             | 1.5                 | 0.8               | 0.8                                  | V     | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |
| $V_{OH}$  | Minimum High Level Output Voltage        | 3.0             | 2.99                | 2.9               | 2.9                                  | V     | $I_{OUT} = -50 \mu A$  |
|           |  | 3.0             |                     | 2.58              | 2.48                                 | V     | $V_{IN} = V_{IL}$ or $V_{IH}$ (Note 3)<br>$I_{OH} = -12 mA$                          |
| $V_{OL}$  | Maximum Low Level Output Voltage         | 3.0             | 0.002               | 0.1               | 0.1                                  | V     | $I_{OUT} = 50 \mu A$   |
|           |  | 3.0             |                     | 0.36              | 0.44                                 | V     | $V_{IN} = V_{IL}$ or $V_{IH}$ (Note 3)<br>$I_{OL} = 12 mA$                           |
| $I_{IN}$  | Maximum Input Leakage Current            | 3.6             |                     | ±0.1              | ±1.0                                 | μA    | $V_I = V_{CC}, GND$  |
| $I_{OLD}$ | Minimum Dynamic (Note 4) Output Current  | 3.6             |                     |                   | 36                                   | mA    | $V_{OLD} = 0.8V$ Max (Note 5)  |
| $I_{OHD}$ |  | 3.6             |                     |                   | -25                                  | mA    | $V_{OHD} = 2.0V$ Min (Note 5)  |
| $I_{CC}$  | Maximum Quiescent Supply Current         | 3.6             |                     | 4.0               | 40.0                                 | μA    | $V_{IN} = V_{CC}$<br>or $GND$  |
| $I_{OZ}$  | Maximum 3-STATE Leakage Current          | 3.6             |                     | ±0.25             | ±2.5                                 | μA    | $V_I (\overline{OE}) = V_{IL}, V_{IH}$<br>$V_I = V_{CC}, GND$<br>$V_O = V_{CC}, GND$ |
| $V_{OLP}$ | Quiet Output Maximum Dynamic $V_{OL}$    | 3.3             | 0.4                 | 0.8               |                                      | V     | (Notes 6, 7)   |
| $V_{OLV}$ | Quiet Output Minimum Dynamic $V_{OL}$    | 3.3             | -0.4                | -0.8              |                                      | V     | (Notes 6, 7)   |
| $V_{IHD}$ | Minimum High Level Dynamic Input Voltage | 3.3             | 1.7                 | 2.0               |                                      | V     | (Notes 6, 8)   |
| $V_{ILD}$ | Maximum Low Level Dynamic Input Voltage  | 3.3             | 1.7                 | 0.8               |                                      | V     | (Notes 6, 8)   |

**Note 3:** All outputs loaded thresholds on input associated with output under test.

**Note 4:** Maximum test duration 2.0 ms, one output loaded at a time.

**Note 5:** Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

**Note 6:** Worst case package.

**Note 7:** Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.

**Note 8:** Max number of Data Inputs (n) switching. (n - 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold ( $V_{ILD}$ ), 0V to threshold ( $V_{IHD}$ ), f = 1 MHz.

## AC Electrical Characteristics

| Symbol            | Parameter                    | V <sub>CC</sub><br>(V) | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |      |      | T <sub>A</sub> = -40°C to +85°C<br>C <sub>L</sub> = 50 pF |      | Units |
|-------------------|------------------------------|------------------------|--|------|------|---|------|-------|
|                   |                              |                        | Min  | Typ  | Max  | Min   | Max  |       |
| t <sub>PHL</sub>  | Propagation Delay            | 2.7                    | 2.0  | 8.4  | 12.7 | 2.0   | 14.0 | ns    |
| t <sub>PLH</sub>  | Data to Output               | 3.3 ±0.3               | 2.0  | 7.0  | 9.0  | 2.0   | 9.5  |       |
| t <sub>PZL</sub>  | Output Enable Time           | 2.7                    | 2.5  | 9.6  | 16.9 | 2.5   | 18.0 | ns    |
| t <sub>PZH</sub>  |                              | 3.3 ±0.3               | 2.5  | 8.0  | 12.0 | 2.5   | 12.5 |       |
| t <sub>PHZ</sub>  | Output Disable Time          | 2.7                    | 1.0  | 10.8 | 19.0 | 1.0   | 20.0 | ns    |
| t <sub>PLZ</sub>  |                              | 3.3 ±0.3               | 1.0  | 9.0  | 13.5 | 1.0   | 14.0 |       |
| t <sub>OSSL</sub> | Output to Output             | 2.7                    |  | 1.0  | 1.5  |   | 1.5  | ns    |
| t <sub>OSLH</sub> | Skew Data to Output (Note 9) | 3.3 ±0.3               |  | 1.0  | 1.5  |   | 1.5  |       |

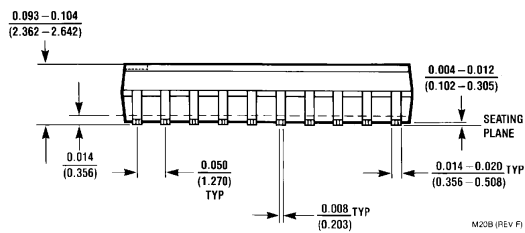
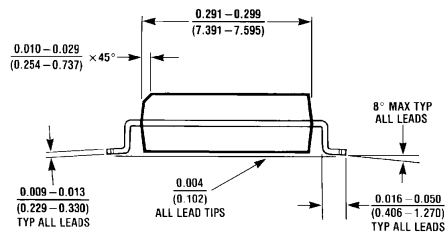
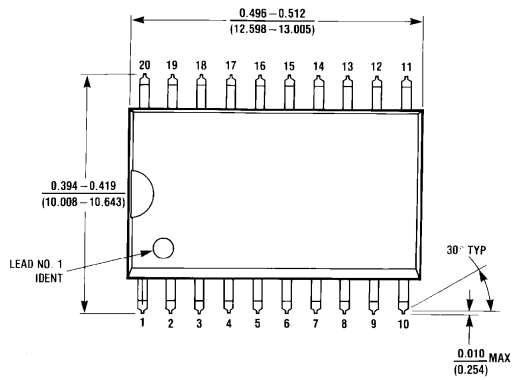
**Note 9:** Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t<sub>OSSL</sub>) or LOW to HIGH (t<sub>OSLH</sub>). Parameter guaranteed by design.

## Capacitance

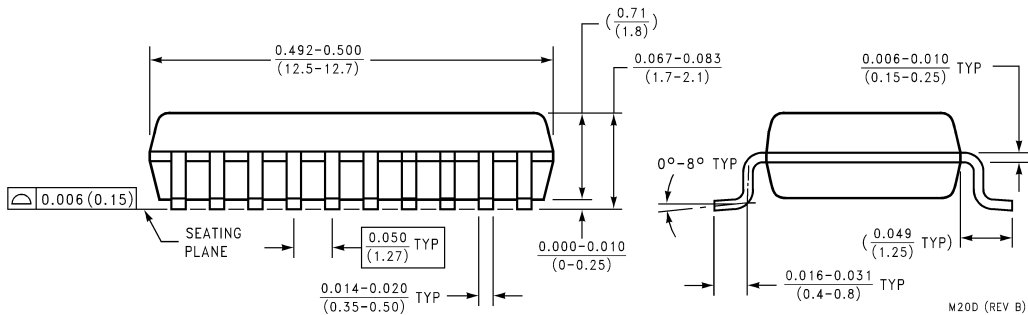
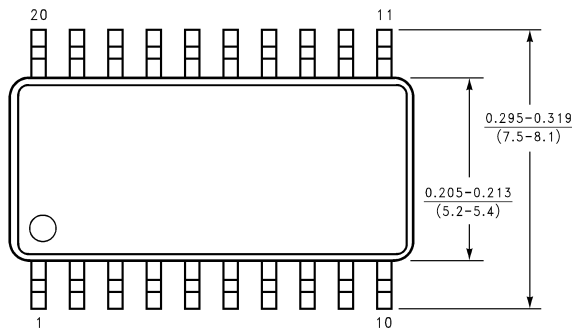
| Symbol                    | Parameter                     | Typ | Units | Conditions             |
|---------------------------|-------------------------------|-----|-------|------------------------|
| C <sub>IN</sub>           | Input Capacitance             | 4.5 | pF    | V <sub>CC</sub> = Open |
| C <sub>PD</sub> (Note 10) | Power Dissipation Capacitance | 70  | pF    | V <sub>CC</sub> = 3.3V |

**Note 10:** C<sub>PD</sub> is measured at 10 MHz.

**Physical Dimensions** inches (millimeters) unless otherwise noted



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Package Number M20B**



**20-Lead Shrink Molded Small Outline Package, SOIC, EIAJ  
Package Number M20D**

