FAIRCHILD SEMICONDUCTOR™

June 1999
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74LVT2245 • 74LVTH2245
Low Voltage Octal Bidirectional Transceiver with 3-STATE Inputs/Outputs and 25Ω Series Resistors in the B Port Outputs (Preliminary)

General Description

The LVT2245 and LVTH2245 contain eight non-inverting bidirectional buffers with 3-STATE outputs and is intended for bus-oriented applications. The Transmit/Receive ($T/\overline{R}$) input determines the direction of data flow through the bidirectional transceiver. Transmit (active-HIGH) enables data from A Ports to B Ports; Receive (active-LOW) enables data from B Ports to A Ports. The Output Enable input, when HIGH, disables both A and B Ports by placing them in a high impedance state. The equivalent 25Ω-series resistor helps reduce output overshoot and undershoot.

The LVTH2245 data inputs include bushold, eliminating the need for external pull-up resistors to hold unused inputs.

These transceivers are designed for low voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT2245 and LVTH2245 are fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining low power dissipation.

Features

- Input and output interface capability to systems at 5V V_{CC}
- Equivalent 25Ω series resistor on B Port outputs
- Bushold data inputs eliminate the need for external pull-up resistors to hold unused inputs (74LVTH2245), also available without bushold feature (74LVT2245)
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink −12 mA/+12 mA on B Port, −32 mA/+64 mA on A Port
- Latch-up performance exceeds 500 mA

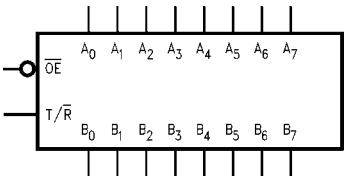
Ordering Code:

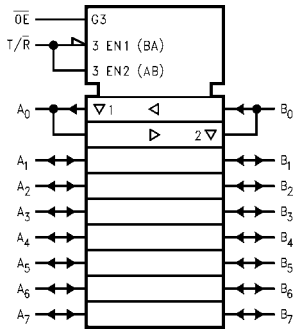
Order Number	Package Number	Package Description
74LVT2245WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, .300" Wide
74LVT2245SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II 5.3mm Wide
74LVT2245MSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
74LVT2245MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74LVTH2245WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, .300" Wide
74LVTH2245SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II 5.3mm Wide
74LVTH2245MSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
74LVTH2245MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

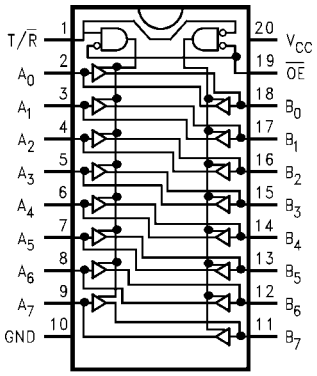
Logic Symbols

IEEE/IEC





Connection Diagram



Pin Descriptions

Pin Names	Description
$\overline{OE}$	Output Enable Input
T/$\overline{R}$	Transmit/Receive Input
A_0–A_7	Side A Inputs or 3-STATE Outputs
B_0–B_7	Side B Inputs or 3-STATE Outputs

Truth Table

Inputs		Outputs
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	HIGH-Z State

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +4.6		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	Output Voltage	−0.5 to +7.0	Output in 3-STATE	V
		−0.5 to +7.0	Output in HIGH or LOW State (Note 2)	
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50	V_O < GND	mA
I_O	DC Output Current	64	$V_O > V_{CC}$ Output at HIGH State	mA
		128	$V_O > V_{CC}$ Output at LOW State	
I_{CC}	DC Supply Current per Supply Pin	±64		mA
I_{GND}	DC Ground Current per Ground Pin	±128		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Recommended Operating Conditions

Symbol	Symbol		Min	Max	Units
V_{CC}	Supply Voltage		2.7	3.6	V
V_I	Input Voltage		0	5.5	V
I_{OH}	HIGH-Level Output Current	A Port		−32	mA
		B Port		−12	
I_{OL}	LOW-Level Output Current	A Port		64	mA
		B Port		12	
T_A	Free Air Operating Temperature		−40	+85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

Note 1: Absolute Maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum rated conditions is not implied.

Note 2: I_O Absolute Maximum Rating must be observed.

DC Electrical Characteristics

Symbol	Parameter		V_{CC} (V)	$T_A = -40°C$ to $+85°C$			Units	Conditions
				Min	Typ (Note 3)	Max		
V_{IK}	Input Clamp Diode Voltage		2.7			−1.2	V	$I_I = -18$ mA
V_{IH}	Input HIGH Voltage		2.7–3.6	2.0			V	$V_O \le 0.1V$ or $V_O \ge V_{CC} - 0.1V$
V_{IL}	Input LOW Voltage		2.7–3.6			0.8	V	
V_{OH}	Output HIGH Voltage	B Port	3.0	2.0			V	$I_{OH} = -12$ mA
		A Port	2.7–3.6	$V_{CC}-0.2$				$I_{OH} = -100$ µA
			2.7	2.4				$I_{OH} = -12$ mA
			3.0	2.0				$I_{OH} = -32$ mA
V_{OL}	Output LOW Voltage	B Port	3.0			0.8	V	$I_{OL} = 12$ mA
		A Port	2.7			0.2		$I_{OL} = 100$ µA
			2.7			0.5		$I_{OL} = 24$ mA
			3.0			0.4		$I_{OL} = 16$ mA
			3.0			0.5		$I_{OL} = 32$ mA
			3.0			0.55		$I_{OL} = 64$ mA
$I_{I(HOLD)}$ (Note 4)	Bushold Input Minimum Drive		3.0	75			µA	$V_I = 0.8V$
				−75				$V_I = 2.0V$
$I_{I(OD)}$ (Note 4)	Bushold Input Over-Drive Current to Change State		3.0	500			µA	(Note 5)
				−500				(Note 6)
I_I	Input Current		3.6			10	µA	$V_I = 5.5V$
		Control Pins	3.6			±1		$V_I = 0V$ or V_{CC}
		Data Pins	3.6			−5		$V_I = 0V$
						1		$V_I = V_{CC}$
I_{OFF}	Power Off Leakage Current		0			±100	µA	$0V \le V_I$ or $V_O \le 5.5V$
$I_{PU/PD}$	Power Up/Down 3-STATE Current		0–1.5V			±100	µA	$V_O = 0.5V$ to $3.0V$, $V_I = GND$ or V_{CC}
I_{OZL}	3-STATE Output Leakage Current		3.6			−5	µA	$V_O = 0.5V$
I_{OZH}	3-STATE Output Leakage Current		3.6			5	µA	$V_O = 3.0V$
$I_{OZH}+$	3-STATE Output Leakage Current		3.6			10	µA	$V_{CC} < V_O \le 5.5V$
I_{CCH}	Power Supply Current		3.6			0.19	mA	Outputs High
I_{CCL}	Power Supply Current		3.6			5	mA	Outputs Low
I_{CCZ}	Power Supply Current		3.6			0.19	mA	Outputs Disabled
$I_{CCZ}+$	Power Supply Current		3.6			0.19	mA	$V_{CC} \le V_O \le 5.5V$, Outputs Disabled
ΔI_{CC}	Increase in Power Supply Current (Note 7)		3.6			0.2	mA	One Input at $V_{CC} - 0.6V$, Other Inputs at V_{CC} or GND

Note 3: All typical values are at $V_{CC} = 3.3V$, $T_A = 25°C$.

Note 4: Applies to Bushold versions only (74LVTH2245).

Note 5: An external driver must source at least the specified current to switch from LOW-to-HIGH.

Note 6: An external driver must sink at least the specified current to switch from HIGH-to-LOW.

Note 7: This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

Dynamic Switching Characteristics (Note 8)

Symbol	Parameter	V_{CC} (V)	$T_A = 25°C$			Units	Conditions $C_L = 50$ pF, $R_L = 500\Omega$
			Min	Typ	Max		
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3		0.8		V	(Note 9)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3		−0.8		V	(Note 9)

Note 8: Characterized in SOIC package. Guaranteed parameter, but not tested.

Note 9: Max number of outputs defined as (n). n–1 data inputs are driven 0V to 3V. Output under test held LOW.

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF, $R_L = 500\Omega$					Units
		$V_{CC} = 3.3V \pm 0.3V$			$V_{CC} = 2.7V$		
		Min	Typ (Note 10)	Max	Min	Max	
t_{PLH}	Propagation Delay Data to B Port Output	1.1		4.0	1.1	4.6	ns
t_{PHL}		1.1		3.7	1.1	4.1	
t_{PLH}	Propagation Delay Data to A Port Output	1.4		3.5	1.4	4.0	ns
t_{PHL}		1.0		3.5	1.0	4.0	
t_{PZH}	Output Enable Time for B Port Output	1.3		5.3	1.3	6.3	ns
t_{PZL}		2.0		5.6	2.0	7.2	
t_{PZH}	Output Enable Time for A Port Output	1.6		5.5	1.6	7.1	ns
t_{PZL}		1.8		5.5	1.8	6.5	
t_{PHZ}	Output Disable Time for B Port Output	2.7		5.6	2.7	6.3	ns
t_{PLZ}		2.4		5.5	2.4	5.5	
t_{PHZ}	Output Disable Time for A Port Output	2.5		5.9	2.5	6.5	ns
t_{PLZ}		2.4		5.0	2.4	5.1	
t_{OSHL}	A Port Output to Output Skew			1.0		1.0	ns
t_{OSLH}	(Note 11)						
t_{OSHL}	B Port Output to Output Skew			1.0		1.0	ns
t_{OSLH}	(Note 11)						

Note 10: All typical values are at $V_{CC} = 3.3V$, $T_A = 25°C$.

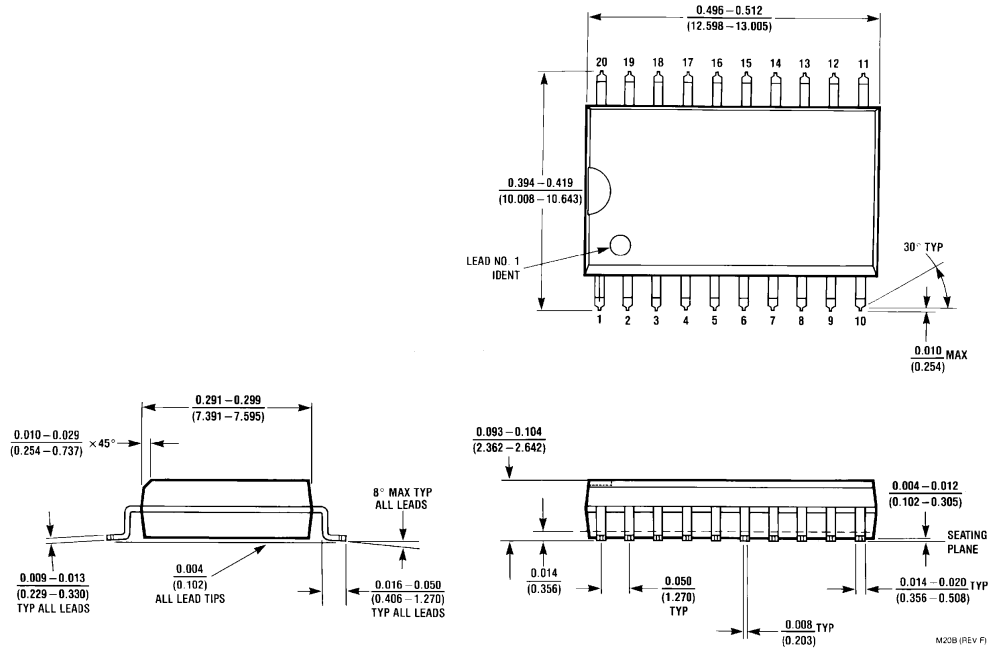
Note 11: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

Capacitance (Note 12)

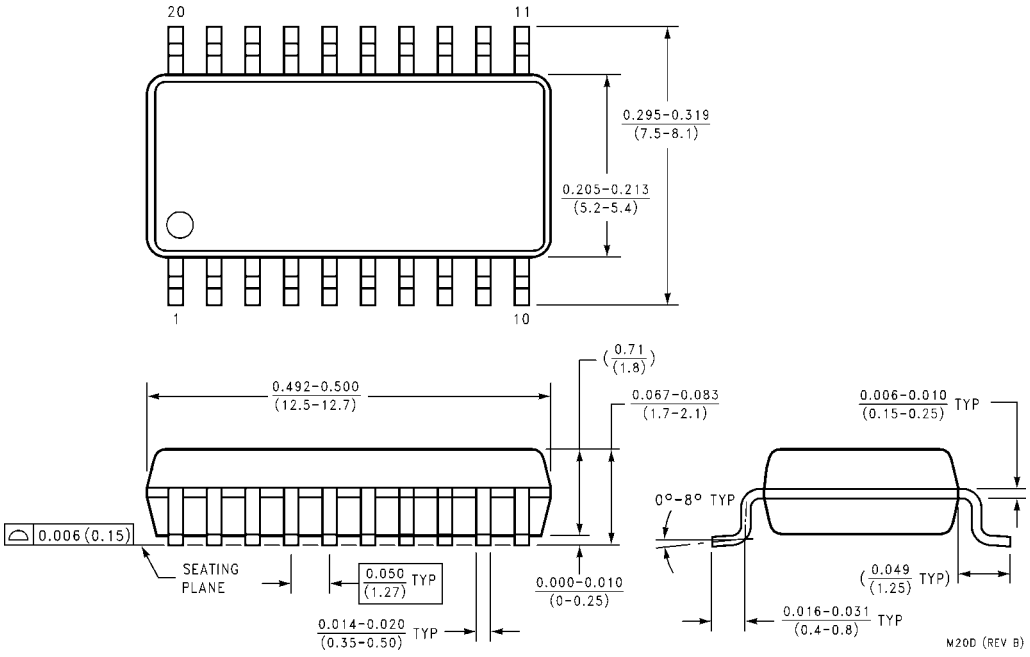
Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	$V_{CC} = 0V$, $V_I = 0V$ or V_{CC}	4	pF
$C_{I/O}$	Input/Output Capacitance	$V_{CC} = 3.0V$, $V_O = 0V$ or V_{CC}	8	pF

Note 12: Capacitance is measured at frequency f = 1 MHz, per MIL-STD-883B, Method 3012.

Physical Dimensions inches (millimeters) unless otherwise noted

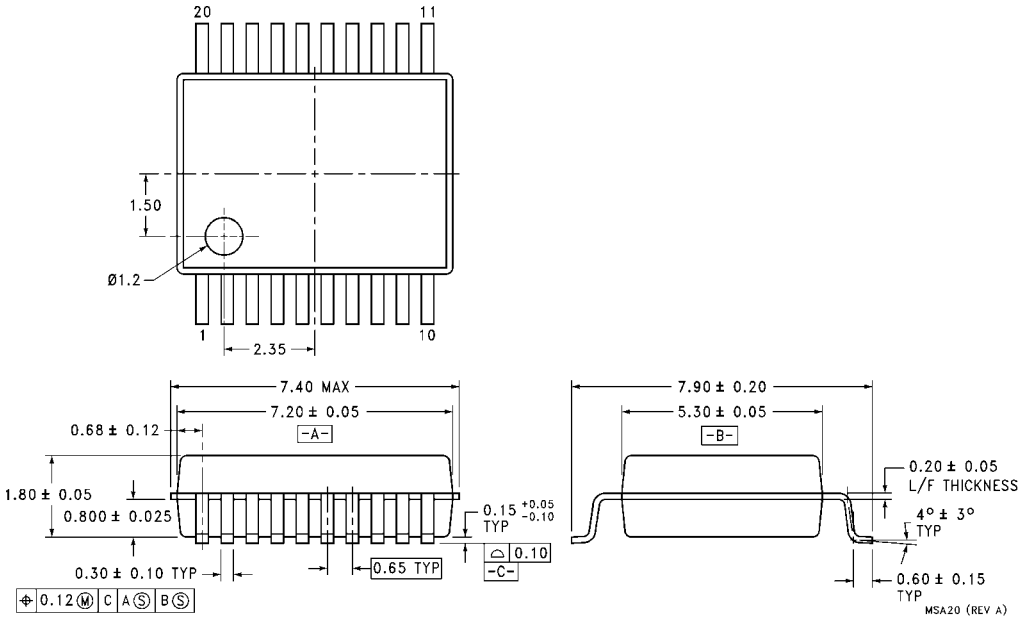


20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, .300" Wide
Package Number M20B



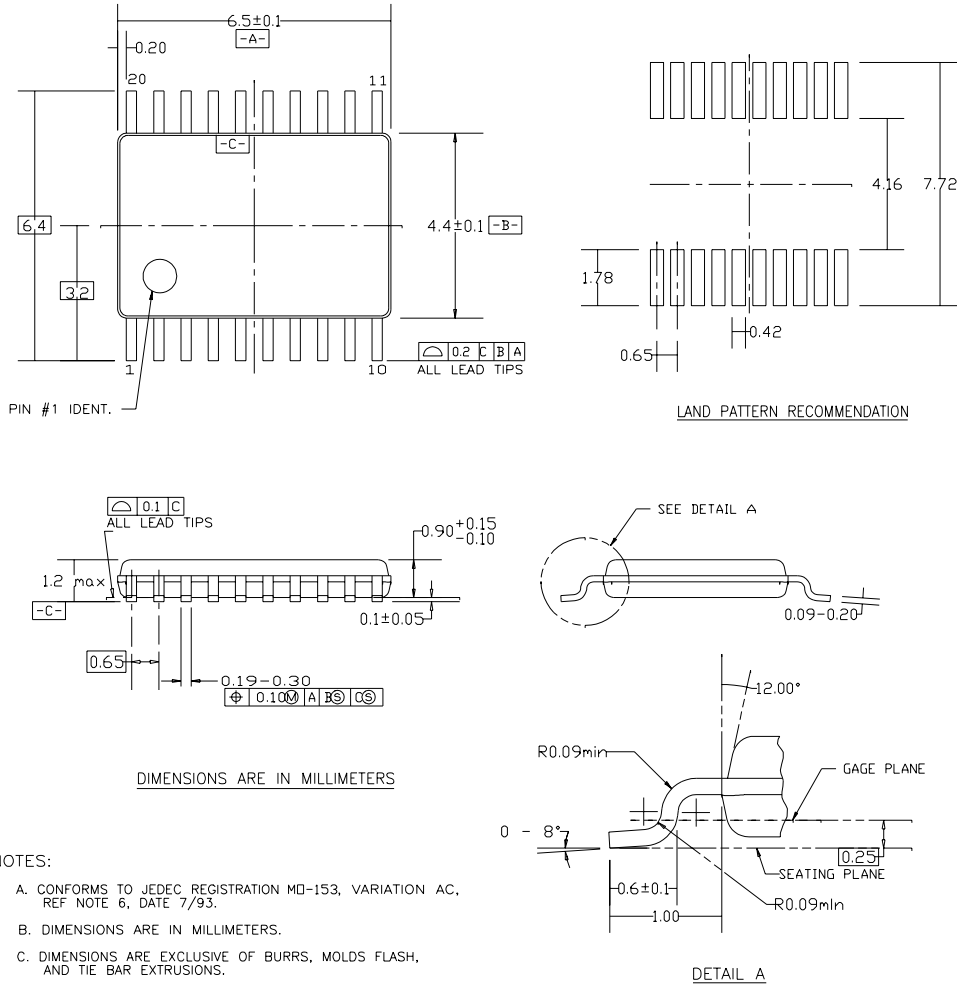
20-Lead Small Outline Package (SOP), EIAJ TYPE II 5.3mm Wide
Package Number M20D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
Package Number MSA20

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO−153, VARIATION AC, REF NOTE 6, DATE 7/93.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC20

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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