

74LVTH273 Low Voltage Octal D-Type Flip-Flop with Clear

General Description

The LVTH273 is a high-speed, low-power positive-edge-triggered octal D-type flip-flop featuring separate D-type inputs for each flip-flop. A buffered Clock (CP) and Clear (CLR) are common to all flip-flops.

The state of each D-type input, one setup time before the positive clock transition, is transferred to the corresponding flip-flop's output.

The LVTH273 data inputs include bushhold, eliminating the need for external pull-up resistors to hold unused inputs.

These octal flip-flops are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVTH273 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining low power dissipation.

Features

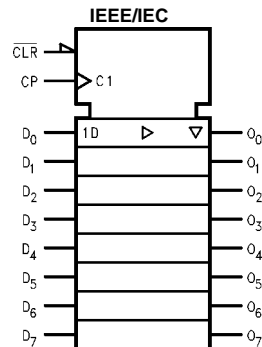
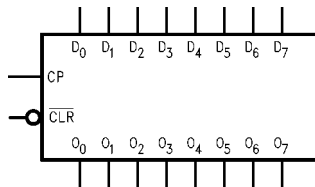
- Input and output interface capability to systems at 5V V_{CC}
- Bushhold on the data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Outputs source/sink -32 mA/+64 mA
- Functionally compatible with the 74 series 273
- Latch-up performance exceeds 500 mA

Ordering Code:

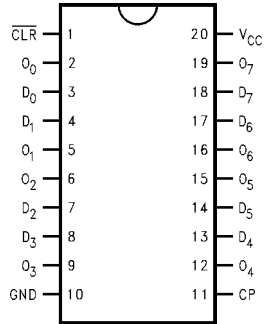
Order Number	Package Number	Package Description
74LVTH273WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74LVTH273SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II 5.3mm Wide
74LVTH273MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Logic Symbols



Connection Diagram



Pin Descriptions

Pin Names	Description
D ₀ -D ₇	Data Inputs
CP	Clock Pulse Input
$\overline{\text{CLR}}$	Clear
O ₀ -O ₇	Outputs

Truth Table

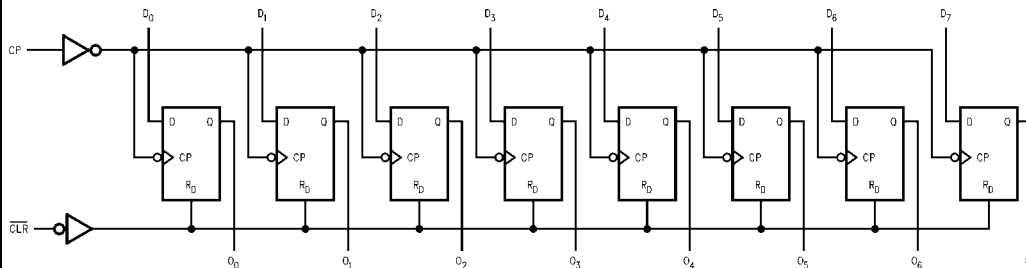
Inputs			Outputs
D _n	CP	$\overline{\text{CLR}}$	O _n
H	↗	H	H
L	↗	H	L
X	H or L	H	O ₀
X	X	L	L

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 ↗ = LOW-to-HIGH Transition
 O₀ = Previous O₀ before HIGH-to-LOW of CP

Functional Description

The LVTH273 consists of eight positive-edge-triggered flip-flops with individual D-type inputs. The buffered Clock and Clear are common to all flip-flops. The eight flip-flops will store the state of their individual D-type inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. When the Clock is either HIGH or LOW, the D-input signal has no effect at the output. When the Clear ($\overline{\text{CLR}}$) is LOW, all Outputs will be forced LOW.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings ^(Note 1)					
Symbol	Parameter	Value	Conditions		Units
V _{CC}	Supply Voltage	-0.5 to +4.6			V
V _I	DC Input Voltage	-0.5 to +7.0			V
V _O	DC Output Voltage	-0.5 to +7.0	Output in HIGH or LOW State (Note 2)		V
I _{IK}	DC Input Diode Current	-50	V _I < GND		mA
I _{OK}	DC Output Diode Current	-50	V _O < GND		mA
I _O	DC Output Current	64	V _O > V _{CC} Output at HIGH State		mA
		128	V _O > V _{CC} Output at LOW State		
I _{CC}	DC Supply Current per Supply Pin	±64			mA
I _{GND}	DC Ground Current per Ground Pin	±128			mA
T _{STG}	Storage Temperature	-65 to +150			°C

Recommended Operating Conditions				
Symbol	Parameter	Min	Max	Units
V _{CC}	Supply Voltage	2.7	3.6	V
V _I	Input Voltage	0	5.5	V
I _{OH}	HIGH Level Output Current		-32	mA
I _{OL}	LOW Level Output Current		64	mA
T _A	Free-Air Operating Temperature	-40	85	°C
Δt/ΔV	Input Edge Rate, V _{IN} = 0.8V-2.0V, V _{CC} = 3.0V	0	10	ns/V

Note 1: Absolute Maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum rated conditions is not implied.

Note 2: I_O Absolute Maximum Rating must be observed.

DC Electrical Characteristics								
Symbol	Parameter	V _{CC} (V)	T _A = -40°C to +85°C			Units	Conditions	
			Min	Typ (Note 3)	Max			
V _{IK}	Input Clamp Diode Voltage	2.7			-1.2	V	I _I = -18 mA	
V _{IH}	Input HIGH Voltage	2.7-3.6	2.0			V	V _O ≤ 0.1V or	
V _{IL}	Input LOW Voltage	2.7-3.6			0.8	V	V _O ≥ V _{CC} - 0.1V	
V _{OH}	Output HIGH Voltage	2.7-3.6	V _{CC} - 0.2			V	I _{OH} = -100 μA	
		2.7	2.4				I _{OH} = -8 mA	
		3.0	2.0				I _{OH} = -32 mA	
V _{OL}	Output LOW Voltage	2.7			0.2	V	I _{OL} = 100 μA	
		2.7			0.5		I _{OL} = 24 mA	
		3.0			0.4		I _{OL} = 16 mA	
		3.0			0.5		I _{OL} = 32 mA	
		3.0			0.55		I _{OL} = 64 mA	
I _{I(HOLD)}	Bushold Input Minimum Drive	3.0	75			μA	V _I = 0.8V	
			-75				V _I = 2.0V	
I _{I(OD)}	Bushold Input Over-Drive Current to Change State	3.0	500			μA	(Note 4)	
			-500				(Note 5)	
I _I	Input Current	3.6			10	μA	V _I = 5.5V	
		Control Pins	3.6		±1		μA	V _I = 0V or V _{CC}
		Data Pins	3.6		-5		μA	V _I = 0V
					1		μA	V _I = V _{CC}
I _{OFF}	Power Off Leakage Current	0			±100	μA	0V ≤ V _I or V _O ≤ 5.5V	
I _{CCH}	Power Supply Current	3.6			0.19	mA	Outputs HIGH	
I _{CCL}	Power Supply Current	3.6			5	mA	Outputs LOW	
ΔI _{CC}	Increase in Power Supply Current (Note 6)	3.6			0.2	mA	One Input at V _{CC} - 0.6V Other Inputs at V _{CC} or GND	

DC Electrical Characteristics (Continued)

Note 3: All typical values are at $V_{CC} = 3.3V$, $T_A = 25^\circ C$.

Note 4: An external driver must source at least the specified current to switch from LOW-to-HIGH.

Note 5: An external driver must sink at least the specified current to switch from HIGH-to-LOW.

Note 6: This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

Dynamic Switching Characteristics (Note 7)

Symbol	Parameter	V_{CC} (V)	$T_A = 25^\circ C$			Units	Conditions $C_L = 50 \text{ pF}$, $R_L = 500\Omega$
			Min	Typ	Max		
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3		0.8		V	(Note 8)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3		-0.8		V	(Note 8)

Note 7: Characterized in SOIC package. Guaranteed parameter, but not tested.

Note 8: Max number of outputs defined as (n). n-1 data inputs are driven 0V to 3V. Output under test held LOW.

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40^\circ C \text{ to } +85^\circ C$					Units
		$C_L = 50 \text{ pF}, R_L = 500\Omega$					
		$V_{CC} = 3.3V \pm 0.3V$			$V_{CC} = 2.7V$		
		Min	Typ (Note 9)	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	150			150		MHz
t_{PLH}	Propagation Delay	1.7		4.9	1.7	5.5	ns
t_{PHL}	CP to O_n	1.9		4.8	1.9	5.1	ns
t_{PHL}	Propagation Delay \overline{CLR} to O_n	1.6		4.8	1.6	5.4	ns
t_W	Pulse Duration	3.3			3.3		ns
t_S	Setup Time	Data HIGH or LOW before CP	2.3		2.7		ns
		\overline{CLR} HIGH before CP	2.3		2.7		ns
t_H	Hold Time	Data HIGH or LOW after CP	0		0		ns

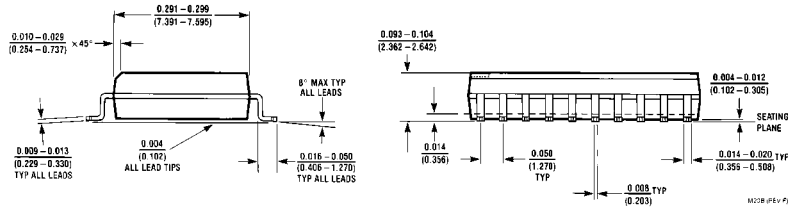
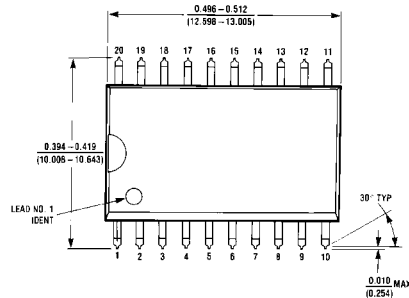
Note 9: All typical values are at $V_{CC} = 3.3V$, $T_A = 25^\circ C$.

Capacitance (Note 10)

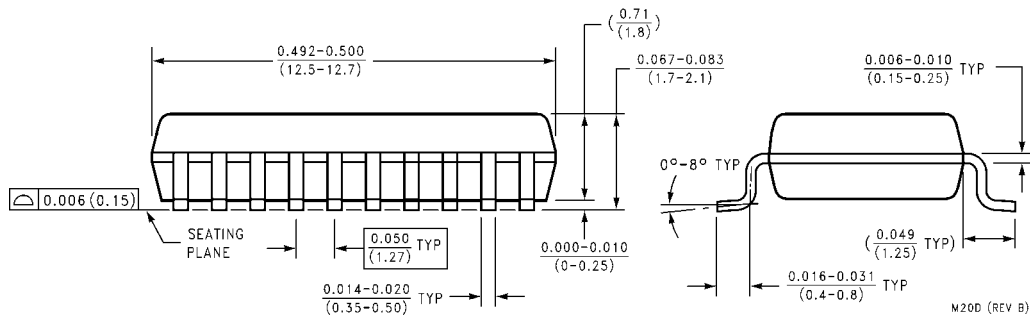
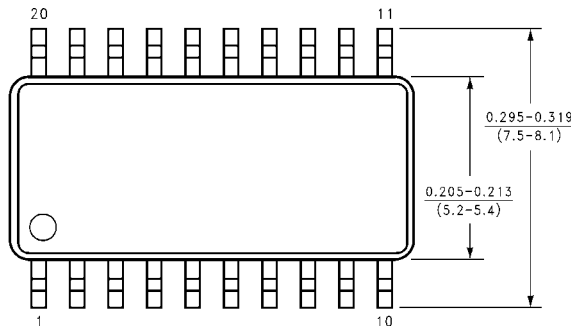
Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	$V_{CC} = 0V, V_I = 0V \text{ or } V_{CC}$	3	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.0V, V_O = 0V \text{ or } V_{CC}$	6	pF

Note 10: Capacitance is measured at frequency $f = 1 \text{ MHz}$, per MIL-STD-883B, Method 3012.

Physical Dimensions inches (millimeters) unless otherwise noted

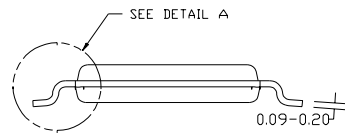
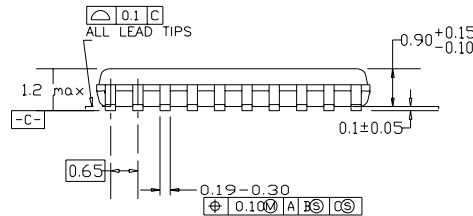
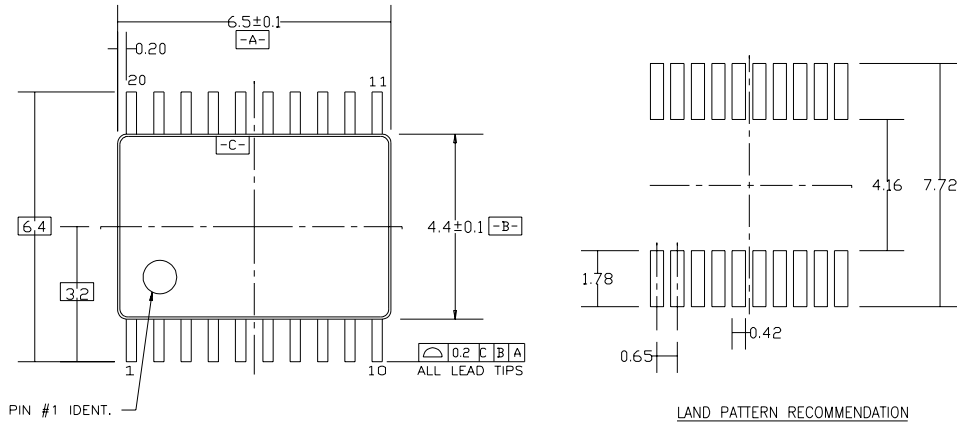


**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M20B**

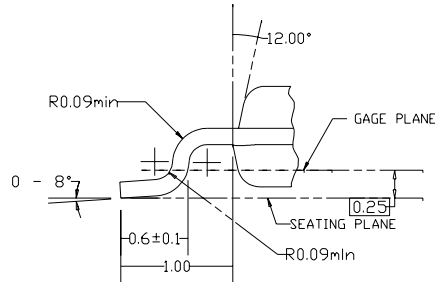


**20-Lead Small Outline Package (SOP), EIAJ TYPE II 5.3mm Wide
Package Number M20D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS



DETAIL A

NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND THE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

**20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC20**

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